General Information

Features

- Companion to the IBM PowerPRS™ 64G Packet Routing Switch and the IBM PowerPRS C192 Common Switch Interface
- PowerPRS C192-compatible Unilink serial interface to PowerPRS 64G-compatible data-aligned synchronous link (DASL) serial interface conversion
- Unilink interface: serial data communication of up to 2.5 Gbps, compatible with InfiniBand™ physical layer standards
- DASL interface: serial data communication of up to 500 Mbps, compliant with Electronic Industries Association/JEDEC Standard No. 8-6 regarding high-speed transceiver logic (HSTL)
- Synchronous clocks on the Unilink and DASL high-speed serial interfaces
- Port speed of 16 Gbps
- Configurable packet length of 64, 68, 72, 76, or 80 bytes
- 16- to 20-byte logical unit (LU) packet processing with PowerPRS 64G four-way port paralleling
- No queuing (pass-through device)
- Send grant and memory grant flow control serialization
- PowerPRS 64G-compatible header parity checking and computation
- DASL cyclic redundancy check (CRC) generation and checking
- Detection of link liveness by reception of specific packets
- 8b/10b encoding/decoding for link synchronization and supervision
- Control resources for internal register display
- Serial processor interface (serial host interface) or eight-bit parallel processor interface to access all registers for control and error reporting
- Internal loopback support for both the PowerPRS 64G and PowerPRS C192
- Internal logic built-in self-test (BIST) and memory BIST
- CMOS 7SF (SA-27E) technology (L_{drawn} = 0.18 µm, L_{eff} = 0.11 µm):
  - 2.5-V LVCMOS-compatible (3.3-V tolerant) I/Os for microprocessor interfaces
  - 1.8-V LVCMOS-compatible test I/Os
- 1.8-V DASL differential I/Os
- IEEE Standard 1149.1 boundary scan to facilitate circuit-board testing
- 399-ball IBM HyperBGA™ package

Description

The IBM PowerPRS Switch Core Interface Chip (SCIC) is a companion device to the IBM PowerPRS 64G Packet Routing Switch. It connects the switch's 32 data-aligned synchronous links (DASLs), which operate between 425 and 500 Mbps, to the PowerPRS C192's eight high-speed serial links (Unilinks), which operate between 2.125 and 2.5 Gbps. The PowerPRS C192 functions as the switch core access layer between the protocol engine and the high-speed serial links. Both the PowerPRS SCIC and the PowerPRS C192 use the same 8b/10b line coding scheme as the fiber channel standard.

The PowerPRS SCIC receives data from incoming PowerPRS C192 packets, which are formatted in logical units (LUs) of 16 to 20 bytes for compatibility with the PowerPRS 64G. The PowerPRS SCIC alternately decodes the corresponding bytes of the two LUs carried on each Unilink to feed the four

DASL ports, which then carry the corresponding nibbles. The PowerPRS SCIC realigns the Unilink and DASL ports to maintain the correct timing offset between the physical ports.

The PowerPRS SCIC resolves all the clock phase differences between its input and output, assuming that both the receive and transmit clocks have the same frequency. The PowerPRS SCIC also transmits the DASL synchronization pattern, which is controlled by the local processor.

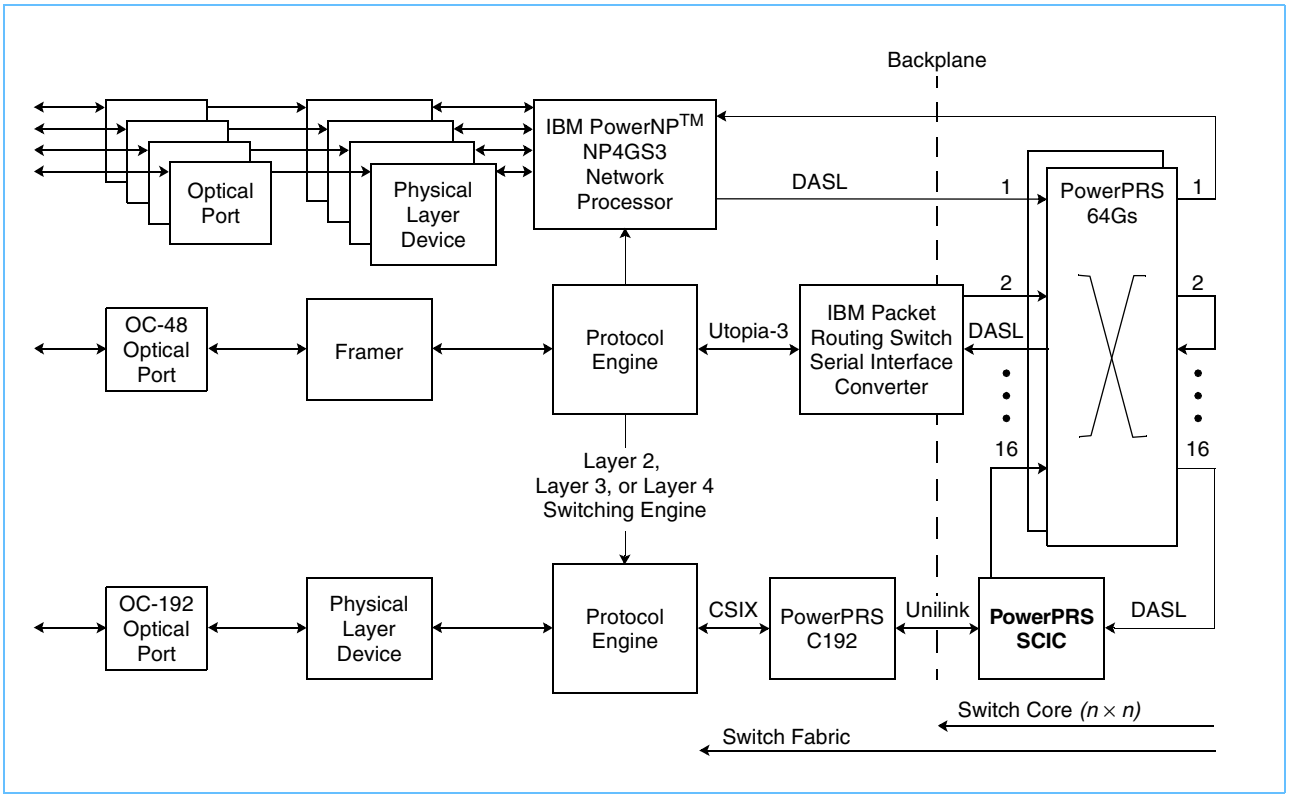
Ordering Information

Part Number	Description	Throughput
IBM3213P0102	IBM Switch Core Interface Chip	16 Gbps

Architecture

In the system architecture illustrated in *Figure 1,* the PowerPRS SCIC is connected to four PowerPRS 64G DASL ports configured for port paralleling, on the right side, and to eight PowerPRS C192 Unilinks, on the left side. In a PowerPRS 64G-based switch core application, the PowerPRS C192 is attached between the switch fabric and the CSIX-compliant protocol engine to produce an OC-192 port.

Figure 1. System View of the PowerPRS SCIC with the Network Processor and Packet Routing Switches



The internal structure of the PowerPRS SCIC is shown in *Figure 2*. The PowerPRS SCIC is comprised of two nearly symmetrical data flows: the ingress flow and the egress flow. To control the traffic flow, send grant and shared memory grant bits are exchanged between the PowerPRS 64G and the PowerPRS C192. The PowerPRS C192 codes up to four send-grant bits (one per priority) in the ingress packet headers before forwarding the packets to the PowerPRS SCIC. The PowerPRS SCIC decodes these bits and sends the data to the PowerPRS 64G via the send grant signal. The PowerPRS 64G sends up to four shared memory grant signals (one per priority) to the PowerPRS SCIC in the same way. The PowerPRS SCIC codes the memory grant bits into the egress packet headers before forwarding the packets to the PowerPRS C192. The PowerPRS C192 then decodes the memory grant bits.

The PowerPRS SCIC is also comprised of a programming interface that provides access to all the internal registers and two phase-locked loops (PLLs), one for Unilink clocks and the other for DASL and internal clocks. The two PLLs are fed by the same clock source so that the Unilinks, DASLs, and all internal logic (except the programming interface) are synchronous. For this reason, there is no packet buffer. On the DASL interface, the throughput is 16 Gbps; on the Unilink interface, it is 20 Gbps. However, the Unilink data is coded in 8b/10b to produce a 16-Gbps throughput of usable data.

Figure 2. PowerPRS SCIC Block Diagram

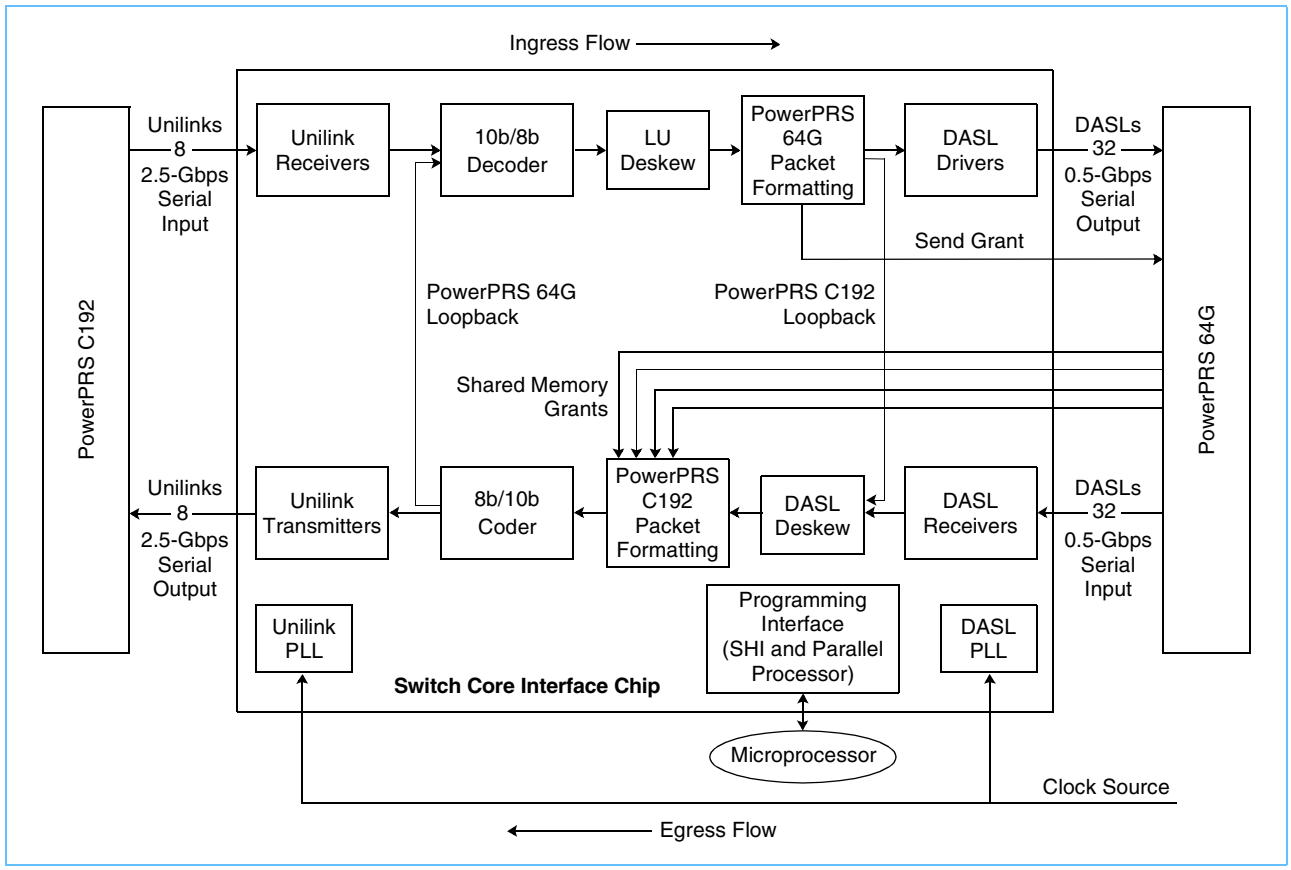


Table 1. PowerPRS SCIC Block Descriptions

Block	Description
Unilink receivers	Deserialize the 2.5-Gbps serial data and transform it into 10-bit parallel bus data. The Unilink receivers also resynchronize the ingress packets according to the PowerPRS SCIC internal clock.
8b/10b coder/decoder	Codes/decodes data in 8b/10b code to improve transmission and synchronization. Code violations are detected by the decoder.
LU deskew	Rearranges the logical unit (LU) sequence to resolve the various link delays that accumulate on the eight Unilink paths (for example, during clock resynchronization). The LU deskew process is performed during synchronization when traffic is comprised of idle packets only.
PowerPRS 64G packet formatting	Analyzes each ingress packet qualifier byte (H0) to characterize the packet type, and extracts the send grant bits. Checks the header parity, and calculates the cyclic redundancy check (CRC) and inserts it into the idle packets. Modifies idle packet and synchronization packet format for DASL compatibility.
DASL drivers and receivers	Serialize or deserialize the data packets on the four DASL switch ports.
DASL deskew	Rearranges the switch port sequence to resolve the various link delays that accumulate on the four DASL paths. The DASL deskew process is performed during synchronization when traffic is comprised of synchronization packets only.
PowerPRS C192 packet formatting	Analyzes each egress packet qualifier byte (H0) to characterize the packet type. Checks the header parity, inserts the shared memory grant bits, recalculates the header parity, and calculates the CRC and inserts it into the idle packets. Modifies the idle packet format for Unilink compatibility.

Table 1. PowerPRS SCIC Block Descriptions

Block	Description
Unilink transmitters	Resynchronize the egress data packets according to the Unilink clocks, and serialize the internal 10-bit bus data into 2.5-Gbps serial data.
Unilink and DASL PLLs	Generate all the clocks for the Unilinks, DASLs, and internal logic (except the programming interface, which has a separate clock).
Programming interface	Allows access to all the internal registers.

Programming Interface and Registers

The PowerPRS SCIC employs two programming interfaces:

- Serial host interface (SHI)
- Parallel processor interface (eight bits)

The SHI is the same programming interface used in the PowerPRS 64G, and the eight-bit parallel processor interface is the same programming interface used in the PowerPRS C192. Only one of these programming interfaces may be used in a given application.

The programming interface provides the read/write access to all the PowerPRS SCIC internal registers; DASL picocode downloading; and diagnostic functions, such as online error detection and reporting, and built-in self-test (BIST).

Table 2 summarizes the registers that provide the mechanism for PowerPRS SCIC configuration specification and status reporting. Registers x‘01’ to x‘09’ are power-on registers; they are reset by activating the PowerOnReset# signal and are clocked with the processor interface clock. These registers can be accessed before the phase-locked loop (PLL) is started or the flush is complete.

Table 2. Register Summary (Page 1 of 3)

Register Name	Address	Access
Power-On Registers: x‘00’ to x‘09’		
Status Register	x‘00’	Read Only and Read/Clear
Internal/DASL PLL Programming Register	x‘01’	Read/Write
Internal/DASL PLL Status Register	x‘02’	Read Only
Unilink PLL Programming Register	x‘03’	Read/Write
Unilink PLL Status Register	x‘04’	Read Only
Reset Register	x‘05’	Read/Write
Interrupt Mask Register	x‘06’	Read/Write
BIST Counter Register	x‘07’	Read/Write
BIST Data Register	x‘08’	Read/Write
BIST Select Register	x‘09’	Read/Write
Application Registers: x‘0A’ to x‘0F’		
General Configuration Register	x‘0A’	Read/Write
Yellow Packet Register	x‘0B’	Read/Clear
Packet Error Register	x‘0C’	Read/Clear
Egress Deskew Status Register	x‘0D’	Read Only
Egress Deskew Command Register	x‘0E’	Read/Write
Debug Bus Select Register	x‘0F’	Read/Write

Table 2. Register Summary (Page 2 of 3)

Register Name	Address	Access
Unilink Programming Registers: x‘10’ to x‘29’		
Unilink Receive Command Register	x‘10’	Read/Write
Unilink Transmit Command Register	x‘11’	Read/Write
Unilink Synchronization Status 1 Register	x‘12’	Read Only
Unilink Synchronization Status 2 Register	x‘13’	Read Only
Unilink Synchronization Status 3 Register	x‘14’	Read Only
Unilink Ingress Deskew Register	x‘15’	Read/Write
Unilink Receive Offset Register	x‘16’	Read/Write
Unilink Transmit Offset Register	x‘17’	Read/Write
Unilink Receive BIST Command Register	x‘18’	Read/Write
Unilink Transmit BIST Command Register	x‘19’	Read/Write
Unilink Error 1 Register	x‘1A’	Read Only
Unilink Error 2 Register	x‘1B’	Read/Clear
Unilink Force Error Register	x‘1C’	Read/Write
Unilink Power Level Register	x‘1D’	Read/Write
Unilink FIR C0 Register	x‘1E’	Read/Write
Unilink FIR C1 Register	x‘1F’	Read/Write
Unilink FIR C2 Register	x‘20’	Read/Write
Unilink FIR C3 Register	x‘21’	Read/Write
Unilink Phase Rotator/Sample Registers	x‘22’ to x‘29’	Read/Write and Read Only
DASL Programming Registers: x‘30’ to x‘3E’		
DASL Output Driver Enable Register	x‘30’	Read/Write
Output Port Enable Register	x‘31’	Read/Write
Input Port Enable Register	x‘33’	Read/Write
DASL Status Register	x‘34’	Read Only
SDC RLOS Enable Register	x‘35’	Read/Write
DASL Synchronization Hunt Register	x‘36’	Read/Write
Picoprocessor Instruction Memory Access Register	x‘37’	Read/Write
DASL Configuration Register	x‘38’	Read/Write
DASL Port Error/Quality Register	x‘39’	Read Only
DASL Port Quality Mask Register	x‘3A’	Read/Write
SDC Resource Control Register	x‘3B’	Read/Write

Table 2. Register Summary (Page 3 of 3)

Register Name	Address	Access
SDC Resource Address Register	x‘3C’	Read/Write
SDC Resource Data Register	x‘3D’	Read/Write
SDC Status Register	x‘3E’	Read Only

Electrical Information

All functional I/O signals are 3.3-V tolerant 2.5-V CMOS-compatible drivers and receivers, except the following:

- Unilink interface signals (common mode logic)
- DASL interface signals (high-speed transceiver logic)
- DASL and Unilink clock and PLL signals (low-voltage pseudoemitter-coupled logic)
- Test signals (1.8-V CMOS-compatible drivers and receivers)

Figure 3. Pinout (399-ball HyperBGA package, bottom view)

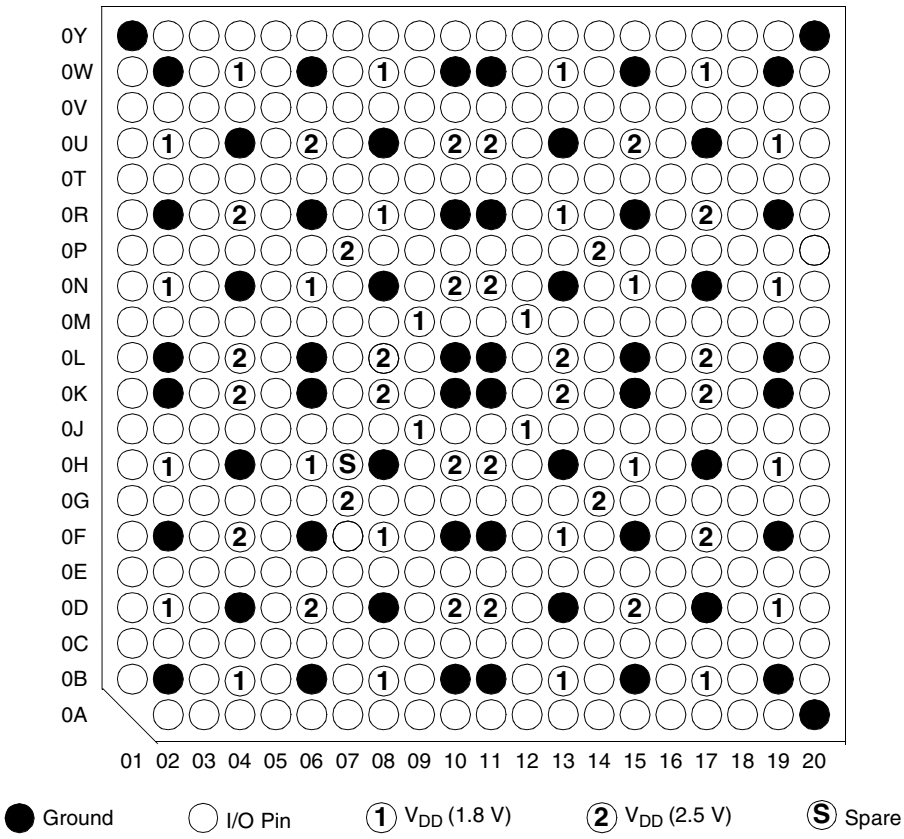


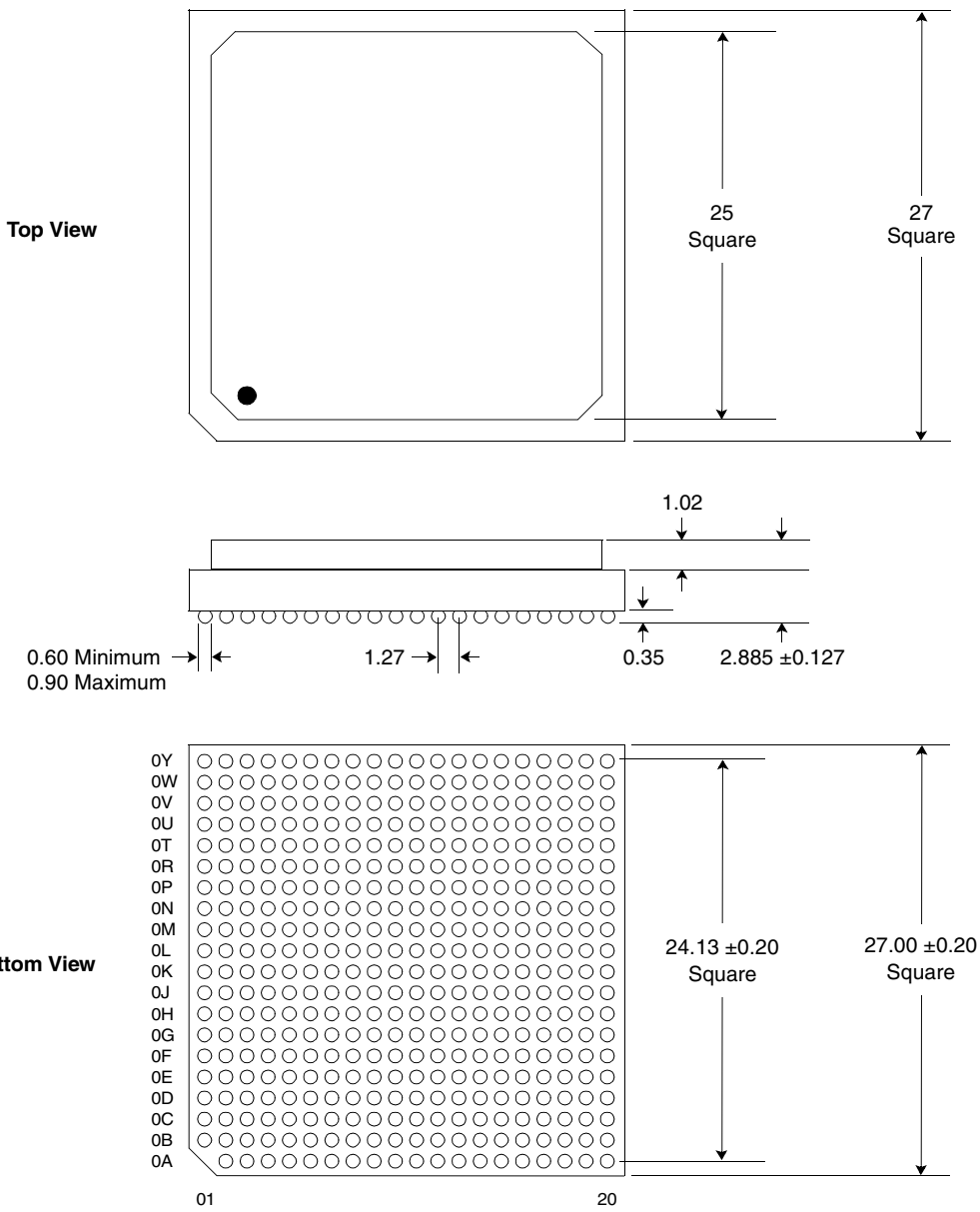
Table 3. Absolute Maximum Ratings

Symbol	Parameter	Rating			Units
		Minimum	Typical	Maximum	
P_{Max}	Power (activity factor = ~0.1)	3.8	4.5	5.2	W
V_{DD} (1.8 V)	Power supply voltage	1.65	1.8	1.95	V
V_{DD} (2.5 V)		2.3	2.5	2.7	V
I_{DD} (1.8 V)	Power supply current	2.0	2.3	2.7	A
I_{DD} (2.5 V)		95	110	125	mA
T_A	Operating junction temperature	0		100	°C
T_S	Storage temperature	-65		150	°C

Note: Permanent device damage may occur if the above absolute maximum ratings are exceeded. Extended exposure to absolute maximum rating conditions may affect device reliability.

Mechanical Information

Figure 4. Package Mechanical



Package type is 399-ball HyperBGA, package size is 27 × 27 mm, and array size is 20 × 20. All dimensions are in millimeters.

Note: This document contains information on products in the sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

Revision Log

Revision Date	Contents of Modification
Sept. 7, 2001	Initial release (00).

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IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6351

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