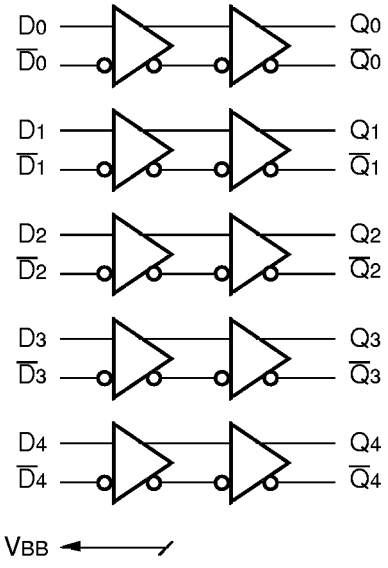
QUINT LVPECL-TO-PECL OR PECL-TO-LVPECL TRANSLATOR

FEATURES

- **3.3V and 5V power supplies required**
- **Also, supports LVPECL-to-PECL translation**
- **500ps propagation delays**
- **Fully differential design**
- **ESD protection of 2000V**
- **Available in 28-pin PLCC package**

BLOCK DIAGRAM



FUNCTION TABLE

Function	Vcc	Vcco	Vcc_VBB
PECL-to-LVPECL	5.0V	3.3V	5.0V
LVPECL-to-PECL	5.0V	5.0V	3.3V

PIN NAMES

Pin	Function
Dn	PECL / LVPECL Inputs
Qn	PECL / LVPECL Outputs
VBB	Reference Voltage Output
Vcco	Vcc for Outputs
Vcc_VBB	Vcc for VBB Output
GND	Common Ground Rail
Vcc	Vcc for Internal Circuitry

DESCRIPTION

The SY100E417 is a quint LVPECL-to-PECL translator. It can also be used as a quint PECL-to-LVPECL translator. The device receives standard PECL signals and translates them to differential LVPECL output signals (or vice versa).

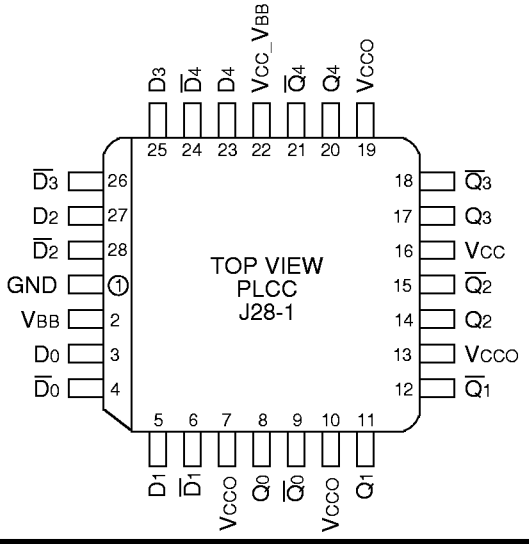
A VBB output is provided for interfacing single ended PECL signals at the inputs. If a single ended PECL input is to be used, the VBB output should be connected to the $\overline{Dn}$ input and the active signal will drive the Dn input. When used, the VBB should be bypassed to ground via a 0.01µF capacitor. The VBB is designed to act as a switching reference for the SY100E417 under single ended input conditions. As a result, the pin can only source/sink 0.5mA of current.

To accomplish the PECL-to-LVPECL level translation, the SY100E417 requires three power rails. The Vcc and Vcc_VBB supply is to be connected to the standard PECL supply, the LVCC supply is to be connected to the Vcco supply, and GND is connected to the system ground plane. Both the Vcc and Vcco should be bypassed to ground with a 0.01µF capacitor.

To accomplish the LVPECL-to-PECL level translation, the SY100E417 requires three power rails as well. The Vcc supply is connected to the Vcc and Vcco pins, LVCC supply is connected to the Vcc_VBB pin and GND is connected to the system ground plane. Vcc_VBB is used to provide a proper VBB output level if a single ended input is used. If inputs are differential signals, LVCC is still required and must be connected to Vcc_VBB to maintain proper functionality.

Under open input conditions, the $\overline{Dn}$ input will be biased at a Vcc/2 voltage level and the Dn input will be pulled to ground. This condition will force the "Qn" output low, ensuring stability.

PIN CONFIGURATION



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PECL INPUT DC ELECTRICAL CHARACTERISTICS

V_{CC_VBB} = V_{CC} = +4.5V to +5.5V; V_{CCO} = +3.0V to +3.8V

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Power Supply Voltage	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	V
V_{IH}	Input HIGH Voltage(1)	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	3.835	—	4.120	V
V_{IL}	Input LOW Voltage(1)	3.190	—	3.515	3.190	—	3.525	3.190	—	3.525	3.190	—	3.525	V
V_{PP}	Minimum Peak-to-Peak Input	150	—	—	150	—	—	150	—	—	150	—	—	mV
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current Dn $\overline{Dn}$	0.5 –600	— —	— —	0.5 –600	— —	— —	0.5 –600	— —	— —	0.5 –600	— —	— —	µA
V_{BB}	Output Reference(1)	3.620	—	3.740	3.620	—	3.740	3.620	—	3.740	3.620	—	3.740	V
I_{CC}	Power Supply Current	—	—	20	—	—	20	—	14	20	—	—	20	mA

NOTE:

1. These levels are for V_{CC_VBB} = 5.0V. Level specifications will vary 1:1 with V_{CC_VBB}.

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS

V_{CC_VBB} = V_{CC} = +4.5V to +5.5V; V_{CCO} = +3.0V to +3.8V

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CCO}	Power Supply Voltage	3.0	—	3.8	3.0	—	3.8	3.0	3.3	3.8	3.0	—	3.8	V
V_{OH}	Output HIGH Voltage(1)	2.215	—	2.420	2.275	—	2.420	2.275	2.350	2.420	2.275	—	2.420	V
V_{OL}	Output LOW Voltage(1)	1.470	—	1.745	1.490	—	1.680	1.490	1.600	1.680	1.490	—	1.680	V
I_{CCO}	Power Supply Current	—	—	35	—	—	35	—	23	35	—	—	37	mA

NOTE:

1. These levels are for V_{CCO} = 3.3V. Level specifications will vary 1:1 with V_{CCO}.

LVPECL INPUT DC ELECTRICAL CHARACTERISTICS

V_{CC_VBB} = +3.0V to +3.8V(1); V_{CC} = V_{CCO} = +4.5V to +5.5V

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CC}	Power Supply Voltage	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	V
V_{IH}	Input HIGH Voltage(2)	2.135	—	2.420	2.135	—	2.420	2.135	—	2.420	2.135	—	2.420	V
V_{IL}	Input LOW Voltage(2)	1.490	—	1.825	1.490	—	1.825	1.490	—	1.825	1.490	—	1.825	V
V_{PP}	Minimum Peak-to-Peak Input	150	—	—	150	—	—	150	—	—	150	—	—	mV
I_{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	—	—	150	µA
I_{IL}	Input LOW Current Dn $\overline{Dn}$	0.5 –600	— —	— —	0.5 –600	— —	— —	0.5 –600	— —	— —	0.5 –600	— —	— —	µA
V_{BB}	Output Reference(2)	1.92	—	2.04	1.92	—	2.04	1.92	—	2.04	1.92	—	2.04	V
I_{CC}	Power Supply Current	—	—	20	—	—	20	—	14	20	—	—	20	mA

NOTES:

1. V_{CC_VBB} = 3.3V is only required for single-ended LVPECL input. For differential LVPECL input, V_{CC_VBB} can be either 3.3V or 5V.
2. These levels are for V_{CC_VBB} = 3.3V. Level specifications will vary 1:1 with V_{CC_VBB}.

PECL OUTPUT DC ELECTRICAL CHARACTERISTICS

V_{CC}_V_{BB} = +3.0V to +3.8V; V_{CC} = V_{CCO} = +4.5V to +5.5V

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{CCO}	Power Supply Voltage	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	4.5	—	5.5	V
V_{OH}	Output HIGH Voltage(1)	3.915	—	4.120	3.975	—	4.120	3.975	—	4.120	3.975	—	4.120	V
V_{OL}	Output LOW Voltage(1)	3.170	—	3.445	3.190	—	3.380	3.190	—	3.380	3.190	—	3.380	V
I_{CCO}	Power Supply Current	—	—	35	—	—	35	—	23	35	—	—	37	mA

NOTES:

1. These levels are for V_{CCO} = 5.0V. Level specifications will vary 1:1 with V_{CCO}.

AC ELECTRICAL CHARACTERISTICS(1)

Symbol	Parameter	T_A = –40°C			T_A = 0°C			T_A = +25°C			T_A = +85°C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation Delay Diff.	490	590	690	510	610	710	510	610	710	530	630	730	ps
t_{PHL}	D to Q S.E.	440	590	740	460	610	760	460	610	760	480	630	780	
t_{skew}	Within-Device Skew													
	Output-to-Output(2)	—	20	100	—	20	100	—	20	100	—	20	100	ps
	Part-to-Part (Diff.)(2)	—	20	200	—	20	200	—	20	200	—	20	200	
	Duty Cycle (Diff.)(3)	—	25	—	—	25	—	—	25	—	—	25	—	
V_{PP}	Minimum Input Swing(4)	150	—	—	150	—	—	150	—	—	150	—	—	mV
V_{CMR}	Common Mode Range(5)													V
	V_{PP} < 500mV	1.3	—	V_{CC}–0.2	1.2	—	V_{CC}–0.2	1.2	—	V_{CC}–0.2	1.2	—	V_{CC}–0.2	
	V_{PP} ≥ 500mV	1.5	—	V_{CC}–0.2	1.4	—	V_{CC}–0.2	1.4	—	V_{CC}–0.2	1.4	—	V_{CC}–0.2	
t_r t_f	Output Rise/Fall Times Q (20% to 80%)	320	—	580	320	—	580	320	—	580	320	—	580	ps

NOTES:

1. Power supply requirements applies as indicated in the DC electrical characteristics tables.
2. Skew is measured between outputs under identical transitions.
3. Duty cycle skew is the difference between a TPLH and TPHL propagation delay through a device Common Mode Range.
4. Minimum input swing for which AC parameters are guaranteed. The device has a DC gain of ~40.
5. The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY100E417JC	J28-1	Commercial
SY100E417JCTR	J28-1	Commercial

Ordering Code	Package Type	Operating Range
SY100E417JI	J28-1	Industrial
SY100E417JITR	J28-1	Industrial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)