3.3V CMOS DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP-FLOP WITH CLEAR AND PRESET, 5 VOLT TOLERANT I/O

IDT74LVC112A

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 1.27mm pitch SOIC, 0.635mm pitch QSOP, 0.65mm pitch SSOP, 0.65mm pitch TSSOP packages
- Extended commercial range of – 40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range
- Vcc = 2.3V to 3.6V, Extended Range
- CMOS power levels (0.4µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- All inputs, outputs and I/O are 5 Volt tolerant
- Supports hot insertion

Drive Features for LVC112A:

- High Output Drivers: ±24mA
- Reduced system switching noise

APPLICATIONS:

- 5V and 3.3V mixed voltage systems
- Data communication and telecommunication systems

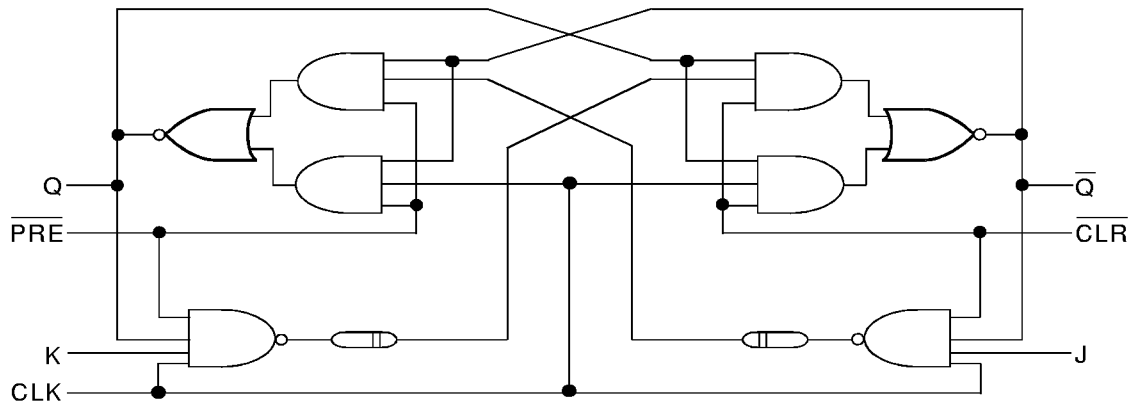
DESCRIPTION:

This dual negative-edge-triggered J-K flip-flop is built using advanced dual metal CMOS technology. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs, regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the J and K inputs meeting the setup time requirements is transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the J and K inputs can be changed without affecting the levels at the outputs. The LVC112A can perform as a toggle flip-flop by tying J and K high.

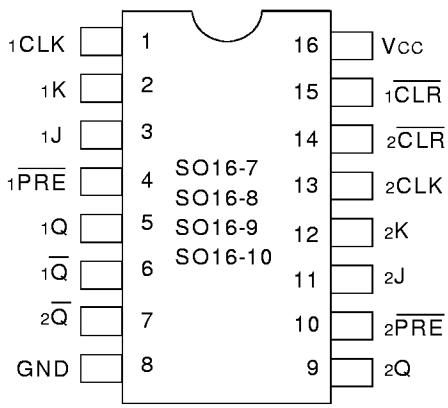
Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of this device as a translator in a mixed 3.3V/5V supply system.

The LVC112A has been designed with a ±24mA output driver. This driver is capable of driving a moderate to heavy load while maintaining speed performance.

Functional Block Diagram



PIN CONFIGURATION



QSOP/ SOIC/ SSOP/ TSSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
xCLK	CLK Inputs
$x\overline{CLR}$	Clear Inputs (Active LOW)
$x\overline{PRE}$	Preset Inputs (Active LOW)
xJ, xK	Data Inputs
xQ, $x\overline{Q}$	Data Outputs

FUNCTION TABLE (1)

Inputs					Outputs	
$x\overline{PRE}$	$x\overline{CLR}$	xCLK	xJ	xK	xQ	$x\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H(2)	H(2)
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Q_0 = Level of Q before the indicated steady-state input conditions were established.
   $\overline{Q}_0$ = Complement of Q_0 or level of $\overline{Q}$ before the indicated steady-state input conditions were established.
2. The output levels in this configuration may not meet the minimum levels for VOH. Furthermore, this configuration is unstable; that is, it does not persist when either $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
VTERM(2)	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
VTERM(3)	Terminal Voltage with Respect to GND	– 0.5 to +6.5	V
TSTG	Storage Temperature	– 65 to +150	°C
IOUT	DC Output Current	– 50 to +50	mA
IIK IOK	Continuous Clamp Current, VI < 0 or VO < 0	– 50	mA
ICC ISS	Continuous Current through each VCC or GND	±100	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VCC terminals.
3. All terminals except VCC.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF
CI/O	I/O Port Capacitance	VIN = 0V	6.5	8	pF

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NOTE:
1. As applicable to the device type.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = – 40°c to +85°c

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage Level	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IH} I_{IL}	Input Leakage Current	V_{CC} = 3.6V	V_I = 0 to 5.5V	—	—	±5	µA
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	V_{CC} = 3.6V	V_O = 0 to 5.5V	—	—	±10	µA
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_O ≤5.5V		—	—	±50	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = 2.3V, I_{IN} = – 18mA		—	– 0.7	– 1.2	V
V_H	Input Hysteresis	V_{CC} = 3.3V		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = 3.6V	V_{IN} = GND or V_{CC}	—	—	10	µA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at V_{CC} – 0.6V other inputs at V_{CC} or GND		—	—	500	µA

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NOTE:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient.

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = 2.3V to 3.6V	I_{OH} = – 0.1mA	V_{CC} – 0.2	—	V
		V_{CC} = 2.3V	I_{OH} = – 6mA	2	—	
		V_{CC} = 2.3V	I_{OH} = – 12mA	1.7	—	
		V_{CC} = 2.7V		2.2	—	
		V_{CC} = 3.0V		2.4	—	
		V_{CC} = 3.0V	I_{OH} = – 24mA	2.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.3V to 3.6V	I_{OL} = 0.1mA	—	0.2	V
		V_{CC} = 2.3V	I_{OL} = 6mA	—	0.4	
			I_{OL} = 12mA	—	0.7	
		V_{CC} = 2.7V	I_{OL} = 12mA	—	0.4	
		V_{CC} = 3.0V	I_{OL} = 24mA	—	0.55	

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NOTE:
1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = – 40°C to +85°C.

OPERATING CHARACTERISTICS, T_A = 25°C

Symbol	Parameter	Test Conditions	Vcc = 2.5V±0.2V	Vcc = 3.3V±0.3V	Unit
			Typical	Typical	
C_{PD}	Power Dissipation Capacitance per Flip-Flop	C_L = 0pF, f = 10Mhz	—	24	pF

SWITCHING CHARACTERISTICS (1)

Symbol	Parameter	Vcc = 2.5V±0.2V		Vcc = 2.7V		Vcc = 3.3V±0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{MAX}		—	—	150	—	150	—	MHz
t_{PLH} t_{PHL}	Propagation Delay x$\overline{CLR}$ or $\overline{PRE}$ to xQ or x$\overline{Q}$	—	—	—	5.5	1	4.8	ns
t_{PLH} t_{PHL}	Propagation Delay x$\overline{CLK}$ to xQ or x $\overline{Q}$	—	—	—	7.1	1	5.9	ns
t_{SU}	Setup Time, Data before CLK↓	—	—	2.3	—	3.1	—	ns
t_{SU}	Setup Time, $\overline{PRE}$ or $\overline{CLR}$ inactive	—	—	1.1	—	2.4	—	ns
t_H	Hold Time, data after CLK↓	—	—	0.7	—	2.5	—	ns
t_W	Pulse Width, CLK HIGH or LOW	—	—	3.3	—	3.3	—	ns
$t_{SK(0)}$	Output Skew(2)	—	—	—	—	—	500	ps

NOTES:
1. See test circuits and waveforms. T_A = – 40°C to + 85°C.
2. Skew between any two outputs of the same package and switching in the same direction.

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 2.5V ±0.2V	$V_{CC}^{(2)}$= 3.3V ±0.3V & 2.7V	Unit
V_{LOAD}	2 x Vcc	6	V
V_{IH}	Vcc	2.7	V
V_T	Vcc / 2	1.5	V
V_{LZ}	150	300	mV
V_{HZ}	150	300	mV
C_L	30	50	pF

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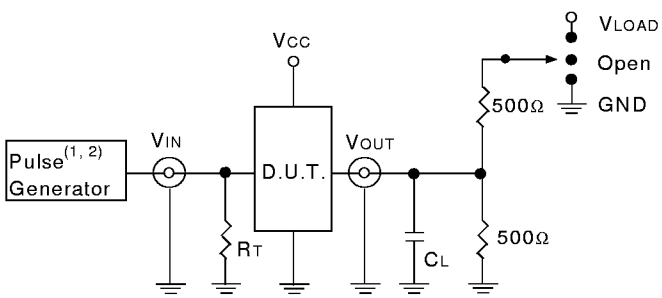
TEST CIRCUITS FOR ALL OUTPUTS



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DEFINITIONS:

C_L= Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V_{LOAD}
Disable High Enable High	GND
All Other tests	Open

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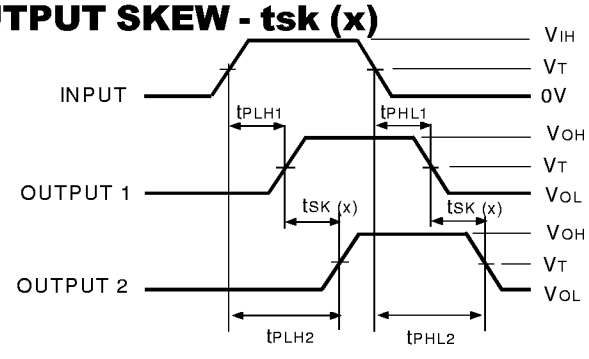
OUTPUT SKEW - tsk (x)



$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

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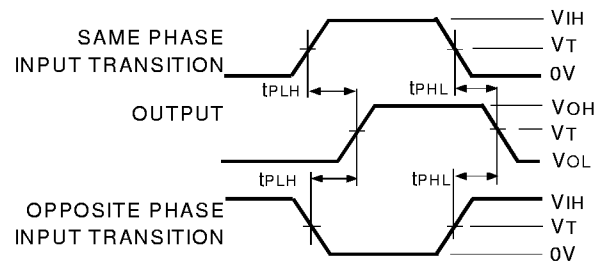
NOTES:

1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



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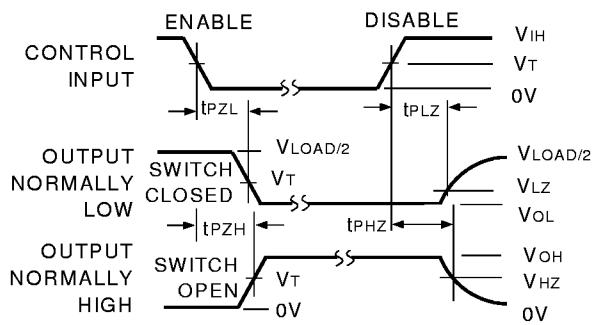
ENABLE AND DISABLE TIMES



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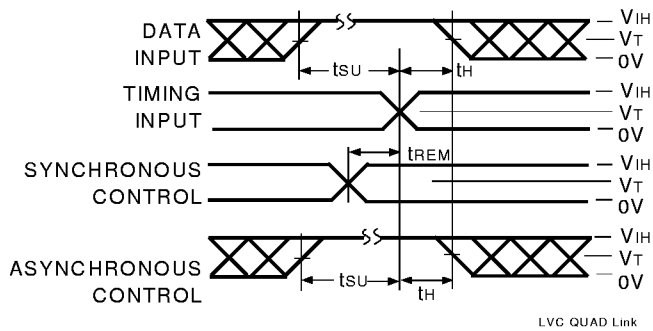
NOTE:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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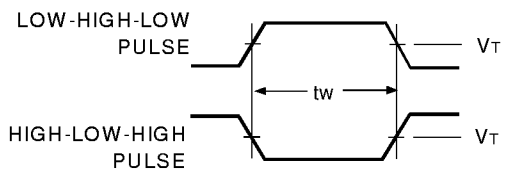
PULSE WIDTH



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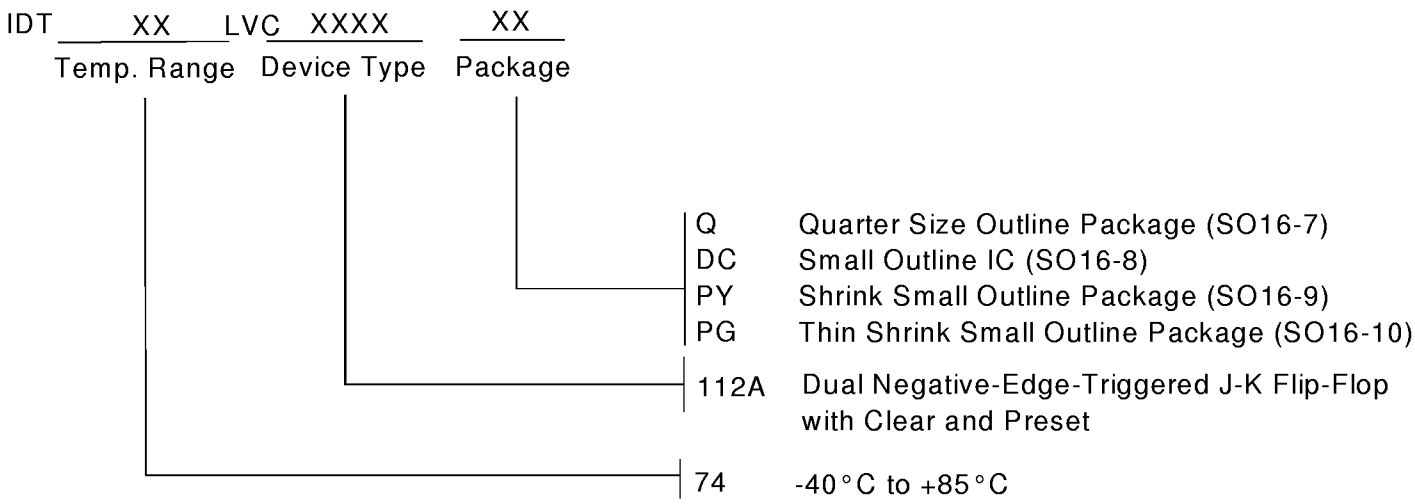
ORDERING INFORMATION



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