VTC Inc.
Value the Customer™

VM313H

14-CHANNEL, HIGH-PERFORMANCE, THIN-FILM HEAD, READ/WRITE PREAMPLIFIER

950801

FEATURES

- High Performance:
  - Read Mode Gain = 250V/V
  - Low Input Noise = $0.8nV/\sqrt{Hz}$ Maximum
  - Input Capacitance = 25pF Maximum
  - Write Current Range = 10mA to 40mA
  - Head Inductance Range = 200nH to 3µH
  - Head Voltage Swing = 7Vp-p Minimum
  - Write Current Rise Time = 5ns
- Low Power Dissipation
- Enhanced System Write-to-Read Recovery Time
- Power Supply Fault Protection
- Schottky Isolated Damping Resistor Standard
- Write Unsafe Detection
- +5V and +12V Power Supply Requirement
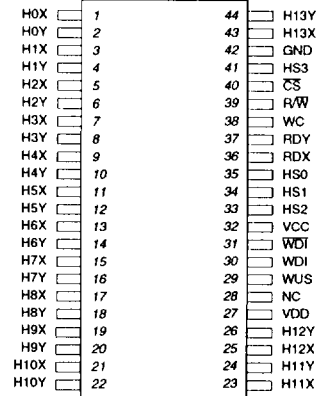- Differential Pseudo ECL Write Data Input

DESCRIPTION

The VM313H is a high-performance, low-power, high gain, bipolar monolithic read / write preamplifier designed for use with two-terminal thin-film recording heads. It provides write current control, data protection circuitry and a low-noise read preamplifier for fourteen channels. When unselected, the device enters a sleep mode, with power dissipation reduced to less than 180mW. Fault protection is provided so that during power supply sequencing the write current generator is disabled. System write-to-read recovery time is minimized by maintaining the read channel common-mode output voltage in the write mode. The VM313H features a read mode voltage gain of 250V/V.
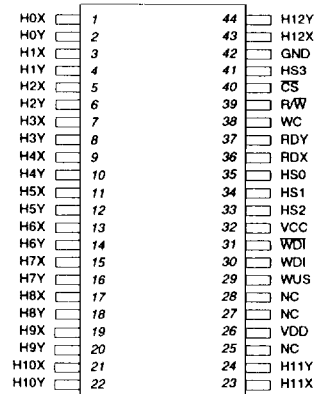
Very low power dissipation from +5V and +12V supplies is achieved through use of high-speed bipolar processing and innovative circuit design techniques. A 400Ω damping resistor is included on-chip in series with a Schottky diode pair to maintain high input resistance in the read mode.

The VM313H is available in a variety of package configurations. Please consult VTC for package availability.
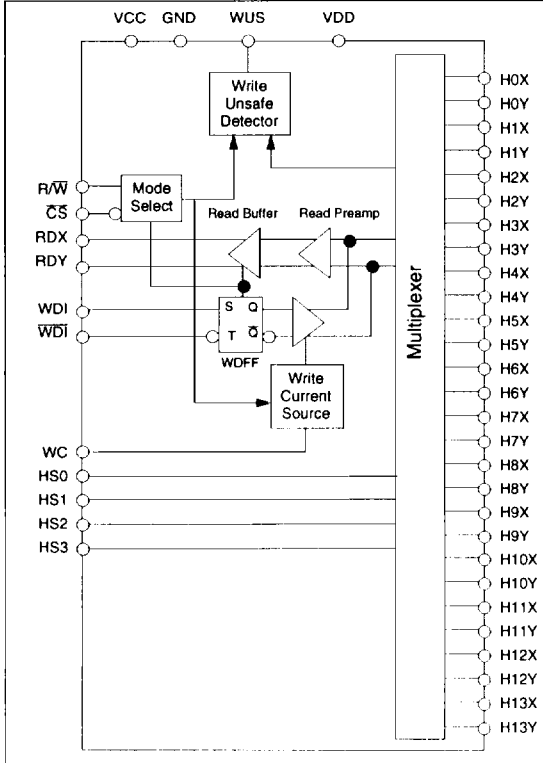
CONNECTION DIAGRAMS

Pin		Pin	
H0X	1	44	H13Y
H0Y	2	43	H13X
H1X	3	42	GND
H1Y	4	41	HS3
H2X	5	40	$\overline{CS}$
H2Y	6	39	R/$\overline{W}$
H3X	7	38	WC
H3Y	8	37	RDY
H4X	9	36	RDX
H4Y	10	35	HS0
H5X	11	34	HS1
H5Y	12	33	HS2
H6X	13	32	VCC
H6Y	14	31	$\overline{WDI}$
H7X	15	30	WDI
H7Y	16	29	WUS
H8X	17	28	NC
H8Y	18	27	VDD
H9X	19	26	H12Y
H9Y	20	25	H12X
H10X	21	24	H11Y
H10Y	22	23	H11X

**14-Channel
44-lead SOIC**

Pin		Pin	
H0X	1	44	H12Y
H0Y	2	43	H12X
H1X	3	42	GND
H1Y	4	41	HS3
H2X	5	40	$\overline{CS}$
H2Y	6	39	R/$\overline{W}$
H3X	7	38	WC
H3Y	8	37	RDY
H4X	9	36	RDX
H4Y	10	35	HS0
H5X	11	34	HS1
H5Y	12	33	HS2
H6X	13	32	VCC
H6Y	14	31	$\overline{WDI}$
H7X	15	30	WDI
H7Y	16	29	WUS
H8X	17	28	NC
H8Y	18	27	NC
H9X	19	26	VDD
H9Y	20	25	NC
H10X	21	24	H11Y
H10Y	22	23	H11X

**13-Channel
44-lead SOIC**

BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages:

V_{DD} .... -0.3V to +14V

V_{CC} .... -0.3V to +7V

Write Current (I_W) 100mA

Input Voltages:

Digital Input Voltage V_{IN} .... -0.3V to (V_{CC} + 0.3)V

Head Port Voltage V_H .... -0.3V to (V_{CC} + 0.3)V

WUS Pin Voltage Range V_{WUS} .... -0.3V to +14V

Output Current:

RDX, RDY: I_O .... -10mA

WUS: I_{WUS} .... +12mA

Junction Temperature, ... 150°C

Storage Temperature Range .... -65° to 150°C

Thermal Characteristics, Θ_{JA}:

44-lead SOIC .... 70°C/W

RECOMMENDED OPERATING CONDITIONS

DC Power Supply Voltage:

V_{DD} .... 12V ± 10%

V_{CC} .... 5V ± 10%

Junction Temperature .... 0°C to 125°C

CIRCUIT OPERATION

The VM313H addresses fourteen two-terminal thin film heads, providing write drive or read amplification. Head selection and mode control are accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 and 2. Internal resistor pullups provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

Write Mode

Write mode configures the VM313H as a current switch and activates the write unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high-to-low transition on pins WDI - $\overline{WDI}$ (differential write data inputs).

A preceding read operation initializes the write data flip-flop (WDFF) so that upon entering the write mode current flows into the "X" head port.

The write current magnitude is determined by an external resistor connected between the WC pin and ground. An internally generated 1.71V reference voltage is present at the WC pin. The magnitude of the write current (0-pk, ± 8%) is:

$$I_W = 1.65 \ V/R_{WC}$$

Typically, an adjustment to the calculated head current is required to account for current shunted by the damping resistor. This complication is avoided in the VM313H because the internal damping resistors are series-connected with Schottky diode pairs.

In multiple-device applications, a single R_{WC} resistor may be made common to all devices.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, may be required to clear the WUS flag.

- No write current
- WDI frequency too low
- Open head
- Device in read mode
- Device not selected

Read Mode

Read mode configures the VM313H as a low-noise high gain differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common-mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the recovery time delay to the subsequent Pulse Detection circuitry.

Idle Mode

When $\overline{CS}$ is high, virtually the entire circuit is shut down so that power dissipation is reduced to less than 180 mW for a *sleep mode*.

Table 11: Mode Select

R/W	CS	MODE
0	0	Write
1	0	Read
X	1	Idle

Table 12: Head Select

HS0	HS1	HS2	HS3	HEAD
0	0	0	0	0
1	0	0	0	1
0	1	0	0	2
1	1	0	0	3
0	0	1	0	4
1	0	1	0	5
0	1	1	0	6
1	1	1	0	7
0	0	0	1	8
1	0	0	1	9
0	1	0	1	10
1	1	0	1	11
0	0	1	1	12
1	0	1	1	13

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
HS0 - HS3	I*	Head Select: selects one of up to 14 heads
H0X - H13X H0Y - H13Y	I/O	X, Y Head Terminals
WDI, WDI	I*	Write Data Input: A negative transition (WDI - WDI) toggles direction of head current.
CS	I	Chip select: low level enables the device
R/W	I*	Read/Write select: high level selects read moden
WUS	O*	Write Unsafe: open collector output, high level indicates writes unsafe condition
WC		Write Current: a resistor adjusts level of write current
RDX, RDY	O*	Read Data Output: differential output data
VCC		+5 volt logic circuit supply
VDD		+12 volt supply
GND		Ground

* When more than one R/W device is used, these signals can be wire OR'ed.

TYPICAL APPLICATION
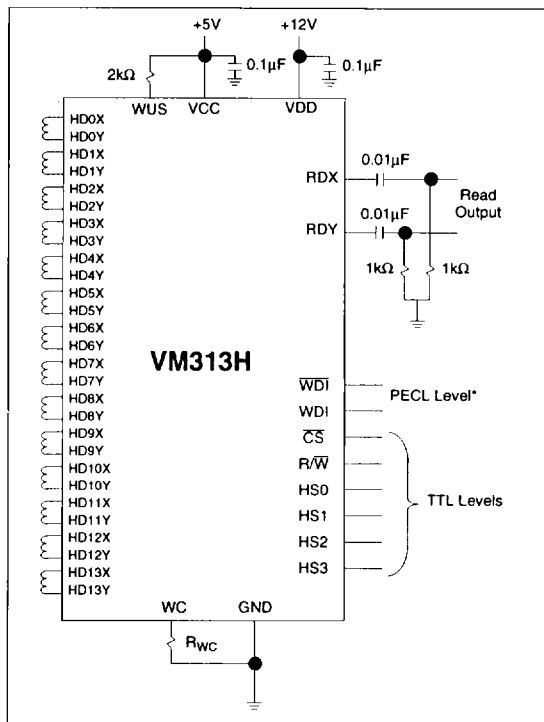
* For proper operation in read or write mode the WDI/WDI inputs must be correctly biased to their respective PECL levels. They cannot float of both be tied high or low.

VM313H

DC CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
VCC Supply Current	I_{CC}	Read Mode			47	mA
		Write Mode			27	
		Idle Mode			4	
VDD Supply Current	I_{DD}	Read Mode			31	mA
		Write Mode			$30 + I_W$	
		Idle Mode			12	
Power Dissipation ($T_J = 125°C$)	P_D	Read Mode		500	670	mW
		Write Mode: $I_W = 20mA$		625	800	
		Idle Mode		105	180	
Input Low Voltage	V_{IL}	TTL			0.8	V
Input High Voltage	V_{IH}	TTL	2.0			V
Input Low Current	I_{IL}	$V_{IL} = 0.8V$, TTL	-0.4			mA
Input High Current	I_{IH}	$V_{IH} = 2.0V$, TTL			100	μA
WDI, $\overline{WDI}$ Input High Voltage	V_{IH}	Pseudo ECL	$V_{CC} - 1.0$		$V_{CC} - 0.7$	V
WDI, $\overline{WDI}$ Input Low Voltage	V_{IL}	Pseudo ECL	$V_{CC} - 1.9$		$V_{CC} - 1.6$	V
WDI, $\overline{WDI}$ Input High Current	I_{IH}	$V_{IH} = V_{CC} - 0.7V$			100	μA
WDI, $\overline{WDI}$ Input Low Current	I_{IL}	$V_{IL} = V_{CC} - 1.6V$			80	μA
WUS Output Low Voltage	V_{OL}	$I_{OL} = 8mA$			0.5	V
VCC Fault Voltage	V_{DDF}		9.0		10.5	V
VCC Fault Voltage	V_{CCF}		3.5		4.3	V
Head Current (HnX, HnY)	I_H	Write Mode, $0 < V_{CC} \leq 3.5V$, $0 < V_{DD} < 9V$	-200		+200	μA
		Write Mode, $0 < V_{CC} < 5.5V$, $0 < V_{DD} < 13.2V$	-200		+200	

READ CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, C_L (RDX, RDY) < 20pF and R_L (RDX, RDY) = 1kΩ.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Voltage Gain	A_V	V_{IN} = 1mVp-p @300kHz	210	250	290	V/V
Bandwidth	BW	-1dB, lZsl < 5Ω, V_{IN} = 1mVp-p @300kHz	25			MHz
		-3dB, lZsl < 5Ω, V_{IN} = 1mVp-p @300kHz	45			
Input Noise Voltage	e_{in}	BW = 15MHz, L_H = 0, R_H = 0		0.65	0.8	nV/√Hz
Differential Input Capacitance	C_{IN}	V_{IN} = 1mVp-p, f = 5MHz		17	26	pF
Differential Input Resistance	R_{IN}	V_{IN} = 1mVp-p, f = 5MHz, (25°C < T_A < 125°C)	500	1000		Ω
Dynamic Range	DR	AC input voltage where the gain falls to 90% of the gain @ 0.2mVrms input, f = 5MHz	2			mVrms
Common Mode Rejection Ratio	CMRR	V_{CM} = 100mVp-p @5MHz	54			dB
Power Supply Rejection Ratio	PSRR	100mVp-p @5MHz on V_{DD} or V_{CC}	54			dB
Channel Separation	CS	Unselected channels driven with 100mVp-p @5MHz, Selected Channels V_{IN} = 0mVp-p	45			dB
Output Offset Voltage	V_{OS}		-250		+250	mV
RDX, RDY Common Mode Output Voltage	V_{OCM}	Read Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	V
		Write Mode	V_{CC} - 2.8	V_{CC} - 2.3	V_{CC} - 2.0	
Single-Ended Output Resistance	R_{SEO}	f = 5MHz			30	Ω
Output Current	I_O	AC coupled load, RDX to RDY	3.2			mA

WRITE CHARACTERISTICS Unless otherwise specified, recommended operating conditions apply, I_W = 20mA, L_H = 1.0µH, R_H = 30Ω and f_{DATA} = 5MHz.

PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
WC Pin Voltage	V_{WC}			1.65		V
Write Current Voltage	V_{DH}	I_{WC} = 40mA	7			Vp-p
Unselected Head Current	I_{UH}				1.0	mA (pk)
Differential Output Capacitance	C_{OUT}				25	pF
Differential Output Resistance	R_{OUT}		3.2			kΩ
WDI Transition Frequency	f_{DATA}	WUS = low	1.7			MHz
Write Current Range	I_W	41.25Ω < R_{WC} < 165Ω	10		40	mA
Write Current Tolerance	ΔI_W	I_W range 10mA to 40mA	-8		+8	%

SWITCHING CHARACTERISTICS (see Figure 1) Unless otherwise specified, recommended operating conditions apply, $I_W = 20mA$, $L_H = 1.0\mu H$, $R_H = 30\Omega$ and $f_{DATA} = 5MHz$.

| PARAMETER	SYM	CONDITIONS	MIN	TYP	MAX	UNITS
R/W̄ to Write Mode	t_{RW}	Delay to 90% of write current			0.6	µs
R/W̄ to Read Mode	t_{WR}	Delay to 90% of 100mV, 10MHz read signal envelope or to 90% decay of write current			0.6	µs
C̄S̄ to Select	t_{IR}	Delay to 90% of write current or to 90% of 100mV, 10MHz read signal envelope			0.6	µs
C̄S̄ to Unselect	t_{IW}	Delay to 10% of write current			0.6	µs
HS0 - HS3 to Any Head	t_{HS}	Delay to 90% of 100mV, 10MHz read signal envelope			0.4	µs
Safe to Unsafe	t_{D1}	50% WDI to 50% WUS	0.6		3.6	µs
Unsafe to Safe	t_{D2}	50% WDI to 50% WUS			1	µs
Propagation Delay	t_{D3}	From 50% points, $L_H = 0$, $R_H = 0$			32	ns
Asymmetry	A_{SYM}	WDI has 50% duty cycle and 1ns rise/fall time, $L_H = 0$, $R_H = 0$			0.5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, $I_W = 20mA$, $L_H = 0$, $R_H = 0$			5	ns
Rise/Fall Time	t_r/t_f	10% - 90% points, $I_W = 20mA$, $L_H = 600nH$, $R_H = 20\Omega$			9	ns
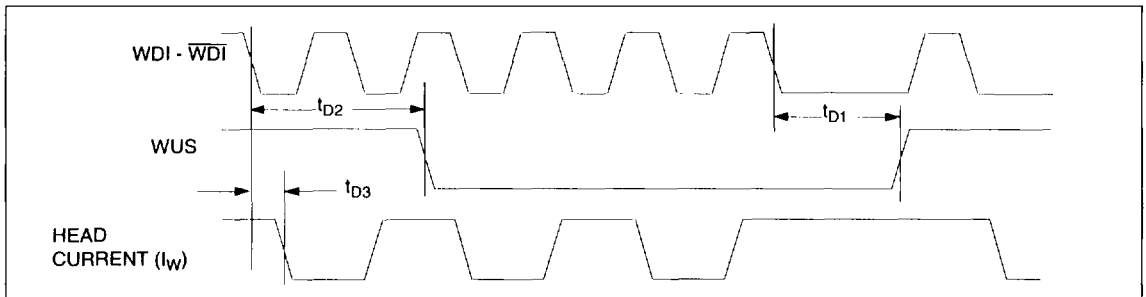
Figure 1: Write Mode Timing Diagram