M02061

3.3 or 5 Volt Laser Driver IC for Applications to 4.25 Gbps

The M02061 is a highly integrated, programmable laser driver intended for SFP/SFF module with data rates up to 4.25 Gbps. Using differential PECL data inputs, the M02061 supplies the bias and modulation current required to drive an edge-emitting laser. The modulation output can be DC-coupled to the laser diode.

The M02061 includes automatic power control to maintain a constant average laser output power over temperature and life. In addition, the modulation current can be temperature compensated to minimize variation in extinction ratio over temperature.

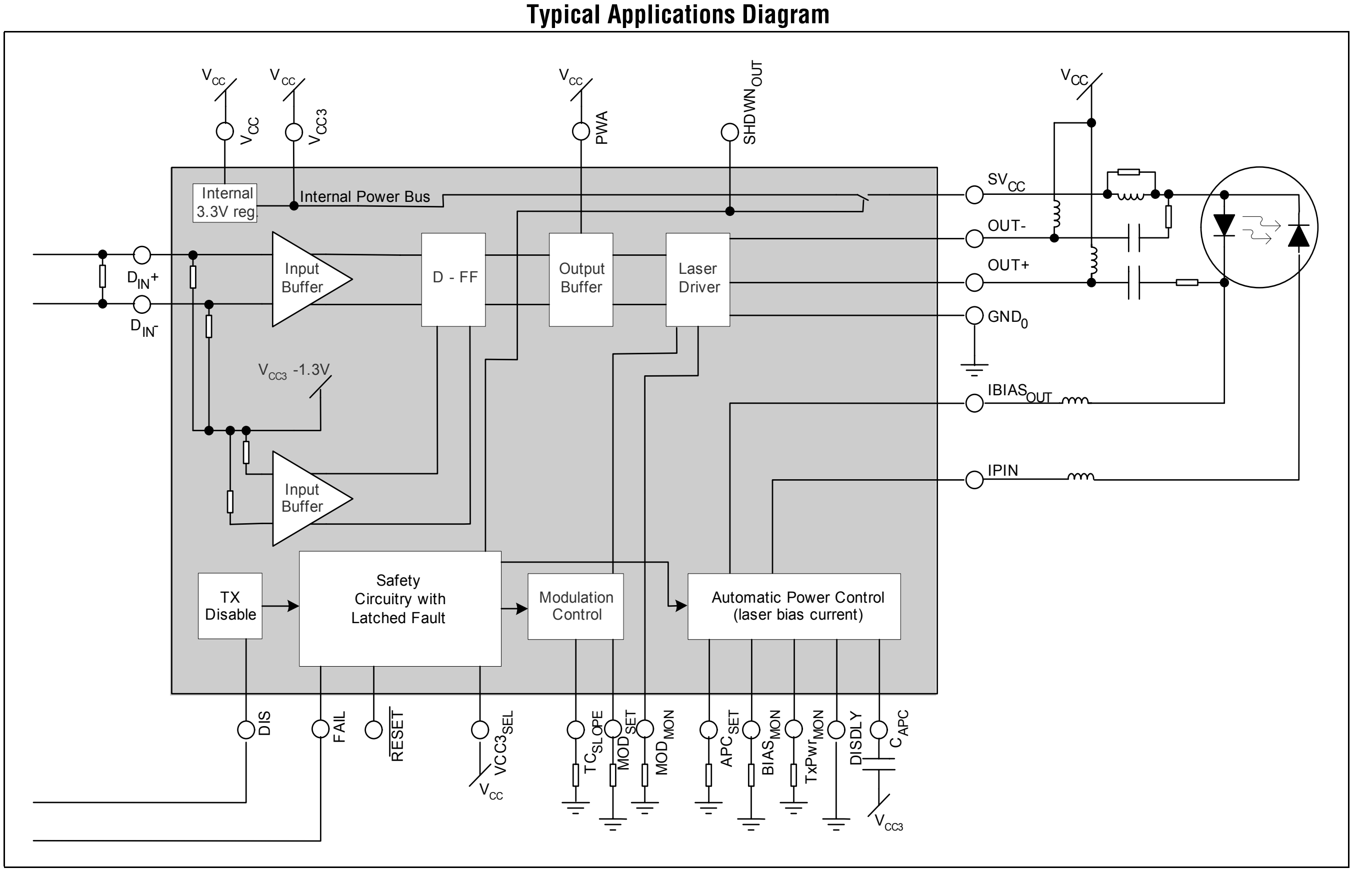
Applications

- SFP and SFF Modules
- 1G/2G/4G Fibre Channel modules
- Short reach and Metro SONET/SDH

Features

- High speed operation; suitable for SFP/SFF applications from 155Mbps to 4.25 Gbps. Typical rise/fall times of 55 ps.
- Programmable temperature compensation. Modulation output and bias output can be controlled using a few discrete resistors.
- Supports DDMI (SFF-8472) diagnostics.
- DC or AC coupled modulation drive. Up to 100mA modulation current available when AC coupled.
- Low overshoot allows high extinction ratio with low jitter.
- Automatic Laser Power Control, with “Slow-Start”.
- PECL and CML compatible differential data inputs.
- Complies with major MSAs (GBIC, SFF, SFF-8472, SFP) including timing requirements
- Packaged in a QFN24
- 3.3V or 5V operation
- Pulsewidth adjustment

Typical Applications Diagram



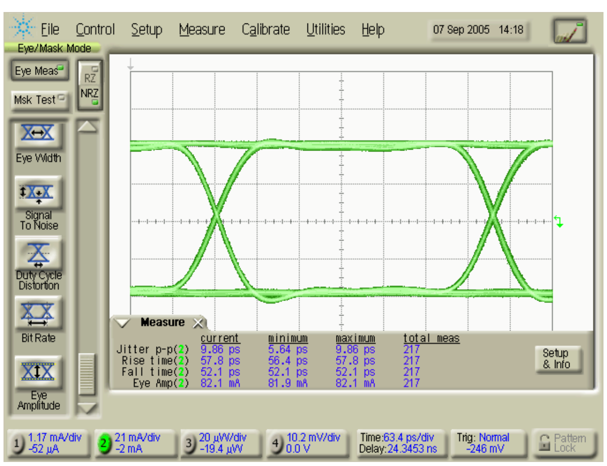
Ordering Information

Part Number	Package	Operating Temperature
M02061-11	QFN24	–40 °C to 95 °C
M02061-EVM	Combination Optical and Electrical Evaluation board	–40 °C to 95 °C
*This part is available in a variety of RoHS compliant packages.		

Revision History

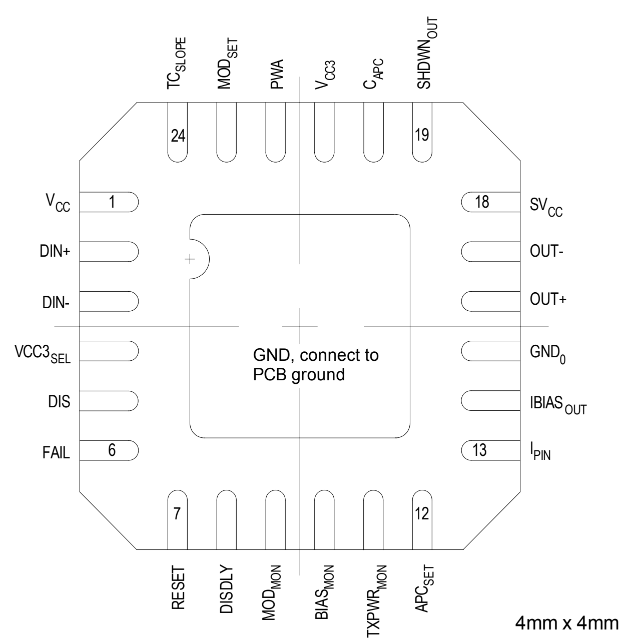
Revision	Level	Date	ASIC Revision	Description
D	Release	September 2005	x	New format. Remove 32 pin package information. Changes to Absolute Maximum Specifications - operating temperature, output voltage. Changes to Recommended Operating Conditions - VCC, operating temperature. Changes to DC Characteristics - ICC, VMD, TxPWRmon, logic inputs and outputs, data inputs, safety logic thresholds. Changes to AC Characteristics - IMOD, Tr, Tf, jitter.
C	Preliminary	March 2004	x	Added eye diagram,; corrected rise/fall times.
B	Advance	January 2004	x	B Version. Changed maximum bandwidth to 4.25 Gbps.
A	Advance	October 2003	x	Advance Information

2.5Gbps Electrical Eye Diagram



Conditions: 80mA modulation current, 2^7-1 PRBS

QFN24 Pin Configuration



1.0 Product Specification

1.1 Absolute Maximum Ratings

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage	-0.4 to +6.0	V
V_{CC3}	3.3V power supply voltage	-0.4 to +4.0	V
T_A	Operating ambient temperature	-40 to +95	°C
T_{STG}	Storage temperature	-65 to +150	°C
$I_{BIASOUT\ (MAX)}$	Maximum bias output current	150	mA
$I_{MOD\ (MAX)}$	Maximum modulation current	140	mA
D_{IN}+/-, CLK+/-	Data and clock inputs	0 to V_{CC3} + 0.4	V
CEN, DIS, $VCC3_{SEL}$	Mode control inputs	-0.4 to V_{CC} + 0.4	V
$BIAS_{MON}$, MOD_{MON}	Bias and modulation output current mirror compliance voltage	-0.4 to V_{CC3} + 0.4	V
IPIN	Photodiode anode voltage	-0.4 to V_{CC3} + 0.4	V
IPIN	Photodiode current	2	mA
FAIL	Status flags	-0.4 to V_{CC} + 0.4	V
PWA, APC_{SET}, MOD_{SET}	Set inputs	-0.4 to V_{CC3} + 0.4	V
TC_{START}	Temperature compensation start temperature	-0.4 to 1.0	V
TC_{SLOPE}	Temperature compensation slope	-0.4 to V_{CC3} + 0.4	V
OUT+, OUT-	Output	-0.4 to V_{CC} + 0.4	V

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Parameter	Rating	Units
Power supply (V_{CC}-GND)	3.3 ± 7.5% or 5.0 + 8%,-5%	V
Operating ambient	-40 to + 95	°C

1.3 DC Characteristics

(V_{CC} = +3.05V to +3.55V or 4.75V to 5.4V, T_A = -40 °C to +95 °C, unless otherwise noted)
Typical values are at V_{CC} = 3.3 V, $I_{BIASOUT}$ = 30 mA, I_{MOD} = 30 mA, T_A = 25 °C, unless otherwise noted.

Table 1-3. DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CC}	Supply current excluding I_{MOD} and I_{BIAS}	PWA high (no pulsewidth adjust) additional current when PWA used additional current when operating from a 5V supply	– - -	35 1.5 1.5	61 - -	mA
I_{BIAS}	Bias current adjust range	$V(I_{BIASOUT})$ > 0.7V For 3.3V operation with an AC coupled laser For 5.0V operation with a DC coupled laser.	1 1		100 60	mA
$I_{BIAS(OFF)}$	Bias current with optical output disabled	DIS = high $V(I_{BIASOUT}) > V_{CC}$ - 1V	–	–	300	µA
	Ratio of I_{BIAS} current to $BIAS_{MON}$ current		–	100	–	A/A
V_{MD}	Monitor diode reverse bias voltage	V_{CC} =3.3V	1.5	–	–	V
I_{MD}	Monitor diode current adjustment range	Adjusted with R_{APCSET}	10	–	1500	µA
	Ratio of $TxPwr_{MON}$ current to monitor photodiode current		0.95	1	1.25	A/A
C_{MD_MAX}	Maximum monitor photodiode capacitance for APC loop stability. Includes all associated parasitic capacitances.				100	pF

Table 1-3. DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	TTL/CMOS input high voltage (DIS)		2.0	–	5.4	V
	TTL/CMOS input low voltage (DIS)		–	–	0.8	V
	CMOS input high voltage ($VCC3_{SEL}$, MON_{POL})			2.4		V
	CMOS input low voltage ($VCC3_{SEL}$, MON_{POL})			1.2		V
	Logic output high voltage (FAIL)	With external 10kΩ pull-up to V_{CC}.	V_{CC} - 0.5	–	–	V
	Logic output low voltage (FAIL)	For 6.8k to 10k Ω resistor when pulled up to 5V. For 4.7k to 10k Ω resistor when pulled up to 3.3V.	–	–	0.4	V
R_{IN}	Differential input impedance	Data inputs	–	6800	–	Ω
V_{SELF}	Self-biased common-mode input voltage		–	V_{CC3} - 1.3	–	V
V_{INCM}	Common-mode input compliance voltage	Data inputs	V_{CC3} - 1.45	–	V_{CC3}-[$V_{IN(Diff)}$]/4	V
$V_{IN(DIFF)}$	Differential input voltage	= 2 x ($D_{IN}+_{HIGH}$ - $D_{IN}+_{LOW}$) (clock inputs follow same relationship)	200	–	2400	mVpp
V_{CC3THL}(1)	3.3V supply detection, lower threshold		2.5	2.8	3.0	V
V_{CC3THH}(1)	3.3V supply detection, upper threshold		3.65	3.9	4.25	V
V_{CC5THL}	5V supply detection, lower threshold		3.9	4.25	4.65	V
V_{CC5THH}	5V supply detection, upper threshold		5.4	5.8	6.1	V
V_{REF1}	Reference voltage for MOD_{SET}		1.18	1.3	1.4	V
V_{APCSET}	Reference voltage for APC_{SET}			1.3		V
V_{BL}	Bias_OK lower voltage threshold		0.88	1.0	1.05	V

Table 1-3. DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{BH}	Bias_OK upper voltage threshold		1.45	1.6	1.7	V
V_{FAULTL}	Lower voltage threshold for fault inputs $I_{BIASOUT}$, OUT+, C_{APC}, AND MOD_{SET}	FAIL asserts if any of these signals fall below this value.		300	400	mV
V_{OUT_DIS}	Self bias voltage for $I_{BIASOUT}$ and OUT+	DIS = high	0.5	1.65	2.2	V
V_{SHDWNL}	$SHDWN_{OUT}$ output low voltage	DIS = low, $I_{SHDWNOUT} \leq 100uA$			V_{CC} - 4	V
V_{SHDWNH}	$SHDWN_{OUT}$ output high voltage	DIS = low, $I_{SHDWNOUT} \leq 10uA$	V_{CC} - 0.3V			V

Notes: 1. When V_{CC} = 5V, V_{CC3} “supply OK” circuitry monitors the internally regulated 3.3V supply. When V_{CC} = 3.3V, V_{CC3} “supply OK” circuitry monitors V_{CC}.

1.4 AC Characteristics

(V_{CC} = 3.05 V to 3.55V or 4.75V to 5.4V, T_A = -40 °C to +95 °C, unless otherwise noted)
Typical values are at V_{CC} = 3.3 V, $I_{BIASOUT}$ = 30 mA, I_{MOD} = 30 mA, 25 ohm load and T_A = 25 °C, unless otherwise noted.

Table 1-4. AC Characteristics (2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units.
I_{MOD}	Modulation current range	3.3V operation, AC coupled, OUT+ and OUT- ≥1.6V 5V operation, DC coupled(1) into a 25Ω load to VCC - 1.2V. OUT+ and OUT- ≥1.15V	10 10	–	100 80	mA
$I_{MOD(OFF)}$	Modulation current with output disabled	DIS = high	–	–	300	µA
	Ratio of modulation current to MOD_{MON} current		–	100	–	A/A
I_{MOD-TC}	Programmable range for modulation current temperature coefficient	Adjustable using TC_{SLOPE} (2)	0	–	10^4	ppm/°C
tr	Modulation output rise time	20% to 80% into 25 Ω. Measured using 11110000 pattern at 2.5Gbps	–	55	75	ps
tf	Modulation output fall time		–	55	75	ps
OS	Overshoot of modulation output current in the off direction.	into 25 Ω load	--	1	–	%
RJ	Random jitter		–	0.8	–	ps_{rms}
DJ	Deterministic jitter	Measured into 25Ω load, 2^{31} - 1 PRBS at 2.7 Gbps K28.5 pattern at 4.25 Gbps (includes pulse width distortion(3))		10 10	25 30	ps_{pp}

Notes:
1. Guaranteed by design and characterization.
2. DC coupled operation at 3.3V is not supported. AC coupled operation at 5V is possible provided the outputs never exceed 6V.
3. Pulse width distortion is measured single-ended.

1.5 Safety Logic Timing

(V_{CC} = 3.05 V to 3.55V or 4.7V to 5.4V, T_A = -40 °C to +95 °C, unless otherwise noted)

Table 1-5. Safety Logic Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units.
t_off	DIS assert time	Rising edge of DIS to fall of output signal below 10% of nominal(1)			10	µs
t_on	DIS negate time	Falling edge of DIS to rise of output signal above 90% of nominal(1)			1	ms
t_init	Time to initialize(2)	Includes reset of FAIL; from power on after Supply_OK or from negation of DIS during reset of FAIL condition	2	3	5	ms
t_fault	Laser fault time - from fault condition to assertion of FAIL	From occurrence of fault condition or when Supply_OK is beyond specified range			100	µs
t_reset	DIS time to start reset	DIS pulse width required to initialize safety circuitry or reset a latched fault			10(3)	µs
t_{VCC_OK}	Supply_OK delay time	Delay between Supply_OK condition and when outputs are enabled	10	20		µs
t_on_{BM}	DIS negate (turn-on) time during burst-mode operation	I_{MOD} > 20mA; outputs DC coupled (5V operation)(4)		300	500	ns
t_off_{BM}	DIS assert (turn-off) time during burst-mode operation	I_{MOD} > 20mA; outputs DC coupled (5V operation)		200	500	ns

Notes:
1. With CAPC ≤ 2.2nF
2. User-adjustable. Specifications reflect timing with no external RESET capacitor.
3. With ≤ 1nF capacitor from RESET pin to ground.
4. Imod >12mA

Figure 1-6. Relationship between Data and Clock Inputs and Modulation Outputs

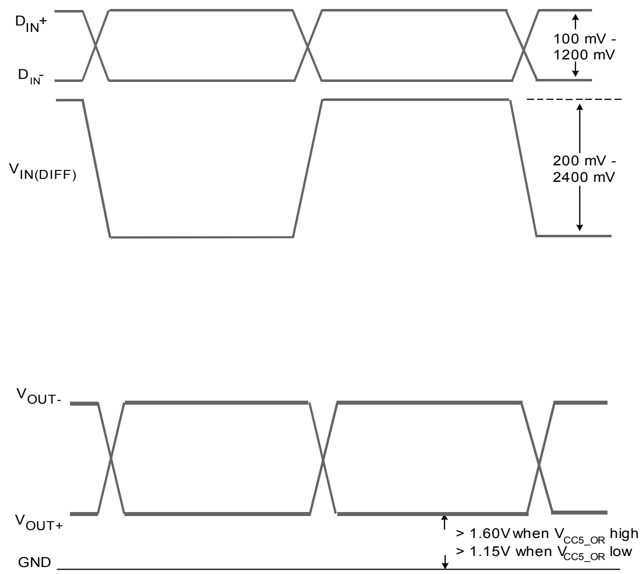
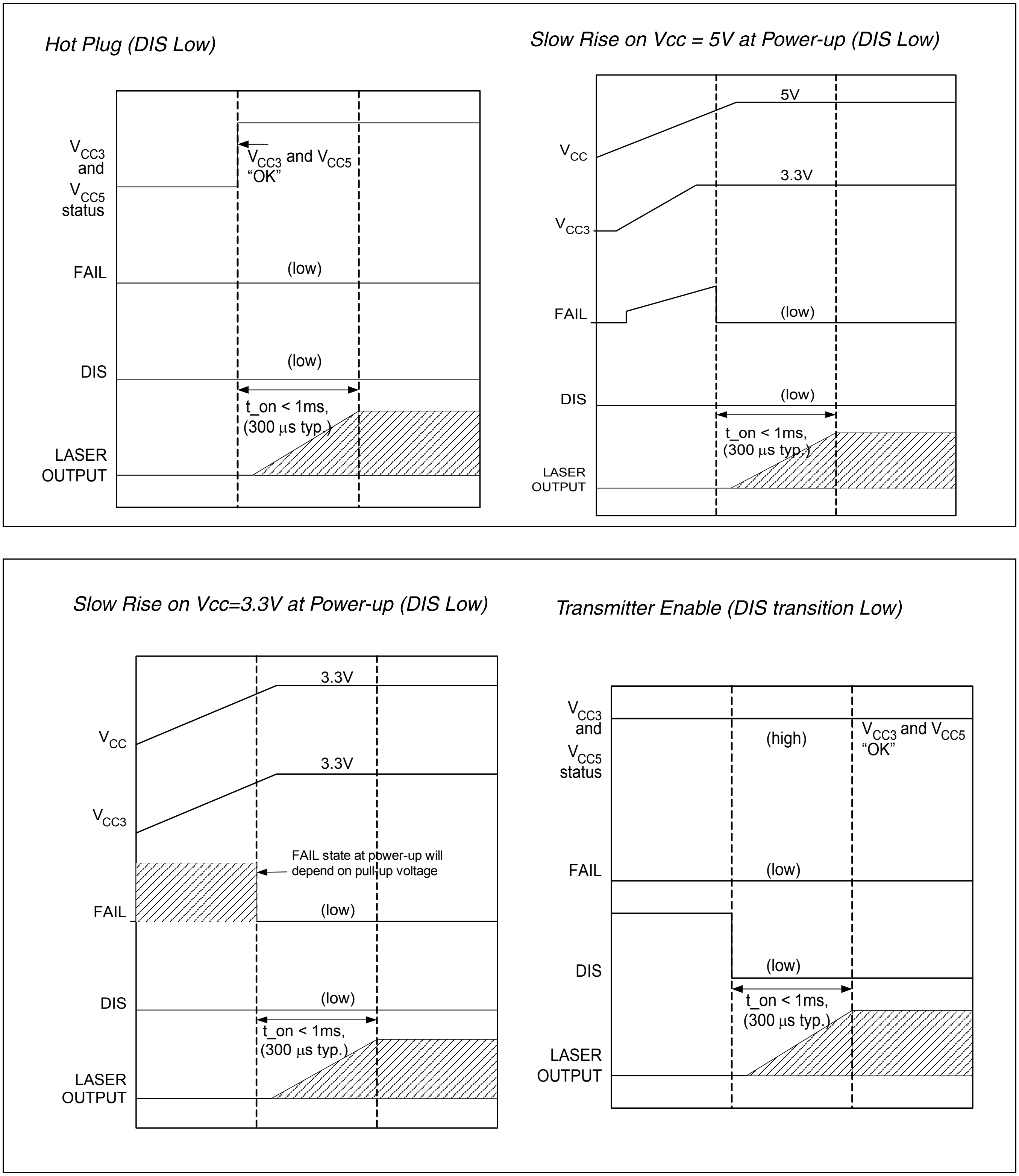
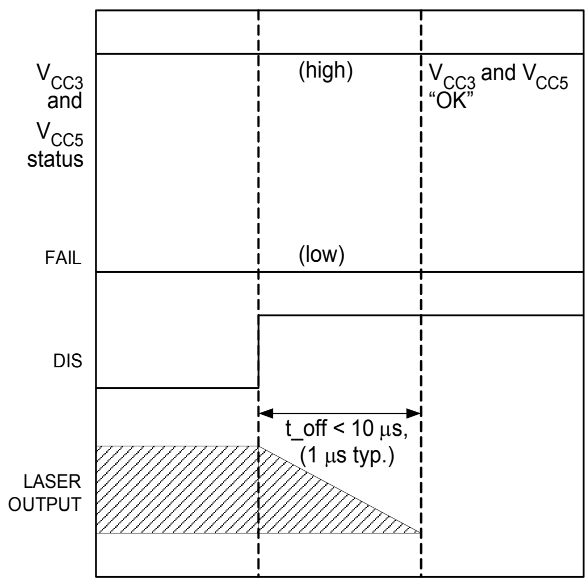


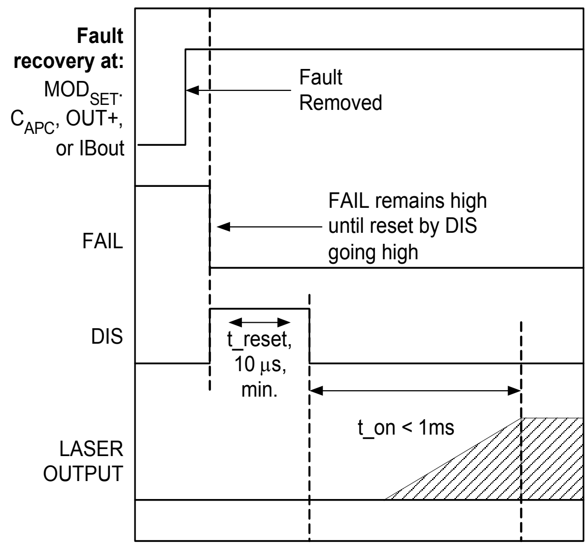
Figure 1-7. Safety Logic Timing Characteristics



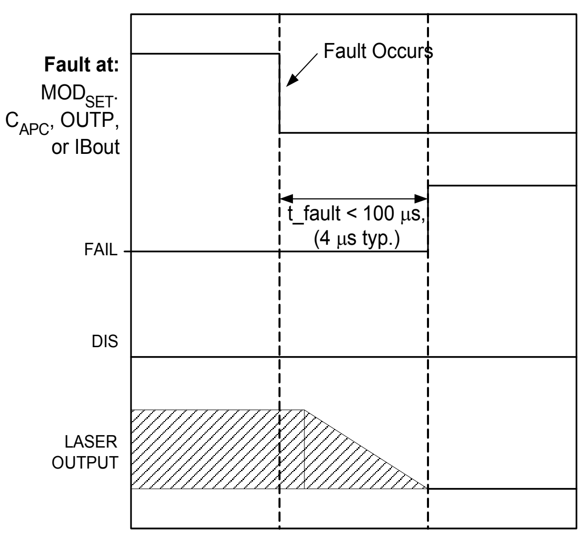
Transmitter Disable (DIS transition high)



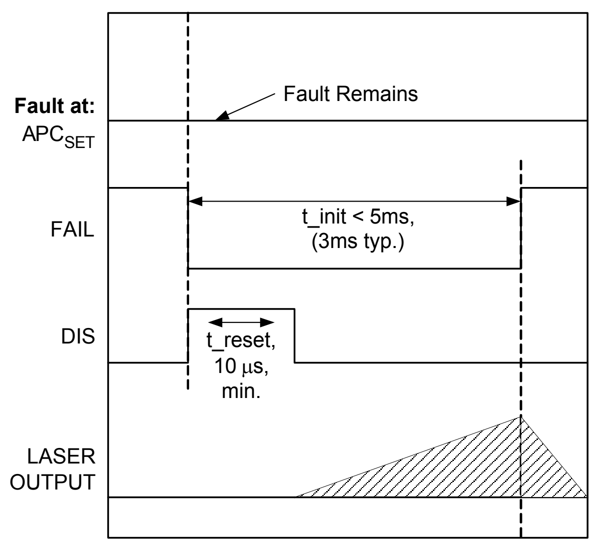
Fault Recovery Behaviour



Response to Fault



Unsuccessful Fault Reset Attempt



2.0 Pin Definitions

Table 2-1 lists pin type definitions and descriptions for the M02061 device.

Table 2-1. M02061 Pin Definitions and Descriptions

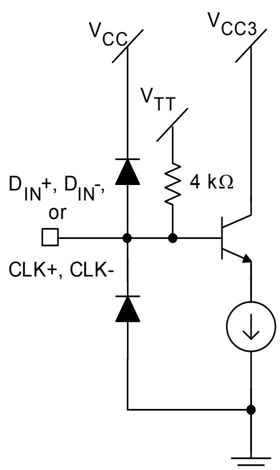
4x4 mm QFN24 Pin Number	Pin Name	Pin equivalent load	Function
1	V_{CC}		Power supply
2	D_{IN}+		Positive data input. Self biased. Compatible with AC coupled PECL, AC coupled CML, and DC-coupled PECL (V_{CC} = 3.3V). When D_{IN}+ is high, OUT+ sinks current.
3	D_{IN}-	See D_{IN}+ drawing	Negative data input. Self biased Compatible with AC coupled PECL, AC coupled CML, and DC-coupled PECL (V_{CC} = 3.3V).

Table 2-1. M02061 Pin Definitions and Descriptions

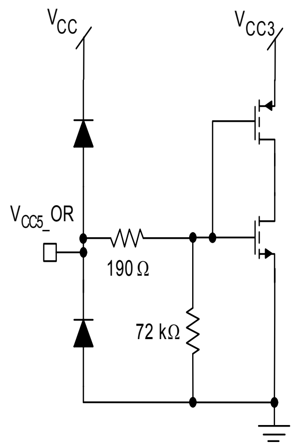
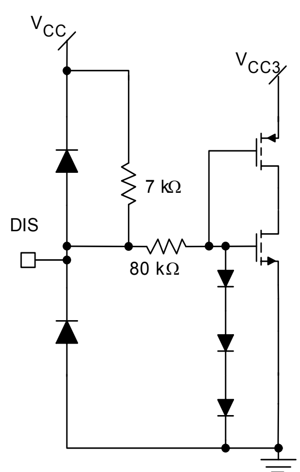
4x4 mm QFN24 Pin Number	Pin Name	Pin equivalent load	Function
4	$VCC3_{SEL}$		3.3V V_{CC} Select. Connect to V_{CC3} for V_{CC} = 3.3V operation. Connect to GND for V_{CC} = 5V operation.
5	DIS		Bias and modulation output disable (TTL/CMOS).

Table 2-1. M02061 Pin Definitions and Descriptions

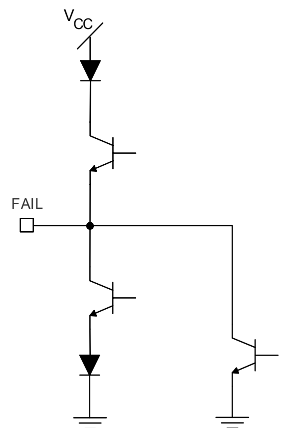
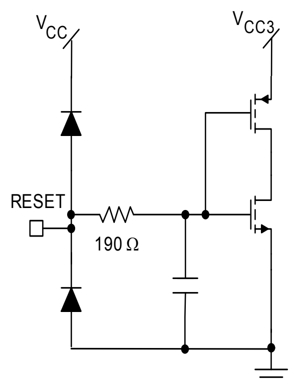
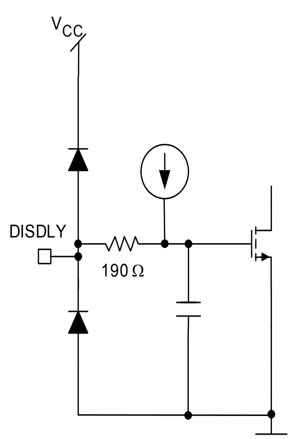
4x4 mm QFN24 Pin Number	Pin Name	Pin equivalent load	Function
6	FAIL		Safety circuit control failure output (TTL/CMOS). Goes high when a safety logic fault is detected. This output will be low when DIS is high.
7	RESET		Safety circuit reset. Leave open for normal operation or add a capacitor to ground to extend the reset time. Connect to GND to disable window comparators at APC_{SET}
8	DISDLY		Disable delay control. Connect to ground for normal operation. In burst mode operation add a capacitor from this pin to ground to set the maximum disable time. Disable times greater than this maximum will engage the “slow-start” circuitry.

Table 2-1. M02061 Pin Definitions and Descriptions

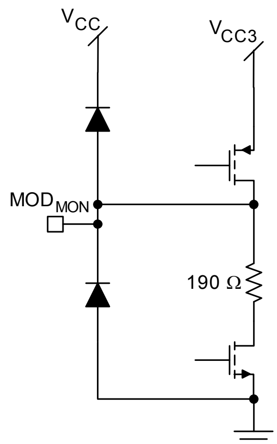
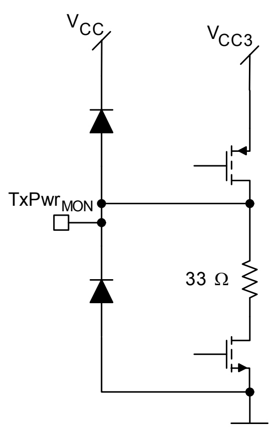
4x4 mm QFN24 Pin Number	Pin Name	Pin equivalent load	Function
9	MOD_{MON}		Modulation Current Monitor. Connect directly through a resistor to GND (MON_{POL} high) or to V_{CC3} (MON_{POL} low). The current through this pin is approximately 1/100th of the MODULATION current to the laser This pin may be left open if the feature is not needed and the M02061 current consumption will be reduced by 0.5mA typically.
10	$BIAS_{MON}$	See MOD_{MON} drawing	Bias Current Monitor. Connect directly through a resistor to GND (MON_{POL} high) or to V_{CC3} (MON_{POL} low). The current through this pin is approximately 1/100th of the BIAS current to the laser. This pin may be left open if the feature is not needed and the M02061 current consumption will be reduced by 0.5mA typically.
11	$TxPwr_{MON}$		Transmit Power Monitor. Connect directly through a resistor to GND (MON_{POL} high) or to V_{CC3} (MON_{POL} low). The current through this pin is approximately the same as the photodiode current into IPIN. This pin may be left open if the feature is not needed and the M02061 current consumption will be reduced by the IPIN current.

Table 2-1. M02061 Pin Definitions and Descriptions

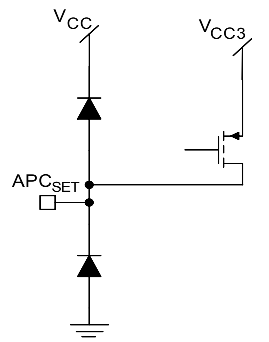
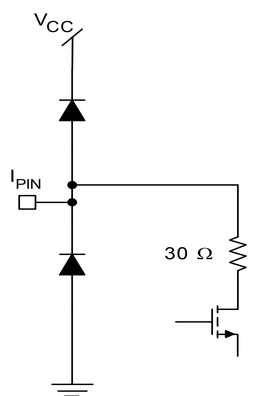
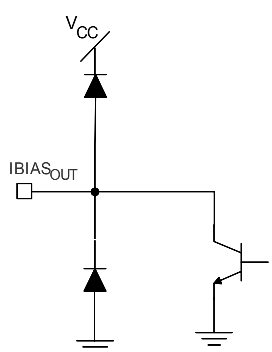
4x4 mm QFN24 Pin Number	Pin Name	Pin equivalent load	Function
12	APC_{SET}		Average Power Control, laser bias current adjustment. Connect a resistor between this pin and ground to set the bias current to the laser. The APC loop will control the laser bias current to maintain a voltage of approximately 1.3V at this pin. The current through this pin is approximately the same as the current into I_{PIN}.
13	I_{PIN}		Current input from monitor photodiode anode. The APC loop will adjust the laser bias current to maintain a voltage at APC_{SET} of approximately 1.3V and at this pin of approximately one V_{GS}. The voltage at this pin will not exceed 1.6V in normal operation
14	$IBIAS_{OUT}$		Laser bias current output. Connect directly to laser cathode or at higher bit rates through a ferrite or a resistor to isolate the capacitance of this pin from the modulation drive, (~2pF). Maintain a voltage $\geq$ 0.7V at this pin.

Table 2-1. M02061 Pin Definitions and Descriptions

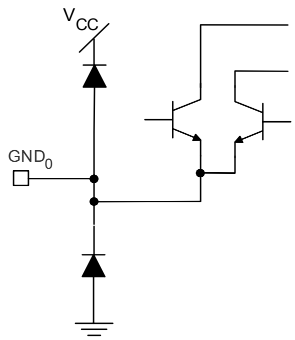
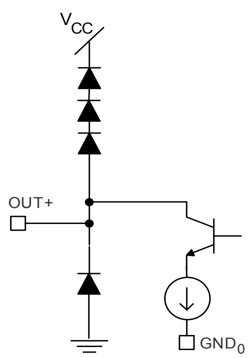
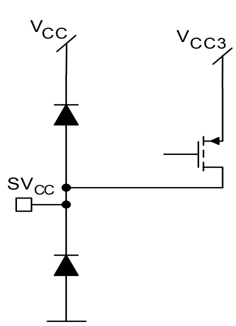
4x4 mm QFN24 Pin Number	Pin Name	Pin equivalent load	Function
15	GND_O		Ground for output stage. May be connected directly to ground. At high bit rates (>2Gb/s) an optional inductor or ferrite may be added to reduce switching transients.
16	OUT+		Positive modulation current output. Sinks current when D_{IN}+ is HIGH. Maintain a voltage $\geq$ 1.6V at this pin when $VCC3_{SEL}$ is high. Maintain a voltage $\geq$ 1.15V at this pin when $VCC3_{SEL}$ is low.
17	OUT-	See OUT+ drawing	Negative modulation current output. Sinks current when D_{IN}- is HIGH Maintain a voltage $\geq$ 1.6V at this pin when $VCC3_{SEL}$ is high. Maintain a voltage $\geq$ 1.15V at this pin when $VCC3_{SEL}$ is low.
18	SV_{CC}		Switched V_{CC}. 3.3V applications - Connect to laser anode. Safety circuitry will open the switch when a fault is detected and no current will flow through the laser. No capacitance is needed on this node. If capacitance to ground is added, do not exceed 100pF. 5V applications - Disabled, leave open.

Table 2-1. M02061 Pin Definitions and Descriptions

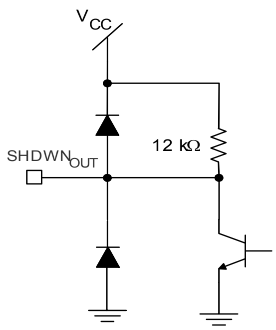
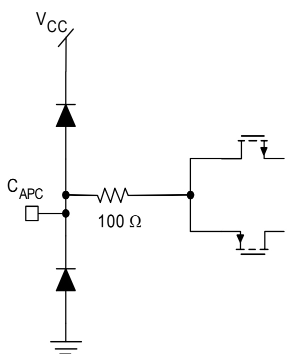
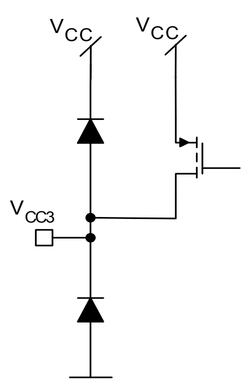
4x4 mm QFN24 Pin Number	Pin Name	Pin equivalent load	Function
19	$SHDWN_{OUT}$		External switched V_{CC} control signal. Use in 5V applications to create an external SV_{CC}.
20	C_{APC}		Automatic power control loop dominant pole capacitor. (Connect a capacitor between this pin and V_{CC3}.) A 2.2nF capacitor will give less than 1ms enable time and a loop bandwidth < 30kHz
21	V_{CC3}		3.3V applications - Power supply input. Connect to V_{CC}. 5V applications - Internally generated 3.3V. Power supply output. Do not attach to non-M02061 circuitry.

Table 2-1. M02061 Pin Definitions and Descriptions

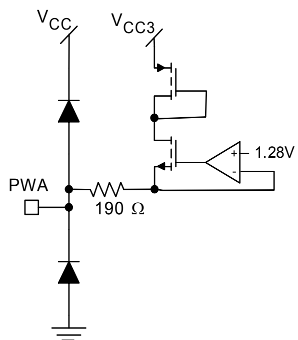
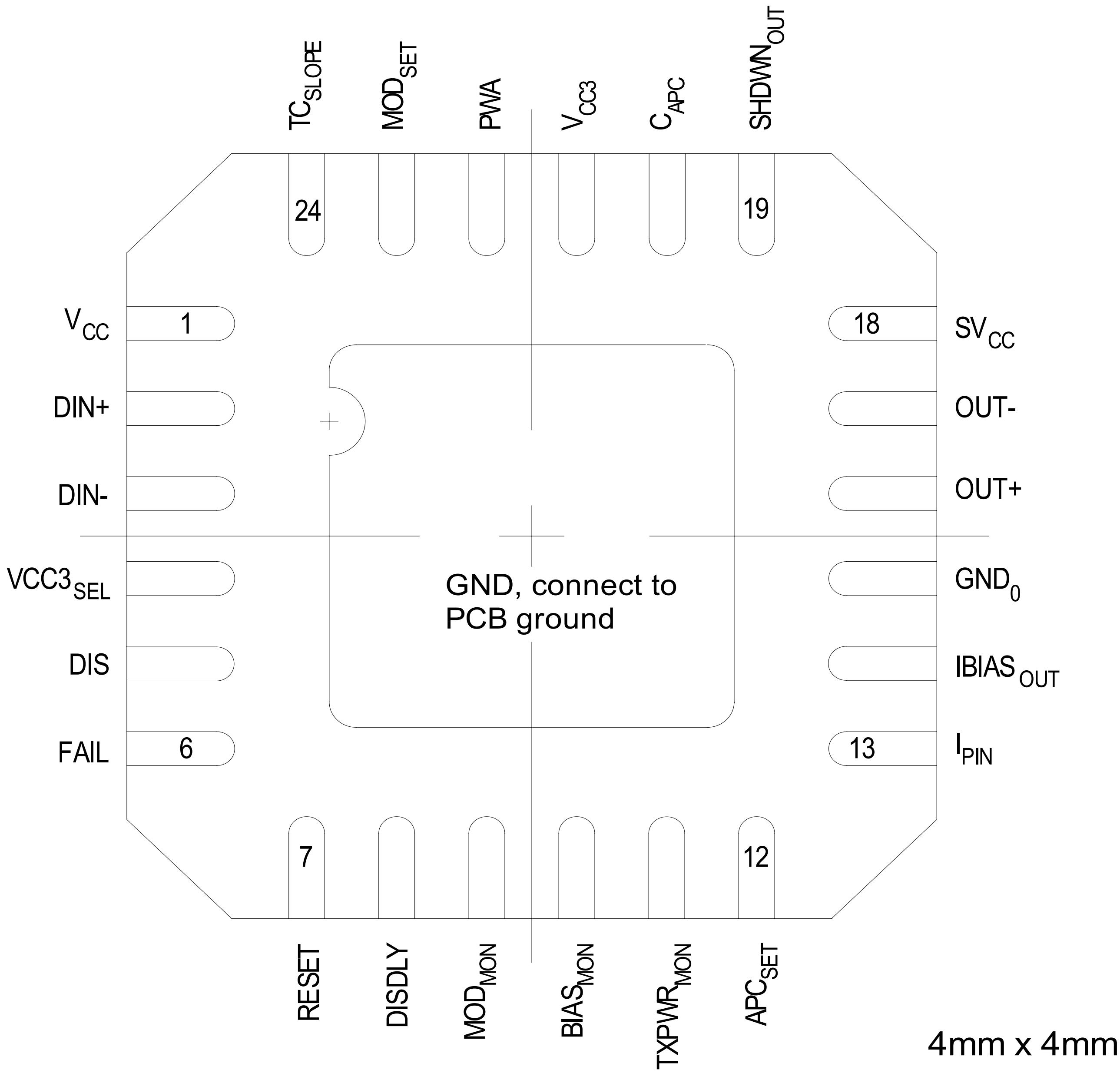
4x4 mm QFN24 Pin Number	Pin Name	Pin equivalent load	Function
22	PWA		Pulse Width Adjust. Connect a resistor to GND to enable, (between 1kΩ and 20kΩ). Connect to V_{CC3} to disable.
23	MOD_{SET}	See PWA drawing	Modulation current control. Connect a resistor to ground to set the modulation current.
24	TC_{SLOPE}	See PWA drawing	Modulation current temperature compensation coefficient adjustment. Connect a resistor to ground to set the temperature compensation coefficient. Leave open to disable the temperature compensation. A 51kΩ resistor will result in a temperature compensation slope of approximately 0.5%/°C
CENTER PAD	GND		Connect to GND.

Figure 2-1. QFN24 Pinout Information



3.0 Functional Description

3.1 Overview

The M02061 is a highly integrated, programmable laser driver intended for SFP/SFF module with data rates up to 4.25 Gbps. Using differential PECL data inputs, the M02061 supplies the bias and modulation current required to drive an edge-emitting laser.

Monitor outputs and internal safety logic in the M02061 combined with the M02088 will support designs requiring DDMI compliance.

The M02061 includes automatic power control to maintain a constant average laser output power over temperature and life. In addition, the modulation current can be temperature compensated to minimize variation in extinction ratio over temperature.

Many features are user-adjustable, including the APC (automatic power control) loop bias control (via a monitor photodiode), modulation current, temperature compensation control of modulation current, and pulse-width adjustment. The part may be operated from a 3.3V or 5V supply.

The driver modulation output can be AC, DC, or Differentially coupled to the laser.

For E-PON and other burst-mode applications, the part supports fast and accurate turn-on and turn-off of the laser bias and modulation currents.

Safety circuitry is also included to provide a latched shut-down of laser bias and modulation current if a fault condition occurs. An internal V_{CC} switch provides redundant shutdown when operating the device from a 3.3V supply. Control is provided to allow for a redundant external switch when operating with a 5V supply, if desired.

To minimize pattern-dependent jitter of the input signal, the device accepts an input clock signal for data retiming.

Figure 3-1 details the functional blocks and pin signals for the M02061 device.

Figure 3-1. M02061 Block Diagram

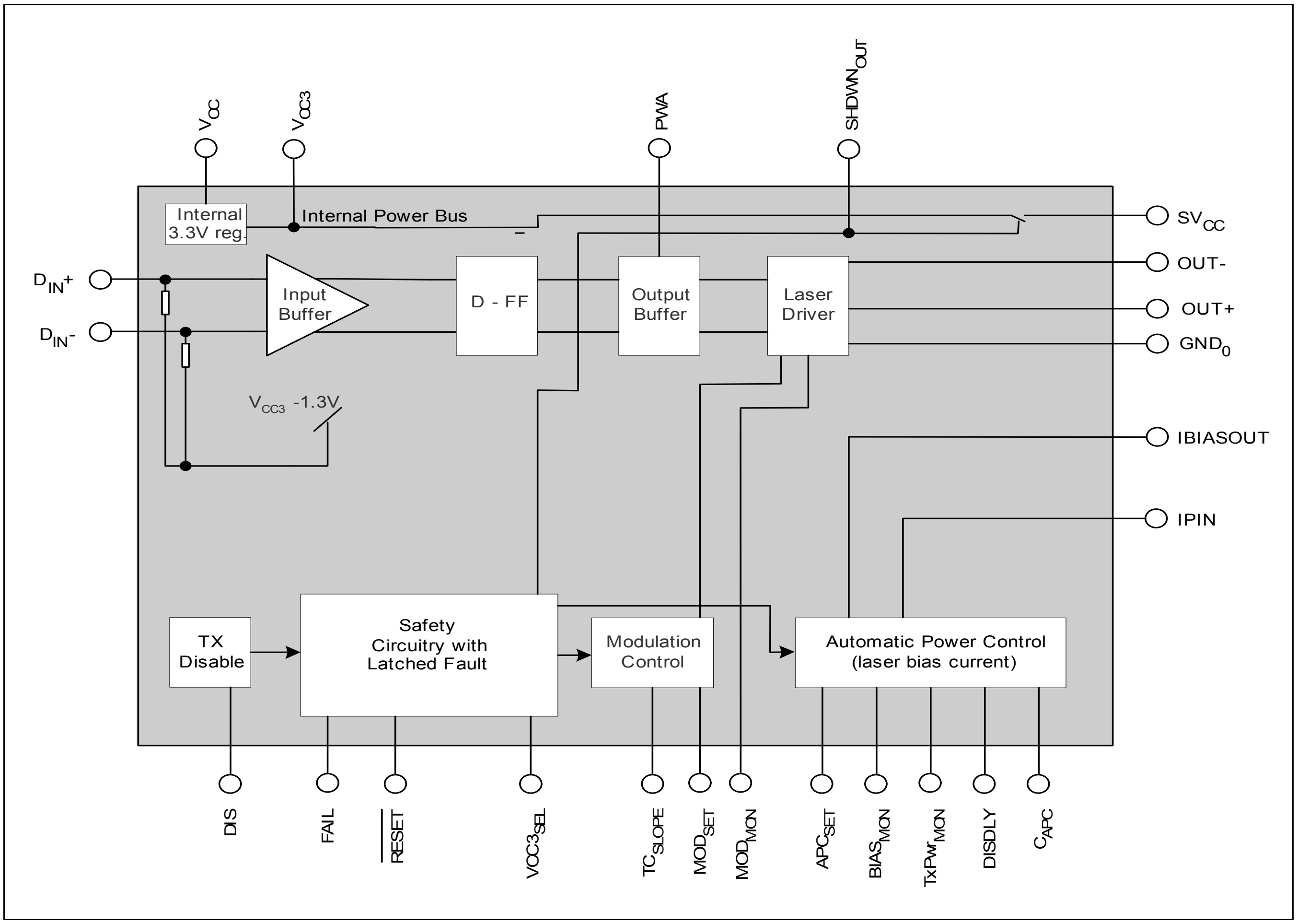
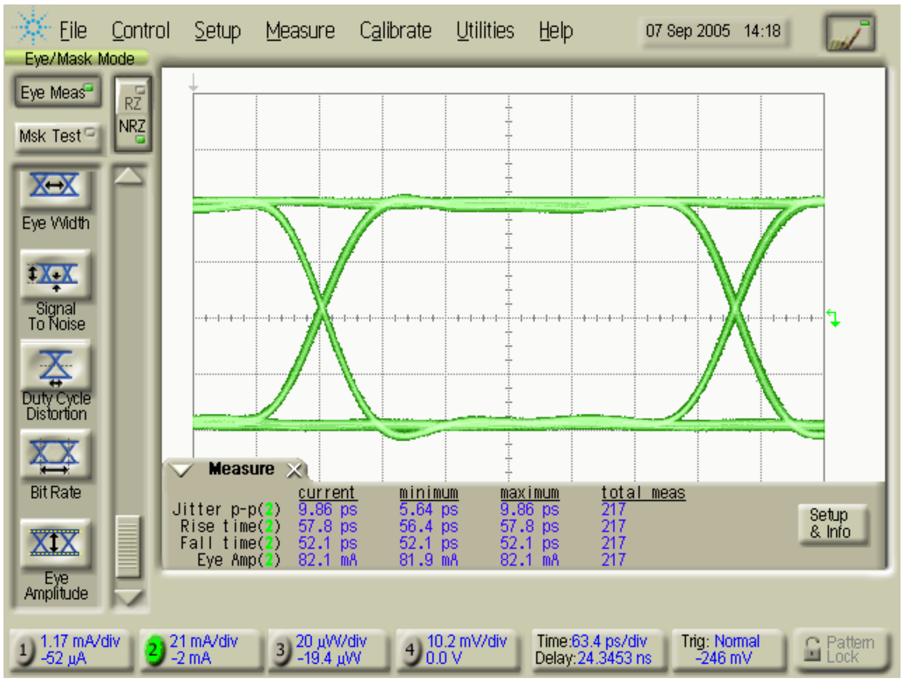
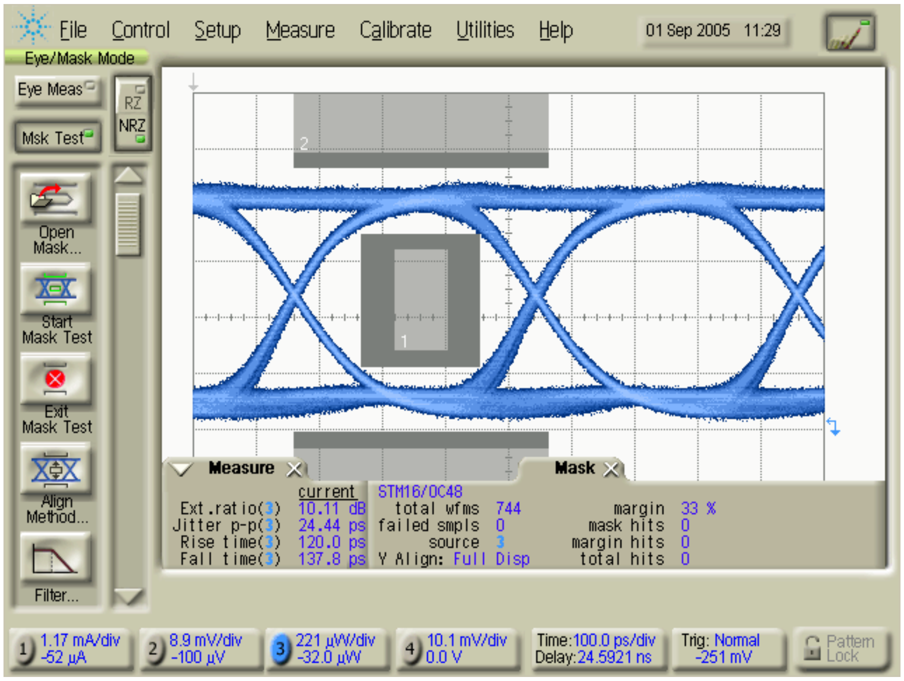


Figure 3-2. ***2.5Gbps Electrical Eye Diagram***



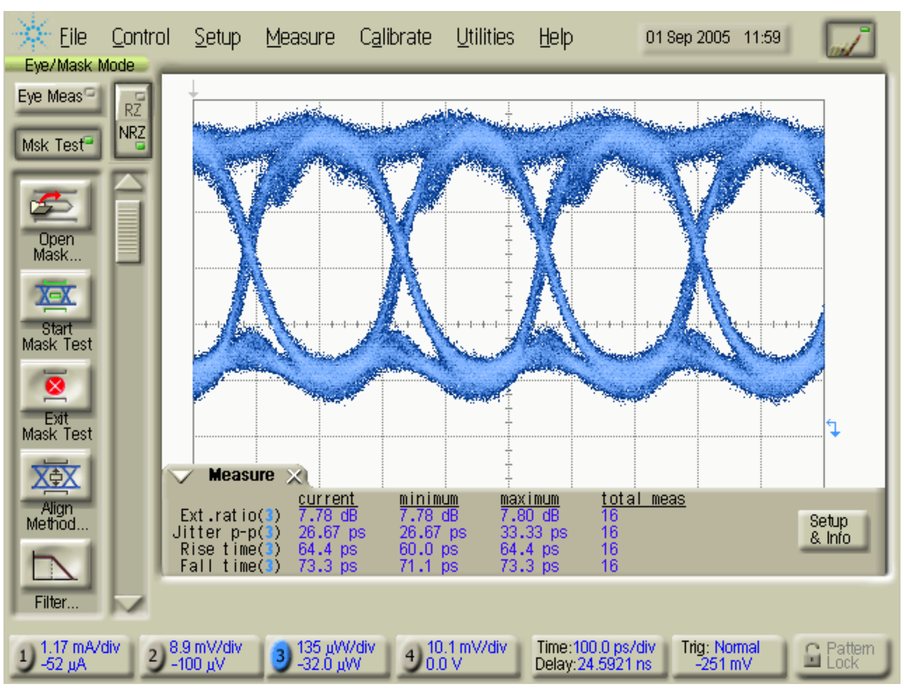
Conditions: 80mA modulation current, 2^7-1 PRBS

Figure 3-3. 2.5Gbps Filtered Optical Eye Diagram with NEC NX7315UA Laser



Conditions: 10dB extinction ratio, 33% eye margin, 2^7-1 PRBS

Figure 3-4. 4.25Gbps Unfiltered Optical Eye Diagram with Archcom AC3460 Laser



Conditions: 7.5dB extinction ratio, 2^7-1 PRBS

3.2 Features

- High speed operation; suitable for SFP/SFF applications from 155Mbps to 4.25 Gbps. Typical rise/fall times of 55 ps.
- Programmable temperature compensation. Modulation output and bias output can be controlled using a few discrete resistors.
- Supports DDMI (SFF-8472) diagnostics when combined with the M02088.
- DC or AC coupled modulation drive. Up to 100mA modulation current available when AC coupled.
- Low overshoot allows high extinction ratio with low jitter.
- Automatic Laser Power Control, with “Slow-Start”.
- Differential data inputs to minimize pattern dependent jitter, PECL and CML compatible.
- Packaged in a QFN24
- 3.3V or 5V operation

3.3 General Description

The M02061 is a highly integrated, programmable laser driver intended for SFP/SFF module with data rates up to 4.25 Gbps. Using differential PECL data inputs, the M02061 supplies the bias and modulation current required to drive an edge-emitting laser. Monitor outputs and internal safety logic support the DDMI requirements.

The M02061 laser driver consists of the following circuitry: an internal regulator, bias current generator and automatic power control, data and clock inputs, buffer with pulse width adjust, modulation current control, modulator output, laser fail indication, disable control, and monitor outputs for the bias current, modulation current, and transmitted power.

3.3.1 Internal Regulator

The M02061 contains an internal 3.3V regulator so high bit rate performance can be achieved with 5V or 3.3V power supply.

When operating from a 5V supply (V_{CC} is connected to +5V), an internal regulator provides a voltage of approximately 3.3V to the majority of the on-chip circuitry. The on-chip regulator is internally compensated, requiring no external components. When a 3.3V supply is used (V_{CC} and V_{CC3} connected to 3.3V) the regulator is switched off and the internal circuitry is powered directly through the V_{CC3} supply pin. The decision as to whether or not the internal regulator is required is made via the $VCC3_{SEL}$ pin, which also determines whether the safety circuitry needs to monitor for proper +5V supply voltage.

For 3.3V applications, SV_{CC} is sourced from V_{CC3} through a switch (leave SV_{CC} open for 5V applications). SV_{CC} is to be used to power the anode of the laser diode and the cathode of the photodiode, any resistive or ferrite pull-ups on the OUT+ and OUT- outputs should be connected directly to VCC.. When a fault condition is present, FAIL will assert and the switch sourcing SV_{CC} will open so no current can pass through the laser. SV_{CC} does not need any external capacitance, if capacitance to ground is added at SV_{CC} it should be $\leq$100pF.

For 5V operation, an analog switch controlled by SHTDWNOUT can be used to source 5V to the laser anode. In the case of a fault condition, SHTDWNOUT will go high and open the analog switch which will result in an open circuit at the laser. SHTDWNOUT is designed to drive a CMOS logic input. An FET transistor may have excessive Miller capacitance and a fault may be signalled if it turns on too slow.

V_{CC} and V_{CC3} status are internally monitored by the M02061 during power-up and normal operation. During power-up the “slow-start” circuitry requires that V_{CC} and V_{CC3} each reach an acceptable level before enabling bias or modulation current.

Table 3-1. Pin Connection for 3.3V and 5V V_{CC}

		Pin Connection For:	
		V_{CC} = 3.3V	V_{CC} = 5V
Pins Dependent on V_{CC} Voltage	V_{CC3}	Connect to V_{CC}	Reference for C_{APC} and PWA
	SV_{CC}	Laser Anode	OPEN
	$SHDWN_{OUT}$	OPEN	External safety control switch
	C_{APC}	Capacitor between C_{APC} and V_{CC3} or V_{CC}	Capacitor between C_{APC} and V_{CC3} (not V_{CC})
	PWA	Connect to V_{CC3} or V_{CC} to disable	Connect to V_{CC3} to disable (not V_{CC})
	$VCC3_{SEL}$	Connect to V_{CC3} or V_{CC}	Connect to GND

3.3.2 Bias Current Generator and Automatic Power Control

To maintain constant average optical power, the M02061 incorporates a control loop to compensate for the changes in laser threshold current over temperature and lifetime. The bias current will be determined by the value of the external resistor R_{APCSET} and the transfer efficiency between the laser and monitor photodiode.

The photo current from the monitor photodiode mounted in the laser package is sunk at I_{PIN}. This photo current is mirrored and an equivalent current is sourced from pins $TxPwr_{MON}$ and APC_{SET}. The APC loop adjusts the laser bias current (hence the monitor diode photo current) to maintain a voltage at APC_{SET} of 1 bandgap voltage or ~1.3V.

$R_{APCSET} * I_{PIN} = 1.3\ V$

The APC loop has a time constant determined by $C_{APC,}$ R_{APCSET} and the transfer efficiency between the laser and monitor photodiode. The larger the C_{APC} capacitor the lower the bandwidth of the loop and the larger R_{APCSET} the lower the loop BW.

In general, it is recommended that at least 2.2 nF of external capacitance be added externally between C_{APC} and V_{CC3}. With use of a 2.2 nF capacitor, the bias current can reach 90% of its final value within 1ms, i.e., bias current risetime is less than 1ms and the APC loop bandwidth is less than 30 kHz, which should be adequate for bit rates of 155Mbps. (and all higher bit rates).

The bias generator also includes a bias current monitor mirror ($BIAS_{MON}$), whose output current is typically 1/100th of the bias current. This pin can be connected directly through a resistor to ground. If this function is not needed this pin can be left open.

3.3.3 Data Inputs

Both CML and PECL inputs signals can be AC coupled to the M02061. These inputs are internally biased to approximately V_{CC3} - 1.3V. In most applications the data inputs are AC coupled with controlled impedance pcb traces which will need to be terminated externally with a 100Ω or 150Ω resistor between the + and - inputs.

PECL and CML signals may be DC coupled to the M02061 data inputs when both the M02061 and the source of the input signals are operating from 3.3V supplies. If the M02061 is operating from a 5V supply, PECL and CML signals may be DC coupled as long as the source of the input signals is operating at a 3.3V supply and the signals are referenced to VCC3 at the M02061.

3.3.4 Pulse Width Adjust

The data output buffer incorporates pulse-width adjustment control to compensate for laser pulse width distortion. A potentiometer can be connected between the PWA input and GND for adjustment (programming resistance should be between 1kΩ and 20kΩ). By adjusting the potentiometer, the pulse-width can be adjusted over a range of approximately ±40 ps. Pulse width control can be disabled by connecting PWA to V_{CC3}, resulting in roughly a 50% crossing point at the output and reducing supply current by approximately 1.5mA.

3.3.5 Modulation Control

There are programmable control lines for controlling the modulation current and its temperature compensation. These inputs can be programmed simply with a resistor to ground.

The modulation current amplitude is controlled by the MOD_{SET} input pin. The modulation current is temperature compensated by the TC_{SLOPE} inputs. The temperature compensation is independent of the setting.

If the temperature compensation at TCSLOPE is disabled, the modulation output current is simply:

$IOUT = 100 \times (1.3V / R_{MODSET})$

Where R_{MODSET} is the resistance from pin MOD_{SET} to ground.

Figure 3-5 is the most accurate method for selecting RTCslope.

However, you can also select $R_{TCSLOPE}$ using the following relationship:

$R_{TCSLOPE} = 19.5*(TC)^{-1.5}$, where TC is the desired slope of the modulation current from 25°C to 85°C in%/°C and $R_{TCSLOPE}$ is in kΩ. If no temperature compensation is desired, leave $R_{TCSLOPE}$ open.

In any case, $R_{TCSLOPE}$ will have negligible effect at M02061 case temperatures below 10°C.

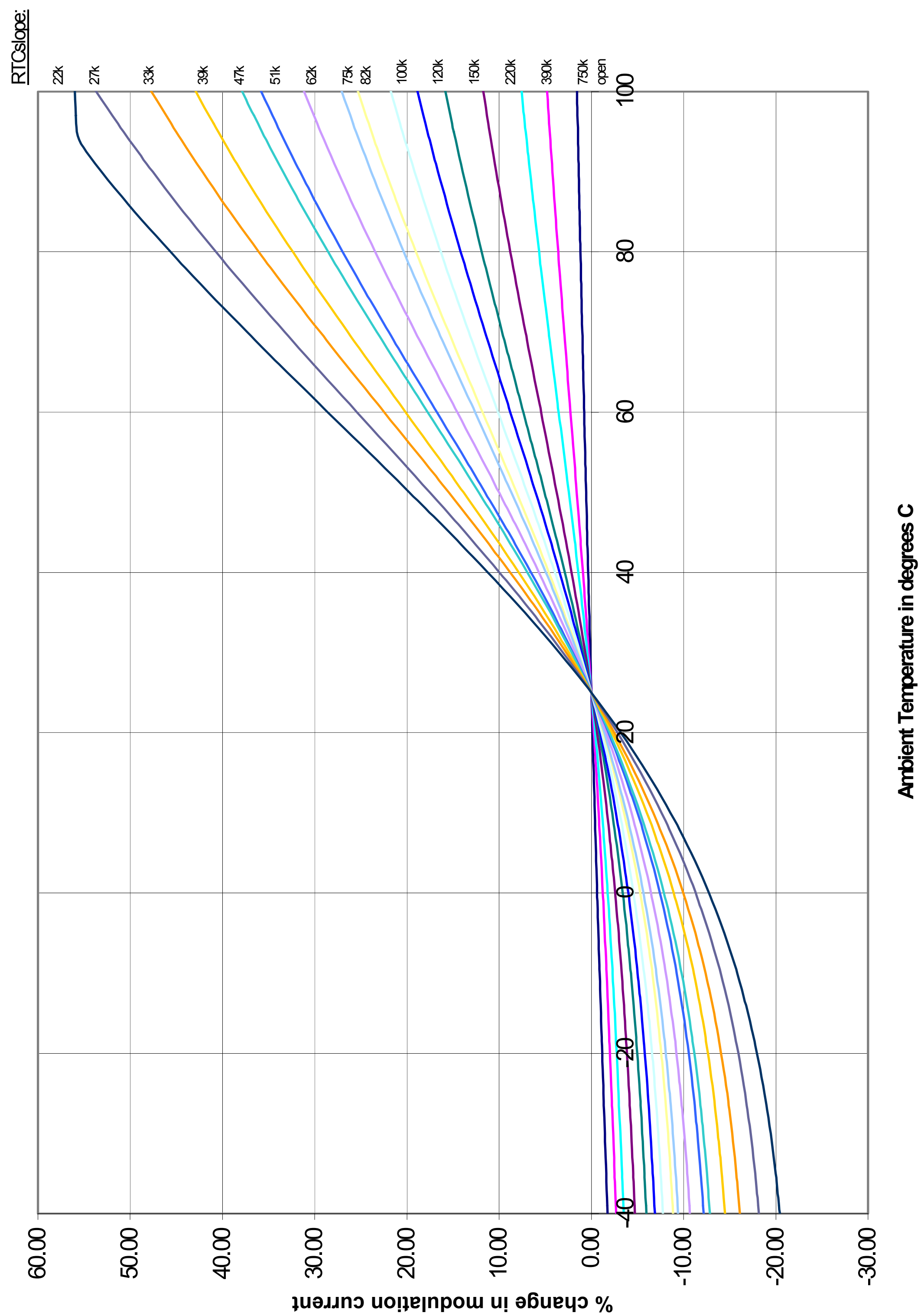
For example:

Given a laser with a desired modulation current at low temperatures of 30mA and a temperature coefficient of -0.5%/°C at high temperatures (which will require a laser driver temperature coefficient of +0.5%).

Choose $R_{MODSET} = 100 \times (1.3V / 30mA) = 4.3k\Omega$

Choose $R_{TCSLOPE} = 19.5*(0.5)^{-1.5}\ k\Omega = 56k\Omega$.

Figure 3-5.


RTCslope:
22k
27k
33k
39k
47k
51k
62k
75k
82k
100k
120k
150k
220k
390k
750k
open
60.00
50.00
40.00
30.00
20.00
10.00
0.00
-10.00
-20.00
-30.00
% change in modulation current
-40
-20
0
20
40
60
80
100
Ambient Temperature in degrees C

3.3.6 Modulator Output

The output stage is designed to drive a 25Ω output load over a wide range of currents and circuit architectures. The laser may be AC, DC, or Differentially coupled depending on the supply voltage.

Table 3-1. Modulation Current Maximums

	Max Modulation Current	Max Bias Current
V_{CC}=5V, Laser DC coupled	80	60
V_{CC}=5V, Laser AC coupled	80(1)	60
V_{CC}=3.3V, Laser DC coupled	100(2)	100
V_{CC}=3.3V, Laser AC coupled	100	100

When differentially coupling, the maximum modulation and bias current is determined by either the AC or DC coupling of the OUT+ or OUT- output, whichever has the minimum rating.

1. When AC coupling the output should never be allowed to swing above the absolute voltage rating of the part, which is 6V.

2. When V_{CC}=3.3V, the OUT+ and OUT- should not be driven below 1.6V. In most 3.3V applications, this will make DC coupling impractical.

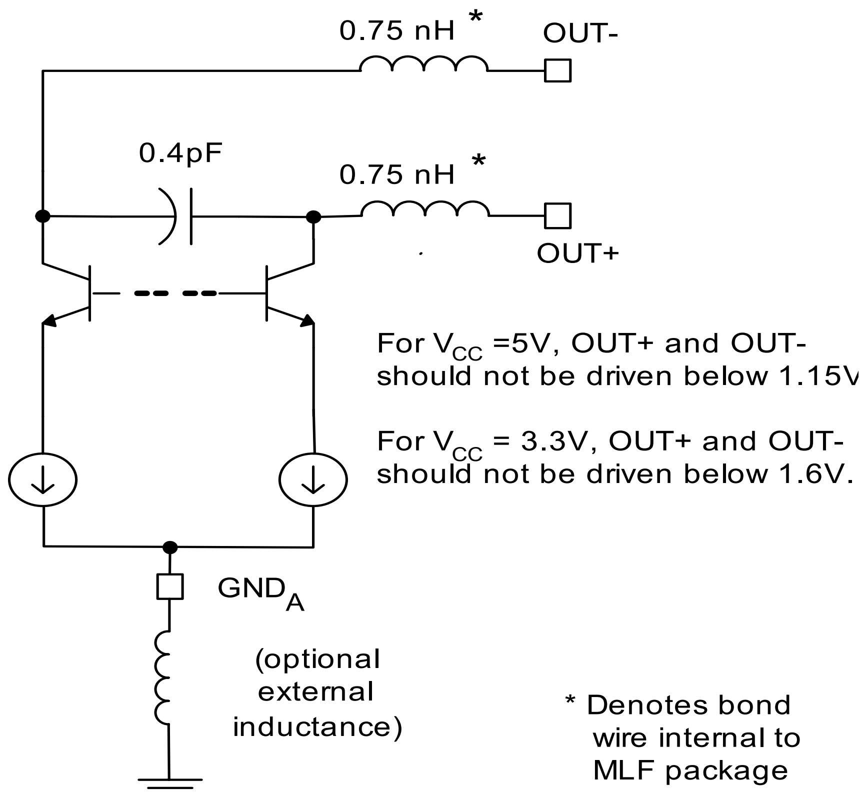
When DC coupled, OUT+ should be connected through a series resistor to the laser such that the total impedance seen at the output is 25 ohms. This will result in the optimum pulse response while allowing the maximum modulation current (see Figure 4-2).

The output can also be AC coupled to the laser. This is the required operating mode when using a 3.3V supply (unless the laser has a small forward voltage and OUT+ will not go below 1.6V). When AC coupled the dynamic resistance seen by OUT+ should still be 25 ohms. In addition to a resistor in series with the laser, a capacitor is added in series and a ferrite is used to pull up the collector at OUT+ to V_{CC}.

When the laser is AC coupled, the OUT- pin is usually tied to the laser anode through an AC coupled series resistor which matches the impedance seen by the OUT+ pad (see Figure 4-1).

The output stage also has a separate current path to GND labelled GND_0. This isolates the output switching currents from the rest of the system.

Figure 3-6. Modulator Output



3.3.7 Fail Output

The M02061 has a FAIL alarm output which is compatible with the TX_FAULT signalling requirements of common pluggable module standards.

The ESD protection on this pin provides a true open collector output that can withstand significant variation in V_{CC} when signalling between circuit boards. Also, if the M02061 loses power the pull-up will signal a fail condition. In a simple static protection scheme used by other ICs the protection diodes would clamp the FAIL signal to ground when the chip loses power.

3.3.8 TX Disable and Disable Delay Control

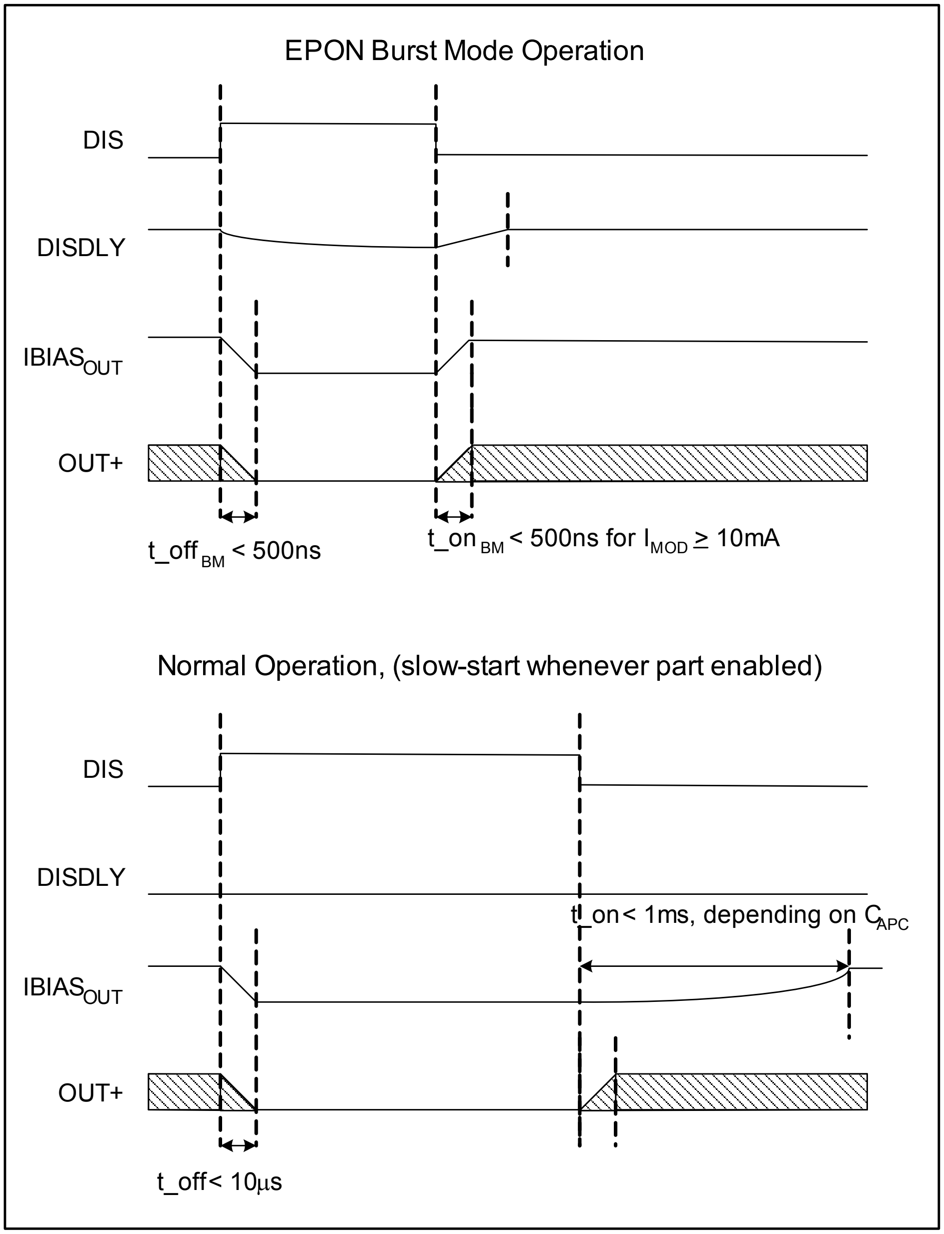
The DIS pin is used to disable the transmit signal (both the modulation and bias current are disabled when DIS = high).

The DIS input is compatible with TTL levels regardless of whether VCC = 5V or VCC = 3.3V. The external 4.7kΩ and 10kΩ pull-up resistor required by most interface standards is not needed because this pin has an internal 7kΩ resistor to V_{CC}.

The DISDLY pin is used in conjunction with the DIS pin to control bias current enable time. In normal operation the DISDLY pin should be connected to ground. In this case, each time DIS transitions from high to low the bias current will be enabled by the “slow-start” circuitry (enable time of less than 1 ms with a C_{APC} = 2.2nF).

For burst mode operation a capacitor C is added to the DISDLY pin, the slow-start circuitry is disabled for approximately $T = 3 * 10^6$ (sec/F) * C (F) following the DIS high transition (see figure 8). If the part is enabled (DIS transitions low) during this time the bias and modulation current will quickly return to within 90% of their final value (in less than 500ns). If DIS transitions low after the DISDLY time the slow-start circuitry will engage and the bias current will not return to its final value for approximately 1ms (depending on the C_{APC} capacitor value).

Figure 3-7. DIS and DISDLY Timing



3.3.9 Monitor Outputs

To facilitate complying with laser safety and DDMI[1] requirements, output monitors are provided for transmit power ($TxPwr_{MON}$) bias ($BIAS_{MON}$) and modulation current (MOD_{MON}).

These outputs will source current proportional to the emitted optical power ($TxPwr_{MON}$) the bias current ($BIAS_{MON}$) and modulation current (MOD_{MON}). These pins should be terminated with a resistor to ground that sets the desired full-scale voltage (not to exceed V_{CC3}-1V). Using a monitor polarity selection (MON_{POL}) these monitors can be set to sink current instead of source current. They will then need to be terminated with a resistor to V_{CC3} and the induced voltage should not exceed 2.5V.

If the outputs of these monitors are not needed, MON_{POL}, $TxPwr_{MON}$, $BIAS_{MON}$, and MOD_{MON} can all be left floating and the chip current consumption will be reduced by the value of the monitor currents.

3.4 Laser Eye Safety

Using this laser driver in the manner described herein does not ensure that the resulting laser transmitter complies with established standards such as IEC 825. Users must take the necessary precautions to ensure that eye safety and other applicable standards are met. Note that determining and implementing the level of fault tolerance required by the applications that this part is going into is the responsibility of the transmitter designer and manufacturer since the application of this device cannot be controlled by Mindspeed.

3.4.1 Safety Circuitry

Safety Circuitry in the M02061 will disable the modulation and bias current and assert the FAIL output immediately upon detecting a fault condition. In addition, the supply voltage that sources the laser (SV_{CC} or an external switch controlled by $SHDWN_{OUT}$) will immediately go open circuit and prevent any current from passing through the laser.

Fault conditions checked by the M02061 include shorts to ground or VCC of all pins which can increase the laser modulation or bias current.

For an initialization sequence to be successful, all the fault detection monitors must signal that the chip is "healthy". When DIS goes low, pins are checked for shorts to ground or V_{CC} and a FAIL condition is latched if there is a fault.

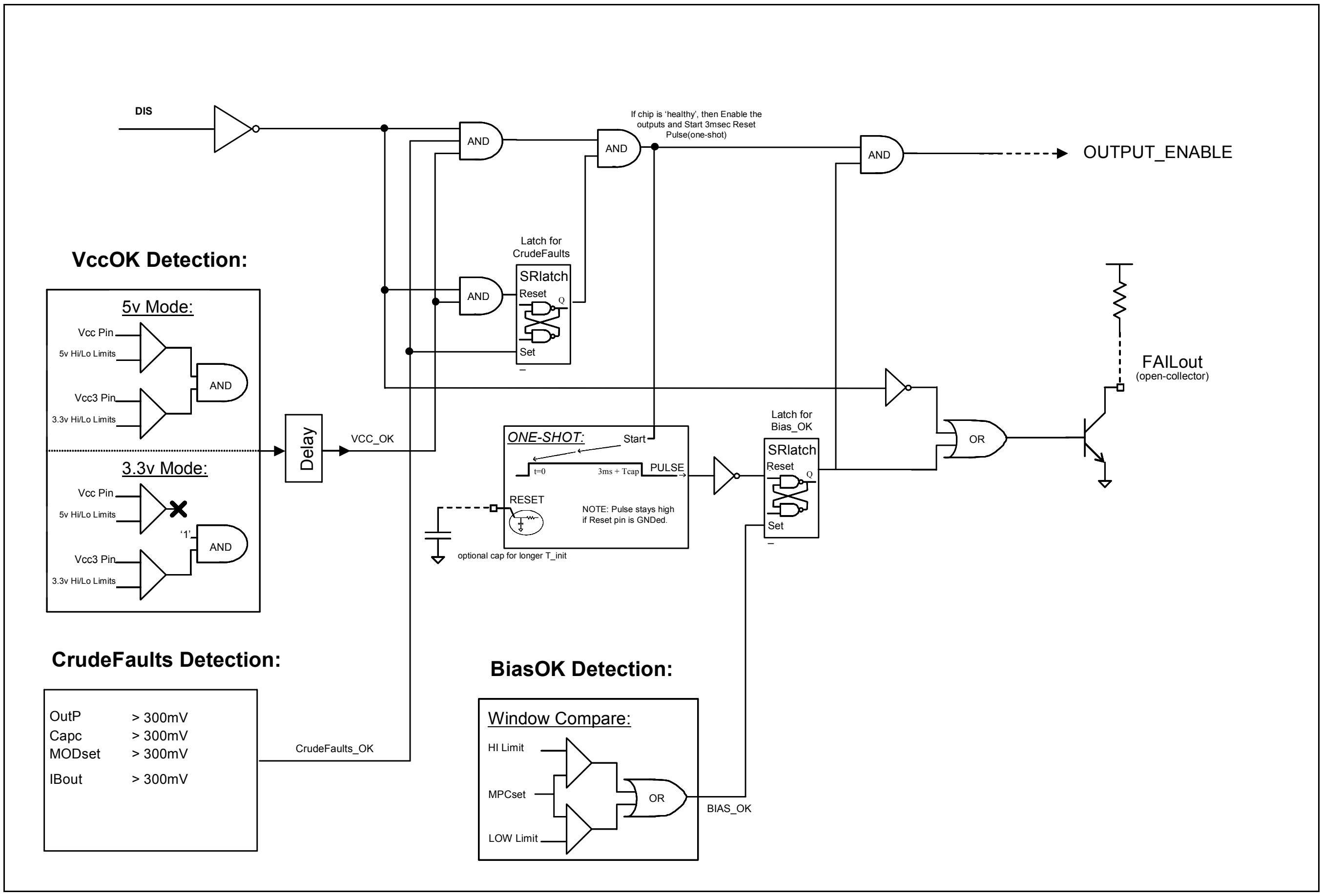
If the state of the pins is OK, a one-shot at the reset pin begins a countdown which will latch a FAIL condition if the bias current has not stabilized to an acceptable level during the one-shot time. The one-shot can be extended with an external capacitor connected from the RESET pin to ground.

The one-shot[1] width is approximately:

$T_{ONE\text{-}SHOT}$ = 3 ms + (0.3 ms/pF)x(external capacitance).

1.The one-shot is actually comprised of an oscillator and 10-bit counter.

Figure 3-8. Safety Circuit Block Diagram



3.5 Fault Conditions

This section describes the M02061 operating modes during fault conditions. Over voltage, under voltage, pins shorted to V_{CC} and pins shorted to ground are included in the fault table.

Table 3-2. Circuit Response to Single-point Fault Conditions [1 2]

Pin Name	Circuit Response to Over-voltage Condition or Short to V_{CC}	Circuit Response to Under-Voltage Condition or Short to Ground
V_{CC}	Bias and modulation outputs are disabled once V_{CC} rises above the supply detection (high voltage) threshold	Bias and modulation outputs are disabled once V_{CC} drops below the supply detection (low voltage) threshold
DIN+, DIN-	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs.[1,2]	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs.[1,2]
$VCC3_{SEL}$	Does not affect laser power.	Does not affect laser power.
DIS	Bias and modulation outputs are disabled. 3.3V operation - SV_{CC} is opened. 5V operation - $SHDWN_{OUT}$ goes high.	Does not affect laser power (normal condition for circuit operation).
FAIL	Does not affect laser power.	Does not affect laser power.
RESET	Does not affect laser power.	Does not affect laser power.
MOD_{MON}	Does not affect laser power.	Does not affect laser power.
$BIAS_{MON}$	Does not affect laser power.	Does not affect laser power.
$TxPWR_{MON}$	Does not affect laser power.	Does not affect laser power.
APC_{SET}	A fault state occurs.[1]	A fault state occurs.[1]
I_{PIN}	A fault state occurs.[1]	A fault state occurs.[1]
$IBIAS_{OUT}$	The laser will be turned off, then a fault state occurs.[1]	A fault state occurs.[1]
OUT_P	Laser modulation is prevented; the APC loop will increase the bias current to compensate for the drop in laser power if it is DC coupled. If the set output power can not be obtained, a fault state occurs.[1,2]	A fault state occurs.[1]
OUT_N	Does not affect laser power.	Does not affect laser power.
SV_{CC}	Does not affect laser power.	Laser bias current will be shut off and a fault state occurs.[1]
C_{APC}	Laser bias current will be shut off, then a fault state occurs.[1]	A fault state occurs.[1]
V_{CC3}	Bias and modulation outputs are disabled once V_{CC3} rises above the supply detection (high voltage) threshold	Bias and modulation outputs are disabled once V_{CC3} drops below the supply detection (low voltage) threshold
PWA	Does not affect laser power.	Does not affect laser power
$SHDWN_{OUT}$	Does not affect laser power. if this pin is used to control an external switch, laser current is disabled and fault state occurs.[1]	Does not affect laser power.
MOD_{SET}	The APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs.[1,2]	A fault state occurs.[1]

Table 3-2. Circuit Response to Single-point Fault Conditions [1 2]

Pin Name	Circuit Response to Over-voltage Condition or Short to V_{CC}	Circuit Response to Under-Voltage Condition or Short to Ground
TC_{SLOPE}	Does not affect laser power.	May affect laser power. If this is the case, the APC loop will attempt to compensate for the change in output power. If the APC loop can not maintain the set average power, a fault state occurs.[1,2]
DISDLY	Does not affect laser power.	Does not affect laser power.

Notes:
1. A fault state will assert the FAIL output, disable bias and modulation outputs and will either open the switch at SV_{CC} (3.3V operation) or $SHDWN_{OUT}$ will go high (5V operation).
2. Does not affect laser power when the output is AC coupled to the laser.

4.0 Applications Information

4.1 General

- SFP and SFF Modules
- 1G/2G/4G Fibre Channel modules
- Short reach and Metro SONET/SDH

Figure 4-1 and Figure 4-2 illustrate typical applications for 3.3/AC coupled and 5V/DC coupled laser.

Figure 4-1. Application Diagram, VCC = 3.3V Laser AC Coupled Example

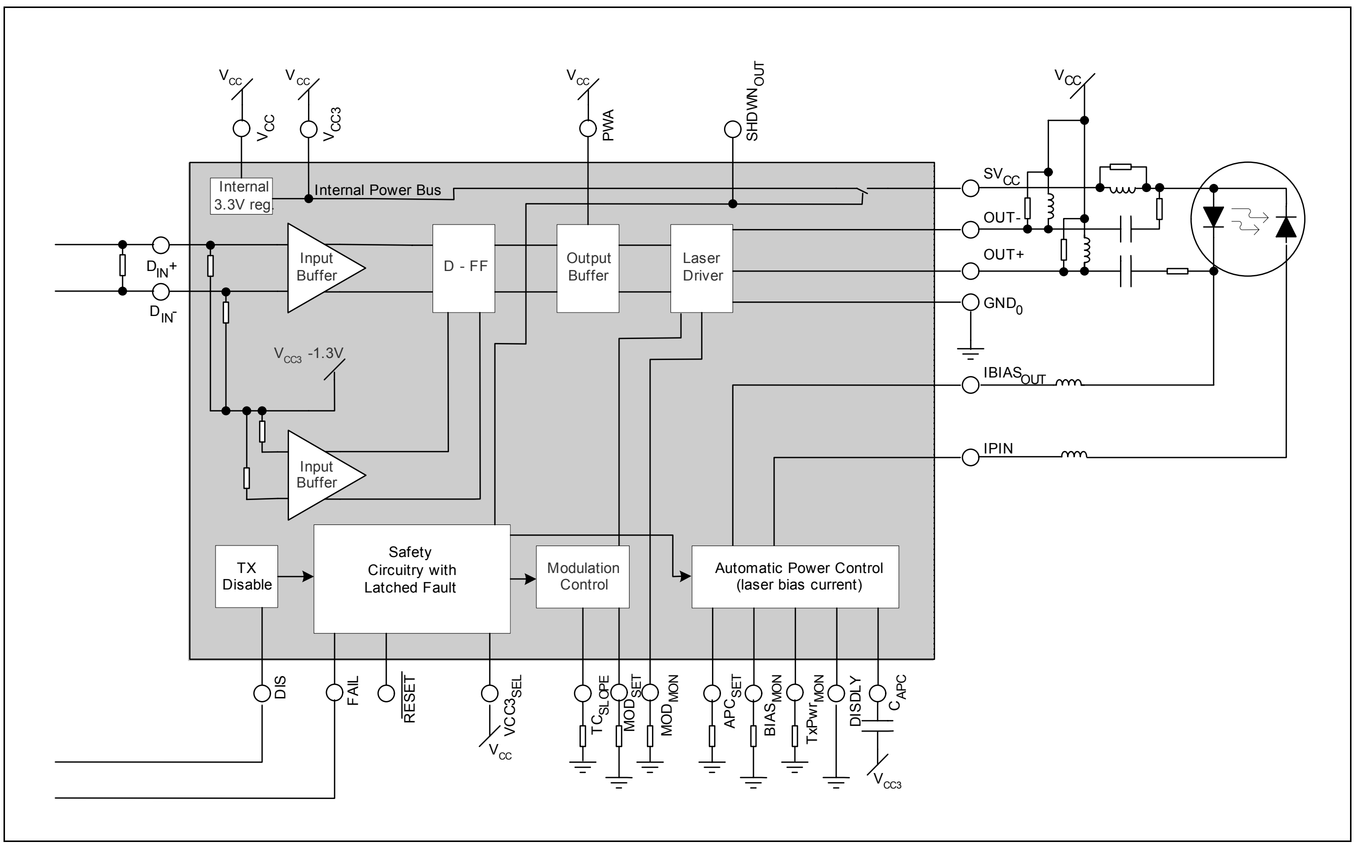
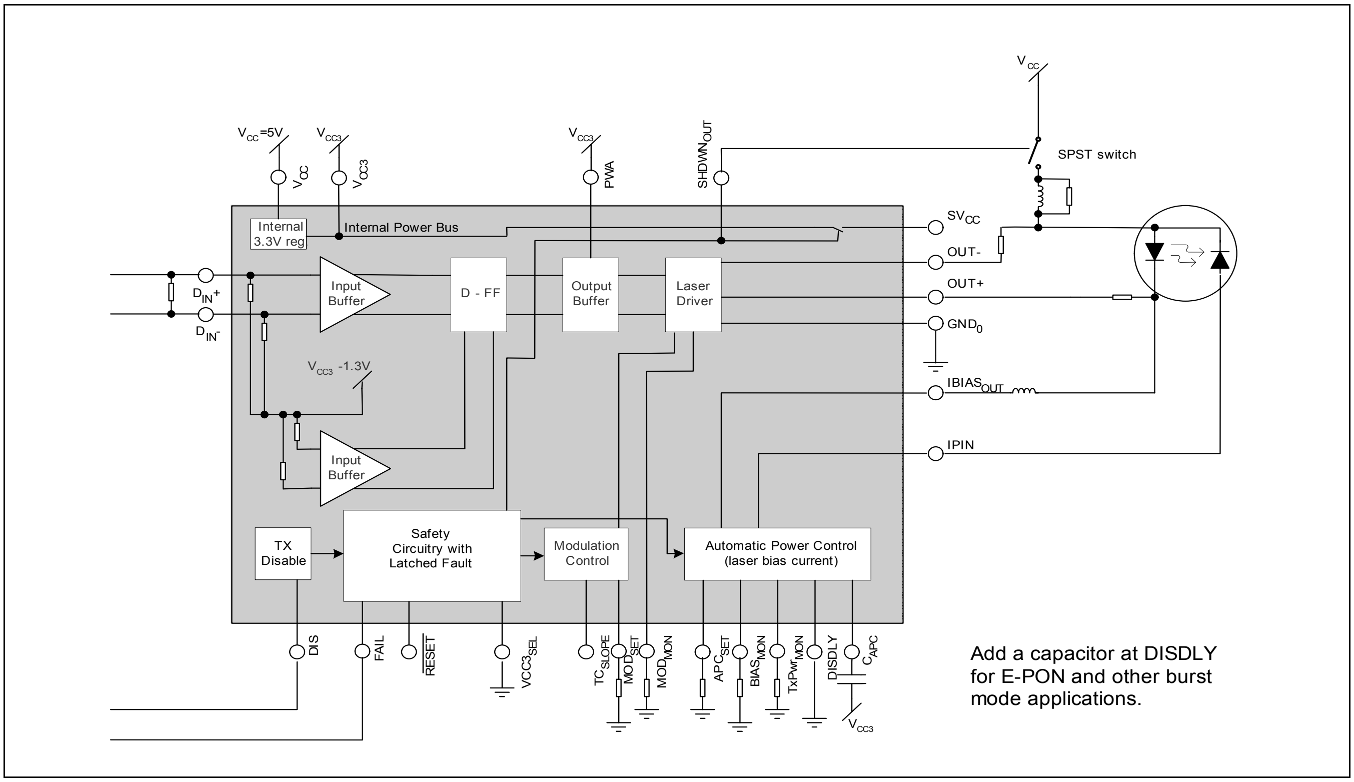


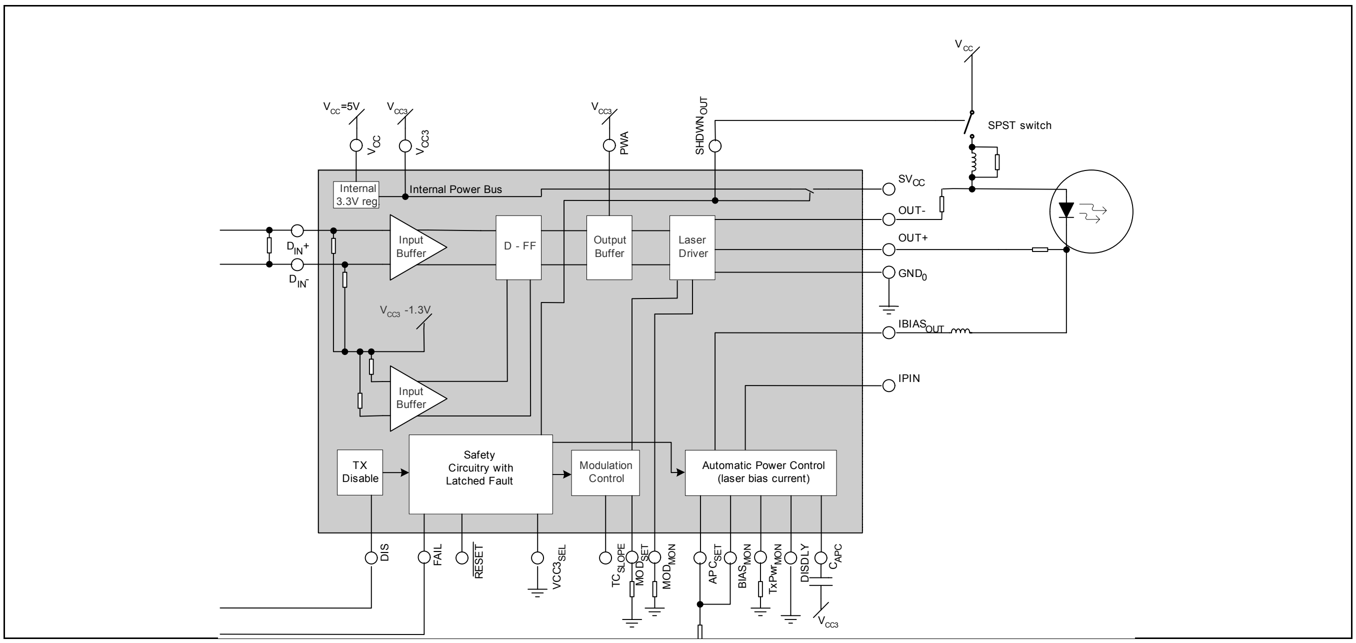
Figure 4-2. Application Diagram, VCC = 5V Laser DC Coupled Example



4.2 Video Operation

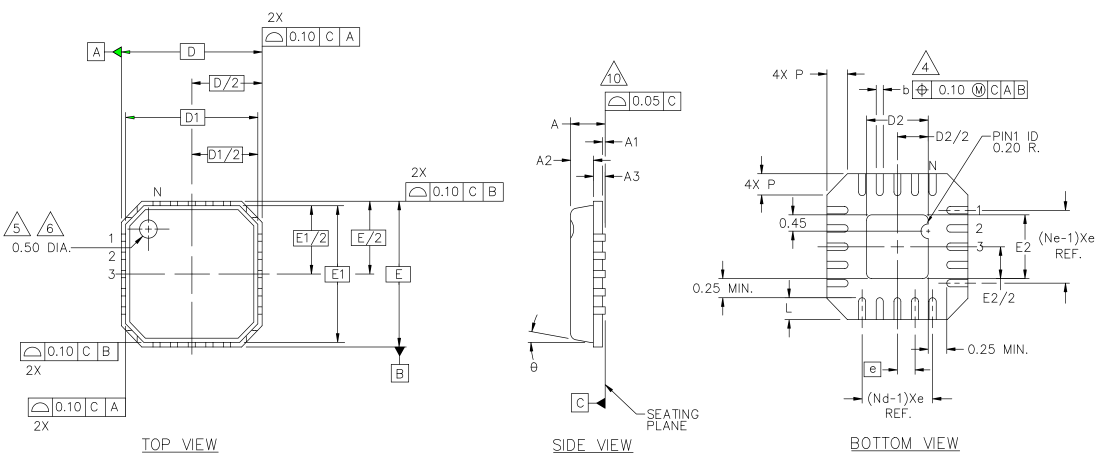
The M02061 can be used to transmit digital video optical data even in the presence of the pathological signal. This is done by fully DC coupling the signal from the input to the laser output.In most data communications applications, AC coupling occurs at 3 points in a laser driver schematic: the data inputs, the APC control, and coupling the modulation current to the laser. In the M02061 DC coupling can be used at all 3 of these points.The data inputs can be DC coupled using PECL or CML levels (see Section 3.3.3, “Data Inputs”). LVDS signals can be DC coupled with level shifting.The APC of the bias current is controlled by feedback from the monitor photodiode in the laser package in most communications applications. In video applications this monitor photodiode should not be used if the pathological pattern may occur. Instead, the APC should be controlled in an "open loop" configuration. (Open loop simply means a monitor photodiode is not used). In the open loop configuration the APC is controlled by a resistor or a thermistor network or a look-up table. This removes AC time constants from the bias current. In Figure 4-3 the BIASmon pin is connected to the APCset pin. In this case the bias current is IBIAS = 100 x (1.3V / RAPCset)The modulation current output OUT+ can be DC coupled to the laser as shown in Figure 4-3. There are no AC time constants in the modulation current amplitude in this configuration.

Figure 4-3. Video Application Block Diagram

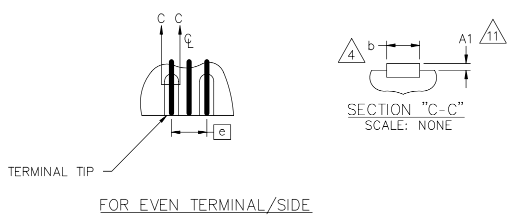


5.0 Package Specification

Figure 5-1. QFN24 Package Information



Note: View is for a 20 pin package. All dimensions in the tables apply for the 24 pin package



SYMBOL	PITCH VARIATION D MIN.	NOM.	MAX.	NOTE
e		0.50 BSC		
N		24		3
Nd		6		3
Ne		6		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	2.19	2.34	2.49	
E2	2.19	2.34	2.49	

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	-	0.85	1.00	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.80	
A3		0.20 REF.		
D		4.00 BSC		
D1		3.75 BSC		
E		4.00 BSC		
E1		3.75 BSC		
θ			12°	
P	0.24	0.42	0.60	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS. Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION & Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.

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