Hybrid Systems
Sipex Corporation

HS 9378 Series
μP Compatible, 16-Bit DAC

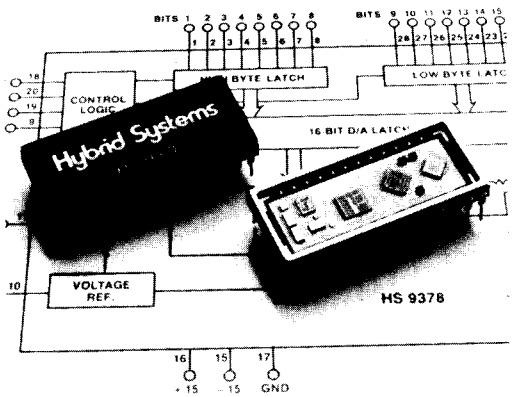
DESCRIPTION

The HS 9378 is a complete voltage output, 16-Bit D/A converter with 16-Bit monotonicity guaranteed at room temperature. Complete with dual storage registers, internal reference and an output amplifier, the HS 9378 series easily interfaces with either 8-Bit or 16-Bit bus structures, eliminating the need for external latches.

A proprietary semicustom gate array is used to significantly reduce digital feedthrough while internal decoupling capacitors reduce the effect of power supply perturbations.

The HS 9378 has dual 8-Bit input registers for direct interface to 8- or 16-Bit bus structures. The pinout of the HS 9378 allows the user with an 8-Bit bus to run only 8 traces directly underneath the hybrid to connect to the 16-Bit input register.

The HS 9378 is available for either commercial (+0°C to +70°C) or military (−55°C to +125°C) applications. Screening to MIL-STD-883 Rev. C, Levels B or S, is available.



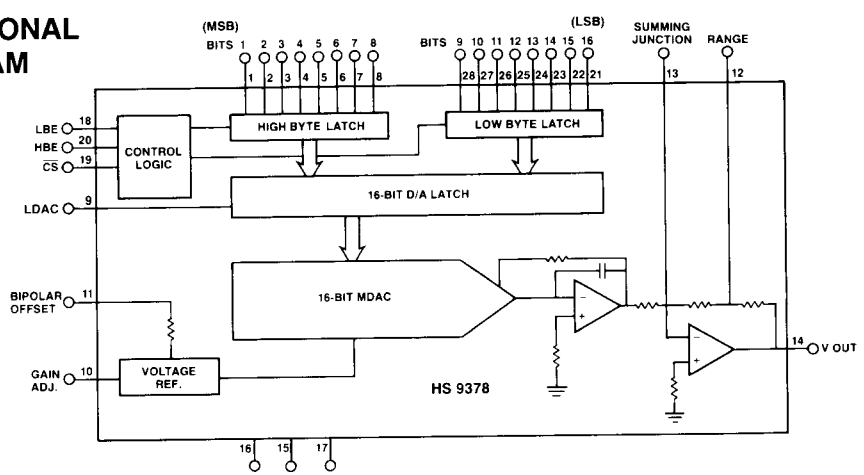
FEATURES

1. Monotonic to 16-Bits at 25°C
2. Double Buffered Input.
3. Proprietary Semicustom Gate Array Signficantly Reduces Digital Feedthrough.
4. Pinout Permits 16 Digital Input Lines to be Connected to an 8-Bit Data Bus without Crossing Bus Lines.

BENEFITS

1. Will Not Cause Oscillations When Used in Feedback Loops for Servo Applications.
2. Allows Direct Interface to 8- or 16-Bit Bus Structure without the Need for External Latches.
3. Eliminates the Need for Output Filtering.
4. Simplifies PC Board Layout.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

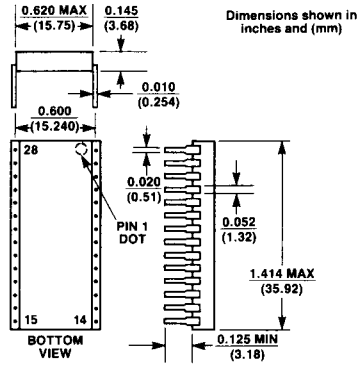
(Typical @ + 25°C unless otherwise specified)

MODEL	HS 9378C	HS 9378TB	HS 9378SB
DIGITAL INPUT			
Resolution	16-bits	•	•
Coding	Straight/Offset Binary	•	•
Logic Compatibility	TTL, LSTTL, CMOS		
V_{IL} (max)[6]	0.8V	•	•
V_{IH} (min)[6]	2.4V		
Input Current	10 μA max	•	•
Latch Control Minimum Pulse Width	100 nsec	•	•
Data Set-Up Time	100 nsec min[1]	•	•
Data Hold Time	0 nsec	•	•
ANALOG OUTPUT			
Scale Factor Error	±0.20% F.S.R. max[2]	•	•
Initial Offset			
Unipolar	±0.15% F.S.R. max[2]	±0.05% F.S.R. max[2]	±0.05% F.S.R. max[2]
Bipolar	±0.15% F.S.R. max[2]	±0.05% F.S.R. max[2]	±0.05% F.S.R. max[2]
Voltage Range			
Unipolar	0 to +10V	•	•
Bipolar	+5V, ±10V	•	•
Current Compliance[5]	5 mA	•	•
Output Impedance	1Ω max	•	•
Noise p-p noise (0.1 Hz to 100 Hz)	50 μV	•	•
STATIC PERFORMANCE			
Integral Linearity Error[3]	0.0008% typ 0.0015% max	0.0008% typ 0.0015% max	0.0015% typ 0.003% max
Differential Linearity Error[4]	0.0015% max	•	0.003% max
Monotonicity Guaranteed to:			
(room temperature)	16 bits	16 bits	15 bits
(over temperature)	15 bits	15 bits	14 bits
Glitch Energy[7]	3 nV-sec	•	•
DYNAMIC PERFORMANCE			
Major Carry Transition Settling to 0.0015% F.S.R.	16 μsec	•	•
Slew Rate	1.7 V/μsec	•	•
Full Scale Transition Settling to 0.0015% F.S.R.	22 μsec	•	•
STABILITY			
Gain	10 ppm/°C max	10 ppm/°C max	15 ppm/°C max
Linearity Drift	1 ppm/°C max	•	•
Offset Drift			
Unipolar	5 ppm/°C	2 ppm/°C	5 ppm/°C
Bipolar	10 ppm/°C	5 ppm/°C	10 ppm/°C
POWER SUPPLY			
Requirements	+15V, ±5% @ 26.3 mA max	•	•
	−15V, ±5% @ 10.3 mA max	•	•
Rejection Ratio	±0.0006% FS/% V_{CC} typ. ±0.002% FS/% V_{CC} max	•	•
Power Dissipation	425 mW typ. 550 mW max	•	•
TEMPERATURE RANGE			
Operating			
C model	0°C to +70°C		
B-model	−55°C to +125°C		
Storage			
C model	−25°C to +85°C		
B-model	−65°C to +150°C		
PACKAGE			
28-pin double DIP			

NOTES:

1. −55°C to +125°C.
2. Adjustable to zero.
3. Integral Linearity is measured per end point definition.
4. Differential Linearity is the deviation of an output step from the theoretical value of 1 LSB for any two adjacent digital input codes.
5. Analog output is fully protected against infinite duration short circuit to ground.
6. Voltages at the digital inputs may not go below 0 volts or exceed +5V.
7. For minimum glitch, lid of Case B units must be grounded.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	BIT 1 (MSB)	28	BIT 9
2	BIT 2	27	BIT 10
3	BIT 3	26	BIT 11
4	BIT 4	25	BIT 12
5	BIT 5	24	BIT 13
6	BIT 6	23	BIT 14
7	BIT 7	22	BIT 15
8	BIT 8	21	BIT 16 (LSB)
9	LDAC	20	HBE
10	GAIN ADJ	19	$\overline{CS}$
11	BIPOLAR OFFSET	18	LBE
12	RANGE	17	GND
13	SUM JCT	16	+15V
14	V_{out}	15	−15V

ABSOLUTE MAXIMUM RATINGS (HS 9378)

+15V Supply (+V_{DD}) to GND ..... +17V

−15V Supply (−V_{DD}) to GND ..... −22V

Digital Input Voltage to GND 6.5V

Analog Input Voltage to GND

Pins 10, 12 ..... ±V_{DD}

Pin 11 ..... +V_{DD} max, −9V min

Pin 13 ..... ±0.1V

V_{OUT} ..... Indefinite short to GND

Package Power Dissipation

(Case A) ..... 1.4W @ +85°C

(Case B) ..... 1.5W @ +125°C

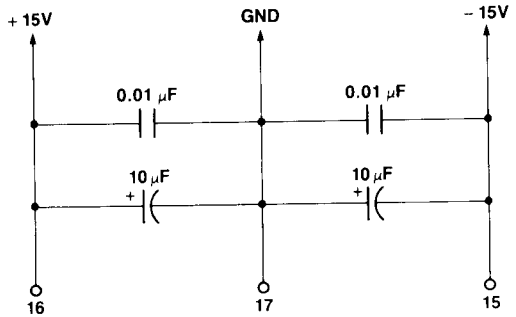
Lead Temperature, Soldering

(Case A) ..... 300°C, 5 sec

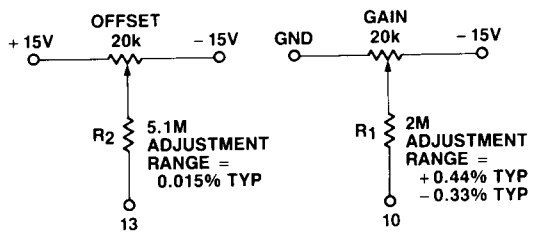
(Case B) ..... 300°C, 10 sec

APPLICATIONS INFORMATION

RECOMMENDED BYPASS CIRCUIT



OPTIONAL OFFSET & GAIN ADJUSTMENT CIRCUIT



Values of R_1 & R_2 can be changed to increase or decrease the sensitivity of the adjustment. (This adjustment should not be greater than ± 1% around the nominal value for best performance.) Decreasing the R_1/R_2 value increases the range of adjustment.

CALIBRATION PROCEDURE
(for optional external Gain & Offset adjustment)

Unipolar operation:

1. Apply a 0 0 0...0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 1 1 1...1 input code and set the GAIN ADJ pot for F.S. – 1 LSB.

Bipolar operation:

1. Apply a 1 0 0...0 input code and set the OFFSET ADJ pot for 0V out.
2. Apply a 0 0 0...0 input code and set the GAIN ADJ pot for – F.S.

TRANSFER CHARACTERISTICS

UNIPOLAR OPERATION

BINARY INPUT	ANALOG OUTPUT
1 1 1 1 1 1	+ F.S. – 1 LSB
1 0 0 0 0 0	+ F.S./2
0 1 1 1 1 1	+ F.S./2 – 1 LSB
0 0 0 0 0 0	0V

BIPOLAR OPERATION

BINARY INPUT	ANALOG OUTPUT
1 1 1 1 1 1	+ F.S. – 1 LSB
1 0 0 0 0 0	0V
0 1 1 1 1 1	– 1 LSB
0 0 0 0 0 0	– F.S.

MICROPROCESSOR INTERFACE CONSIDERATIONS

General

The HS 9378 is easily interfaced to either an 8-bit or 16-bit microprocessor. First, a signal to select (or address) the HS 9378 must be generated. Then the input data must be written (or latched) to the DAC and after settling, the analog output is valid.

The bus interface logic consists of three independently addressable registers in two buffers. The first buffer consists of two 8-bit registers which can be loaded directly from an 8- or 16-bit microprocessor bus. Once the complete 16-bit word has been assembled in the first buffer, it can be loaded into the second buffer for conversion.

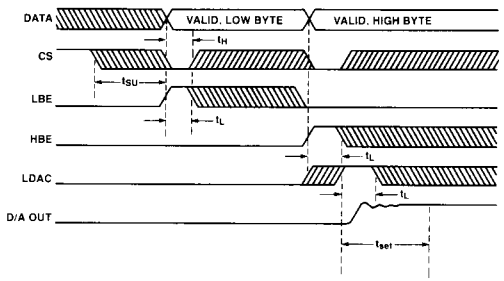
The required selection signal, $\overline{CS}$, is easily derived in most systems. Usually a base address is decoded and this active low signal is used for $\overline{CS}$. The active high signal for the low byte enable (LBE) and high byte enable (HBE) loads the two 8-bit registers into the first buffer while the LDAC signal loads the second buffer for conversion. The double-buffered input eliminates the generation of spurious analog output values.

MEMORY MAPPED INTERFACE TO 8-BIT μP

Figure 1 shows the timing sequence for operating the HS 9378 with an 8-bit μP bus and Figure 2 shows a general interface. Note that the pinout of the HS 9378 allows the user to run only 8 traces directly underneath the hybrid to connect to the two 8-bit input registers in the first buffer.

The HS 9378 is addressed by the chip select ($\overline{CS}$) signal going low for a minimum of 100 nsec. Since t_{su}, the minimum time required for the input data to be valid before $\overline{CS}$, LBE, or HBE are active, is 0 ns minimum, the $\overline{CS}$ signal can go low simultaneously with data. The low byte enable (LBE) signal going high loads the 8 LSBs into the lower register of the first buffer. After a minimum latch time of 100 nsec, the LBE signal going low latches the data in the lower register. A similar control signal and timing sequence is used to load the 8 MSBs into the upper register of the first buffer (HBE). The load DAC (LDAC) signal going high loads the full 16-bits of data from the first buffer into the second buffer and the D/A for conversion. A minimum latch time of 100 nsec is required for the LDAC signal. The analog output then changes to the new value within the specified settling time. Table 1 is a truth table for the control inputs.

8-BIT BUS INTERFACE



t_{SU}	Setup time required for input data to be valid before $\overline{CS}$, LBE or HBE going active	0 nsec min
t_H	Hold time for $\overline{CS}$ to stay low	100 nsec min
t_L	Latch time for LBE, HBE, and LDAC	100 nsec min
t_{SET}	Settling time from LDAC going active to valid output	
	0.0015% F.S.R., all zeros to all ones	22 μ sec typ
	0.0015% F.S.R., midscale LSB transition	16 μ sec typ

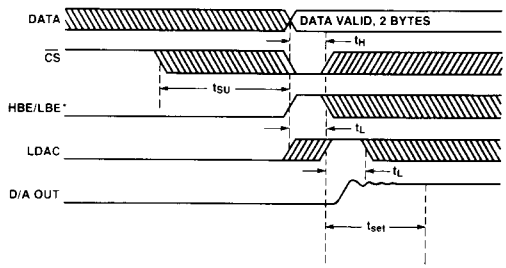
Figure 1. Timing Diagram for Interface to 8-Bit μP Bus

A_7-A_3 ($\overline{CS}$)	A_2 (LDAC)	A_1 (HBE)	A_0 (LBE)	OPERATION
Defined by switches to give low signal to $\overline{CS}$ when 9378 is addressed	0	0	0	All data latched
	0	0	1	Data into low byte of 1st buffer, all others latched
	0	1	0	Data into high byte of 1st buffer, all others latched
	0	1	1	Invalid address
	1	0	0	Data into 2nd buffer (16 bits) and D/A, 1st buffer latched
	1	0	1	Invalid address
	1	1	0	Invalid address
	1	1	1	Data directly to D/A from bus, latches transparent

Table 1. Truth Table — Control Inputs (References Figure 2)

MEMORY MAPPED INTERFACE TO 16-BIT μP

Figure 3 shows the timing sequence for operating the HS 9378 with a 16-bit μP bus and Figure 4 shows a general interface. Table 2 is a truth table for the control inputs. Note that the control inputs are simplified since the HBE and LBE signals can be connected together.



*HBE and LBE are connected together.

Figure 3. Timing Diagram for Interface to 16-Bit μP Bus

A_{15}-A_2 ($\overline{CS}$)	A_1 (LDAC)	A_0 (HBE, LBE)	OPERATION
Defined by switches to give low signal to $\overline{CS}$ when 9378 is addressed	0	0	Data latched
	0	1	Data into 1st buffer, 2nd buffer latched
	1	0	Data into 2nd buffer, 1st buffer latched
	1	1	Data directly to D/A, latches transparent

Table 2. Truth Table — Control Inputs (References Figure 4)

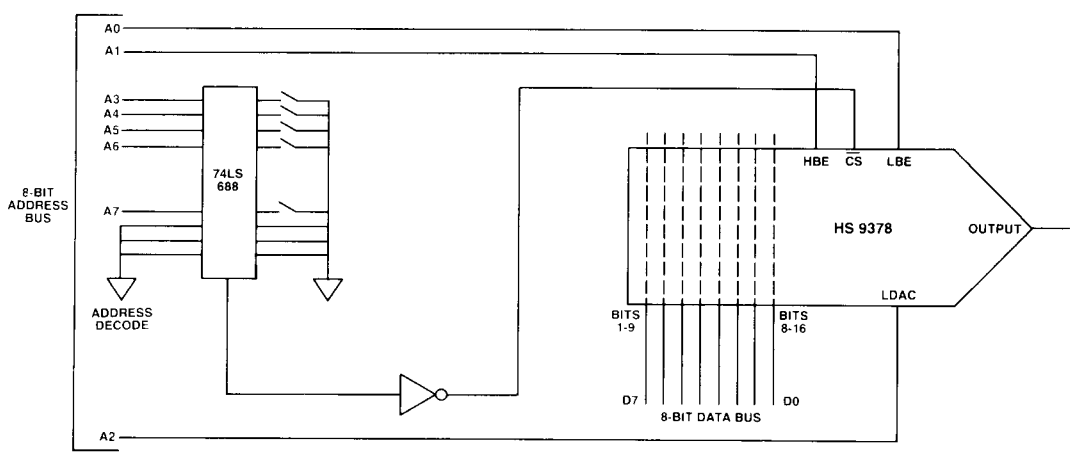


Figure 2. Block Diagram of HS 9378 Interfaced to 8-Bit μP

APPLICATIONS INFORMATION (continued)

MEMORY MAPPED INTERFACE TO 16-BIT μP (continued)

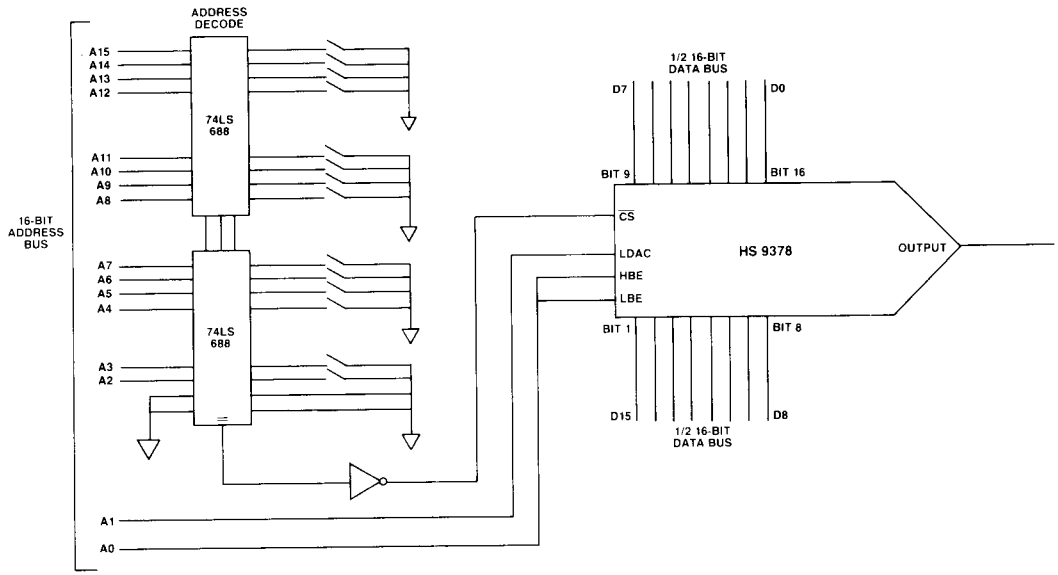


Figure 4. Block Diagram of HS 9378 Interfaced to 16-Bit μP

POWER SUPPLY CONSIDERATIONS

Power supplies used for the HS 9378 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output voltage may result with noisy power sources. It is important to remember that 156 μV is 1 LSB for a 10 volt output.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10 μF tantalum type in parallel with 0.01 μF disc ceramic type.

ADDITIONAL RECOMMENDATIONS

1. For optimum performance, HS 9378 should be allowed sufficient warmup time (5 min.).
2. Due to the small bit weight (156 μV), noise becomes a noticeable factor; therefore, high quality sockets are recommended (if sockets are used) to minimize contact resistance.
3. No digital input should be left floating as the unit will draw excessive current. Unused digital inputs must be tied to a voltage potential of 0V or +5V.
4. If optimum transient and glitch energy performance are required, electrically connect the lid (Case B) to pin 17.
5. If the D/A is driven from a non-buffered or heavily loaded bus, best linearity is obtained by adding 2kΩ pullups to the digital bit inputs.

CONTROL LOGIC

Figure 5 details the control logic function. Note that the LDAC signal is independent of the $\overline{CS}$ signal. All the latches are level controlled as opposed to edge triggered. This allows each of the latches to be operated in a transparent mode by tying the latch control input to a fixed logic "1" level. Since all 3 latches are independent of one another, the sequence of loading the 8 MSBs and the 8 LSBs is reversible.

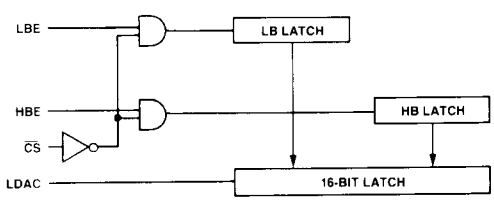


Figure 5. Control Logic Function

LAYOUT CONSIDERATIONS

Due to the small bit weight (156 μV for 1 LSB) special attention must be paid to the layout of the PC-board. To avoid capacitive coupling from digital lines to the hybrid substrate, a ground-plane should be placed directly under the converter package on the component side. This ground-plane can be directly connected to pin 17 of the HS 9378. All digital lines should run on the soldering side of the PC-board.

The pin assignment of the HS 9378 has been arranged so that the 16 digital inputs can be connected to an 8-bit data bus without crossing of bus lines (see Figure 2). In systems with 16-bit data buses, capacitive coupling of the data bus to the HS 9378 can be further reduced by not routing any of the digital lines under the package (see Figure 4).

In general, analog and digital lines should be separated as far as possible and should not run in parallel. If analog and digital lines must cross, they should be at right angles to minimize coupling capacitance. The ground connection to the converter should be made using a wide, low resistive run to minimize voltage drop. If your system distinguishes between analog and digital ground lines, they must be connected at only one point, preferably directly at the converter package. If the connection cannot be made at the package, only the analog ground should be connected to the HS 9378.

TERMINOLOGY

Major Carry Transition Settling: The total elapsed time between the application of a new input code and the point at which the analog output has settled to within a specified error band. The HS 9378 specifies settling to within 0.0015% FSR. For a major carry transition, the change is when the MSB just turns on or off; i.e., when the digital input goes from a "0" and all "1's" to a "1" and all "0's" or vice versa.

Full Scale Transition Settling: The same as major carry transition settling with the exception that the change is a full scale change. For the HS 9378, the change is −10V to +10V, or 20V.

Monotonicity: A monotonic DAC means that the analog output does not decrease as the input is increased or vice versa. The relevant specification is over what temperature range and to what accuracy monotonicity is guaranteed.

CAUTION: ESD (Electro-Static Discharge) sensitive device. Permanent damage may occur when unconnected devices are subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Protective foam should be discharged to the destination socket before devices are removed. Devices should be handled at static safe workstations only. Unused digital inputs must be grounded or tied to the logic supply voltage. Unless otherwise noted, the voltage at any digital input should never exceed the supply voltage by more than 0.5 volts or go below −0.5 volts. If this condition cannot be maintained, limit input current on digital inputs by using series resistors or contact Hybrid Systems for technical assistance.

OUTPUT VOLTAGE RANGE

The HS 9378 can be configured for 3 output ranges: ±10V, ±5V and 0 to 10V. (If unipolar operation is desired, the 20V range is not possible since the output amplifiers saturate at approximately 13V.) Range connections are given in the following chart:

OUTPUT RANGE	PIN 12	PIN 13
±10V	Open	Connect to Pin 11
±5V	Connect to Pin 14	Connect to Pin 11
0 to 10V	Connect to Pin 14	Open (Connect Pin 11 to Main Ground)

LONG TERM DRIFT

Long-term drift of the DAC's transfer function, after initial trim of offset and gain, is composed of several factors which are discussed below.

a. **Offset Drift.** For maximum performance, the offset should be zeroed after at least one hour of operation. Then the offset drift will be typically 200 V for the first 1000 hrs; and 100 V per 1000 hrs thereafter.

b. **Reference Voltage Drift.** The intrinsic long-term drift of the breakdown voltage of the temperature compensated zener-diode in the reference voltage circuitry will cause a gain error at the output of the DAC. The drift that will occur is typically less than 1mV per year. A correction of this drift error can be made using the gain adjustment circuitry.

c. **Output Amplifier Gain Change.** Any noticeable gain change will be caused by a drift of the internal feedback resistor relative to the DAC's network impedance. This can contribute 10ppm F.S.R./1000 hrs. which can be corrected using the gain circuitry.

d. **Linearity Drift.** Due to the unique circuitry used in the DAC network, effects of resistor accuracy drift on linearity are greatly reduced. Typical differential linearity drift is less than 3ppm F.S.R./1000 hrs.

ORDERING INFORMATION

MODEL	MONOTONICITY (over temp.)	TEMPERATURE RANGE
HS 9378C	15 bits	0°C to +70°C
HS 9378TB	15 bits	−55°C to +125°C
HS 9378SB	14 bits	−55°C to +125°C

NOTE: Contact factory for serial input version or for voltage MDAC version.