73M2901C/5V
V.22bis Single Chip Modem

DATA SHEET

JULY 2005

DESCRIPTION

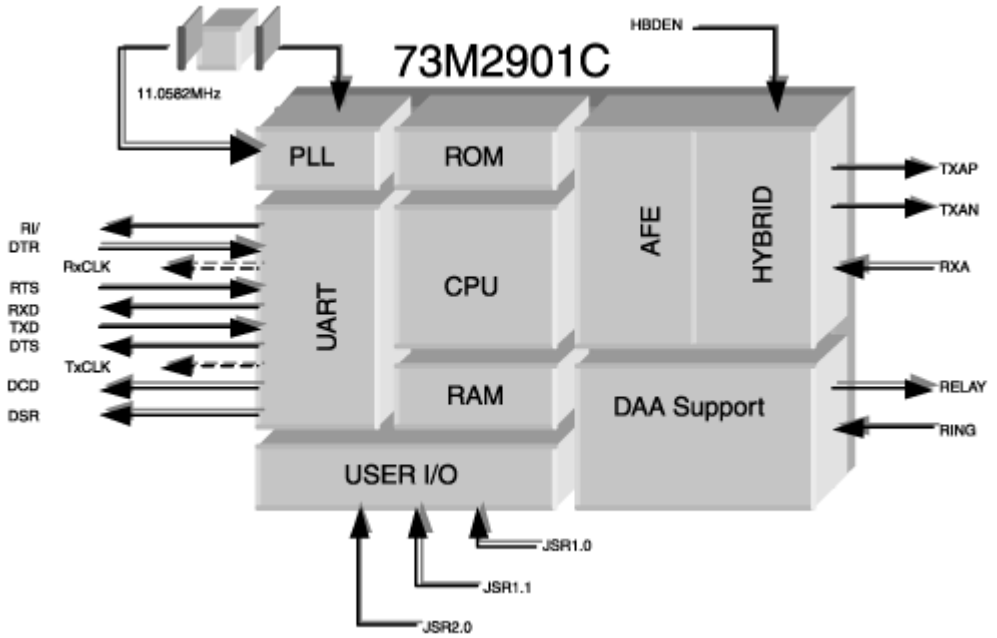
The 73M2901C/5V is a single-chip modem that combines all the controller (DTE) and data pump functions necessary to implement an intelligent V.22bis data modem. This device is based on TERIDIAN Semiconductor's implementation of the industry standard 8032 microcontroller core with a proprietary multiply and accumulate (MAC) coprocessor; Sigma-Delta A/D and D/A converters; and an analog front end. The ROM and RAM necessary to operate the modem are contained on the device. Additionally, the 73M2901C/5V provides an on-chip oscillator and Hybrid driver.

The 73M2901C/5V is a high performance, low voltage, low power, single chip modem capable of data transmission and reception through 2400bps. The 73M2901C/5V is intended for embedded applications and battery operation. This device offers options for a low power conventional 5-volt design with optional internal hybrid and country specific call progress support.

FEATURES

- **True one chip solution for embedded systems**
- **Low operating power (~250mW @ 5V, with standby and power down mode available)**
- **Designed for +5 volts (+/-10%)**
- **Data speeds:**
  - **V.22bis – 2400bps**
  - **V.22/Bell 212 – 1200bps**
  - **V.21/Bell 103 – 300bps**
  - **V.23 – 1200/75bps (with PAVI turnaround)**
  - **Bell 202 – 1200bps**
  - **Bell 202/V23 4-wire operations**
- **International Call Progress Support (FCC68, CTR21, JATE…)**
- **Host access to modem port pins via AT commands for custom I/O expansion**
- **DTMF tone generation and detection**
- **On chip optional hybrid driver**
- **Worldwide Caller ID capability**
- **Blacklisting capability**
- **Line-In-Use and Parallel Pick-Up (911) detection capability**
- **Manufacturing Self Test capability**
- **Packaging: 32 pin PLCC or 44 pin TQFP**

BLOCK DIAGRAM



HARDWARE DESCRIPTION

The 73M2901C/5V is designed for a single +5 volt supply with low power consumption (~250mW @ 5 volts). The modem supports automatic standby idle mode. The modem will also accept a request to power down from the DTE via hardware control. No additional major components are required to complete the modem core logic. The modem provides direct firmware LED support via port pins.

HARDWARE FEATURES

- Fully self-contained. "AT" Command interpreter and data pump
- User pin available
- Synchronous serial data I/O available
- Asynchronous serial port
- On-chip hybrid driver.
- Autobaud capability from 300bps to 9600bps

POWER SUPPLY

Power is supplied to the 73M2901C/5V via the VPD and VPA pins. The 73M2901C/5V is designed for a single +5 (+/-10%) volt supply and for low power consumption (~250mW @ 5 volts). Ground Reference is provided at the VND and VNA pins.

LOW POWER MODE

The TERIDIAN 73M2901C/5V supports a low power mode. If the low power standby option is enabled the 73M2901C/5V will go into a power saving mode when idle. The oscillator will be running, clocks will be supplied to the UART, timers and interrupt blocks; but no clocks will be supplied to the CPU. Instruction processing and activity on the internal busses is halted. Normal operation is resumed when an interruption such as $\overline{\text{DTR}}$, $\overline{\text{RING}}$ or $\overline{\text{ASRCH}}$ (any character send to the 73M2901C/5V) is requested or when a reset occurs.

ANALOG LINE / HYBRID INTERFACE

The 73M2901C/5V provides a differential analog output (TXAP and TXAN) and a single-ended analog input (RXA) with internal A/D and D/A converters. A driver is provided for an internal hybrid function.

The internal hybrid driver is capable of driving an external load matching impedance and a line-coupling transformer. If an external hybrid is to be used, the on-chip hybrid drivers can be reconfigured to drive a minimum load of 50kΩ and thus reduce the driver's power consumption.

The hybrid configuration is controlled by the state of the HBDEN pin. For driving a line-coupling transformer, HBDEN should be pulled high. For driving an external hybrid (load on TXAP and TXAN is 50kΩ or larger), HBDEN should be pulled low.

The 73M2901C/5V provides firmware control for a hook relay driver ($\overline{\text{RELAY}}$) as well as interrupt support for a ring detect opto-coupler ($\overline{\text{RING}}$).

INTERRUPT PINS

The external interrupt sources, $\overline{\text{DTR}}$, $\overline{\text{ASRCH}}$ and $\overline{\text{RING}}$, come from dedicated input pins of the same name.

$\overline{\text{DTR}}$ informs the 73M2901C/5V that the host has requested the 73M2901C/5V perform a specific function. The actual particulars of that function can be changed by "AT" commands (described in full in the TERIDIAN 73M2901C User's Guide).

$\overline{\text{RING}}$ informs the 73M2901C/5V that the external DAA circuitry has detected a ring signal.

CRYSTAL OSCILATOR

The TERIDIAN 73M2901C/5V single chip modem can use an external 11.0592 MHz reference clock or can generate such a clock using only a crystal and two capacitors. If an external clock is used, it should be applied to OSCIN.

SPECIFYING A CRYSTAL

The manufacturer of a crystal resonator verifies its frequency of oscillation in a test set-up, but to ensure that the same frequency is obtained in the application, the circuit conditions must be the same. The TERIDIAN 73M2901C/5V modem requires a parallel mode (antiresonant) crystal, the important specifications of which are as follows:

Mode:	Parallel (antiresonant)
Frequency:	11.0592 MHz
Frequency tolerance:	±50 ppm at initial temperature.
Temperature drift:	±50 ppm additional over full Range.
Load capacitance:	18pF or 20pF
ESR:	75Ω max.
Drive level:	Less than 1mW.

RESET

A reset is accomplished by holding the RESET pin high. To ensure a proper power-on reset, the reset pin must be held high for a minimum of 3μs. At power on, the voltage at VPD, VPA, and RESET must come up at the same time for a proper reset. The signals $\overline{DCD}$, $\overline{CTS}$, and $\overline{DSR}$ will be held inactive for 25ms, acknowledging the reset operation within a 250ms time window after the reset triggerring event. The 73M2901C/5V is ready for operation after that 250ms window and/or after the signals $\overline{DCD}$, $\overline{CTS}$, and $\overline{DSR}$ become active.

ASYNCHRONOUS AND SYNCHRONOUS SERIAL DATA INTERFACE

The serial data interface consists of the TXD and RXD data paths (LSBit shifted in and out first, respectively); and the TXCLK and RXCLK serial clock outputs associated with the data pins; $\overline{CTS}$/$\overline{RTS}$ flow control; $\overline{DCR}$, $\overline{DSR}$ and $\overline{DTR}$. In synchronous mode, the data is passed at the bit rate (tolerance is +1%, -2.5%).

PIN DESCRIPTIONS

POWER PIN DESCRIPTION

PIN NAME	32-PIN	44-PIN	TYPE	DESCRIPTION
VPA	15	16	I	Positive analog voltage (+ Analog Supply)
VNA	21	22	I	Negative analog voltage. (Analog Ground)
VPD	6, 25, 29	2,12, 27, 33	I	Positive digital voltage (+ Digital Supply)
VND	5, 22, 26	11, 24, 44, 28	I	Negative digital voltage. (Digital Ground)

ANALOG INTERFACE PIN DESCRIPTION

PIN NAME	32-PIN	44-PIN	TYPE	DESCRIPTION
RXA	20	21	I	Receive analog data
TXAN	16	17	O	Transmit Analog -
TXAP	17	18	O	Transmit Analog +
HBDEN	14	15	I	2w/4w hybrid driver enable pin 0 = Driver configured for 50kΩ or greater load (Tie to VND) 1 = Driver configured for driving line-coupling transformer (Tie to VPD)
VBG	19	20	O	Analog Band Gap voltage reference pin (0.1μF to VNA)
VREF	18	19	O	Analog reference voltage pin (0.1μF to VNA)

EXTERNAL INTERRUPTS PIN DESCRIPTIONS

PIN NAME	32-PIN	44-PIN	TYPE	DESCRIPTION
$\overline{RING}$	2	39	I	External interrupt – Line interface ring detection circuitry input
$\overline{DTR}$	32	37	I	External interrupt – DTE DTR signal input

PIN DESCRIPTIONS (continued)

OSCILLATOR PIN DESCRIPTION

PIN NAME	32-PIN	44-PIN	TYPE	DESCRIPTION
OSCIN	24	26	I	Crystal input for internal oscillator, also input for external source.
OSCOUT	23	25	O	Crystal oscillator output.

DIGITAL INTERFACE PIN DESCRIPTION

PIN NAME	32-PIN	44-PIN	TYPE	DESCRIPTION
RESET	13	9	I	Resets 73M2901C/5V
RXCLK	31	36	O	Receive Data Synchronous Clock
RXD	30	35	O	Serial output to DTE.
TXCLK	28	31	O	Transmit Data Synchronous Clock
TXD	27	30	I	Serial data input from DTE.
USR10	12	8	I/O	This pin can optionally be configured as an active low detect pin. This can be used to implement such functions as “parallel-pick-up”, “line-in-use”, or “seize” detect.
USR11	11	7	I/O	Programmable I/O port. This pin can ooptionnaly be used to control an external switch for Caller ID decoding operations.
$\overline{\text{RTS}}$ (USR12)	10	6	I	Request to Send
$\overline{\text{CTS}}$ (USR13)	9	5	O	Clear to Send
$\overline{\text{DSR}}$ (USR14)	8	4	O	Data Set Ready
$\overline{\text{DCD}}$ (USR15)	7	3	O	Data Carrier Detect
$\overline{\text{RI}}$ (USR16)	4	43	O	Ring Indicator
$\overline{\text{RELAY}}$ (USR17)	3	40	O	Relay driver output
USR20	1	38	I/O	Programmable I/O port

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum rating may permanently damage the device.

PARAMETER	RATING
Supply Voltage	-0.5V to +7.0V
Pin Input Voltage	-0.5V to VPD + 0.5V
Storage Temperature	-55ºC to 150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply Voltage	+5.0V (+/-10%)
Oscillator Frequency	11.0592MHz +/- 50ppm
Operating Temperature	-40°C to +85°C

TRANSMITTER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ITU Guard Tone Power	550Hz (relative to carrier) 1800Hz (relative to carrier)	-5 -8	-3.5 -6.5	-2 -5	dB dB
Calling Tone transmit power	1300Hz		-11.5		dBm0[1]
Answer Tone transmit power	2225/2100Hz		-11		dBm0[1]
Transmit tolerance, all tones and carriers		-1.2		1.2	dB

[1] dBm0 refers to the TERIDIAN recommended line interface (8dB loss from Transmit pins to the line and 5dB loss from the line to the Receive pin). Results may vary depending on selected DAA. 0dBm = $0.775V_{rms}$. dBm = 10log {$Vrms^2$/[(1mW)(600Ω)]}

ELECTRICAL SPECIFICATIONS (continued)

TRANSMITTER

NOMINAL TRANSMIT LEVELS	CONDITIONS	MAX	UNIT
QAM	Vref=1.25V, S73=48	-13.3	dBm0[1]
	Vref=2.25V, S73+128	-8.3	dBm0[1]
DPSK	Vref=1.25V, S73=48	-13.3	dBm0[1]
	Vref=2.25V, S73+128	-8.3	dBm0[1]
FSK	Vref=1.25V, S73=48	-11	dBm0[1]
	Vref=2.25V, S73+128	-6	dBm0[1]
DTMF (HIGH TONE)	Vref=1.25V, S92=4	-11.5	dBm0[1]
	Vref=2.25V, S92+2	-6.5	dBm0[1]
DTMF (HIGH TONE)	Vref=1.25V, S92=4	-13	dBm0[1]
	Vref=2.25V, S92+2	-8	dBm0[1]
DTMF (HIGH TONE)	Vref=1.25V, S92=4	-6.7	dBm0[1]
	Vref=2.25V, S92+2	-1.7	dBm0[1]

ELECTRICAL SPECIFICATIONS (continued)

TRANSMITTER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Gain Adjust Tolerance	By step (ATS13)	-0.3	0	0.3	DBm0[1]
TX boost, carrier or DTMF	ATS73+128 or ATS92+2	4.7	5.0	5.3	dB
Total Harmonic Distortion (THD)	1kHz sine wave at output (TXAP-TXAN) 1.5Vpk(2.7dBm) for Vref=1.25V 2.4Vpk (6.8dBm) for Vref=2.25V THD = 2nd and 3rd harmonic.			-50	dB
Intermod Distortion	At output (TXAP-TXAN) 1.0kHz, 1.2 kHz sine waves summed 2.0Vpk for Vref=1.25V 2.4Vpk for Vref=2.25V	each unwanted frequency component		-33	dB
	Refer to CTR21 specification for complete description of requirements	sum of unwanted frequency components in pass band		-20	dB below low tone
Power Supply Rejection Ratio	-30 dBm signal at VPA 300Hz – 30kHz. Measured TXAP to TXAN.			30.0	dB

RECEIVER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Carrier Detect On	Tip and Ring			-43.0	dBm0[1]
Carrier Detect Off	Tip and Ring	-48.0			dBm0[1]
Carrier Detect Hysteresis	Tip and Ring		2.0		dB
Receive Level	Tip and Ring	-43.0		-9.0	dBm0[1]
Idle Channel Noise	0.2kHz - 4.0kHz		-70	-65	dB

ELECTRICAL SPECIFICATIONS (continued)

RECEIVER (continued)

PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNITS
Input Impedance	RXA	150	---	---	kΩ
Receive Gain Boost	SFR 96h bit 2 (Rxgain) = 1	17.75		20.75	dB
Maximum Input Level at RXA	VREF=1.25V			0.587	Vpk
	VREF=2.25V			1.069	Vpk
Total Harmonic Distortion (THD)	1kHz 450mV-pk on RXA THD = 2nd and 3rd harmonic.		-70	-50	dB

DC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	NOM	MAX	UNIT
Input Low Voltage (Except OSCIN,RESET)	VIL		-0.5		0.2Vcc	V
Input Low Voltage OSCIN,RESET	VIL		-0.5		0.2 Vcc	V
Input High Voltage (Except OSCIN,RESET)	VIH		0.5 Vcc		Vcc + 0.5	V
Input High Voltage OSCIN,RESET	VIH		0.7 Vcc		Vcc + 0.5	V
Output Low Voltage (Except OSCOUT)	VOL	IOL = 4mA			0.45	V
Output Low Voltage OSCOUT	VOLOSC	IOL = 3.0mA			0.7	V
Output High Voltage (Except OSCOUT)	VOH	IOH = -4mA	Vcc – 0.45			V
Output High Voltage OSCOUT	VOHOSC	IOH =-3.0mA	Vcc – 0.9			V
Input Leakage Current (Except OSCIN)	IIH	Vss < Vin < Vcc			1	µA
Input Leakage Current OSCIN	IIH	Vss < Vin < Vcc	1		30	µA

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN	NOM	MAX	UNIT
5V Operations						
Maximum Power Supply Normal Operation @ 5V HBDEN pulled high	IDD1	30pF/pin		51	62	mA
Maximum Power Supply Normal Operation @ 5V HBDEN pulled low	IDD1	30pF/pin		35	43	mA
Maximum Digital Power Supply @ 5V	IDDd	30pF/pin		31	37	mA
Maximum Analog Power supply @ 5V HBDEN pulled high	IDDah1	30pF/pin		20	25	mA
Maximum Analog Power Supply @ 5V HBDEN pulled low	IDDah0	30pF/pin		4	6	mA
Maximum Power Supply Idle Mode @ 5V	IDD2	30pF/pin		11	15	mA
Maximum Power Supply Power Down Mode @ 5V	IDD3	30pF/pin		4	10	µA

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Vbg	Vcc=5V	1.19	1.25	1.31	V
Vref	Vcc=5V – no boost	1.19	1.25	1.31	V
Vref	Vcc=5V + internal boost	2.14	2.25	2.36	V

FIRMWARE DESCRIPTION[2]

An "AT" command interpreter provides command and configuration of the 73M2901C/5V. This provides the user a uniform interface to control the modem in embedded applications.

The signal processing is performed by obtaining data from and providing data to the integrated A/D converter. A MAC hardware processor is provided for computation.

To provide maximum flexibility, the system host processor can access the internal RAM and Control Register space in the modem. This will allow the OEM user to modify parameters such as filter response, transmit levels through the AT command set using proprietary commands. The host processor can also access the modem I/O port pins, providing extended I/O capability.

FIRMWARE REQUIREMENTS

The modem always powers up in the idle (on hook) mode. "AT" commands are issued via the serial interface from the host. All modem configuration commands are received in this manner. The data modem firmware is contained in an internal ROM. The firmware will automatically enter a power saving idle mode if the modem is on hook and there are no incoming host commands. The modem automatically powers up upon receiving the next command. This power up sequence occurs without delay to the host. This function, while saving power, is transparent to the host processor and can be disabled by the host via an "AT" command. The host can also program the modem to power down via external pin ($\overline{DTR}$) or via a firmware command.

FIRMWARE FEATURES

- "AT" command set
- Supports data standards through V.22bis
- Provides DAA control firmware (e.g. ring detect, hook control, line in use detection support)
- Multinational Call progress support (FCC68, CTR21, JATE…)
- Caller ID capability
  - *FSK demodulation (V23 or Bell202)*
  - *DTMF Demodulation*
  - *Intra 1st/2nd ring CID data operations*
  - *Post Line reversal CID data operations*
- Interfaces with standard V.24/EIA-232 (5 volt inverted level) serial interface using the built in serial port and firmware control of port pins
- Provides tone generation and detection, four imprecise and four precise call progress detect filters
- On hook Line-In-Use detection support (No line seizure will occur when a Line-In-Use condition is detected)
  - *Tip/Ring voltage sensing*
  - *Quiescent line validation*
- Off hook Parallel Pick-Up detection support (line seizure will be aborted as soon as a Parallel Pick-Up condition is detected)
  - *Loop current variation sensing*
- Host access to program RAM provided
- User access to modem functions
- Bell 212A fast connect

[2] For a detailed description of the firmware consult the TERIDIAN 73M2901C User's Manual.

DESIGN CONSIDERATIONS

TERIDIAN Semiconductor's single chip modem solutions include all the basic modem functions. This makes these devices adaptable to a variety of applications.

Unlike digital logic circuitry, modem designs must contend with precise frequency tolerances and verify low-level analog signals, to ensure acceptable performance. Using good analog circuit design practices will generally result in a sound design. The crystal oscillator should be held to a 50ppm tolerance. Following are additional recommendations that should be taken into consideration when starting new designs.

LAYOUT CONSIDERATIONS

Good analog/digital design rules must be used to control system noise in order to obtain high performance in modem designs. The more digital circuitry present in the application, the more attention to noise control is needed.

High speed, digital devices should be locally bypassed, and the telephone line interface and the modem should be located next to each other near where the telephone line connection is accessed. It is recommended that power supplies and ground traces should be routed separately to the analog and digital portions on the board. Digital signals should not be routed near low-level analog or high impedance analog traces.

The 73M2901C/5V should be considered a high performance analog device. A 10μF electrolytic capacitor in parallel with a 0.1μF Ceramic capacitor should be placed between VPD and VND as well as between VPA and VNA. A 0.1μF ceramic capacitor should be placed between VREF and VNA as well as VBG and VNA. Use of ground planes and large traces on power is recommended.

The 73M2901C/5V is the first of a series of parts with different and/or additional features. In order to insure full lay out compatibility for all the series, it is recommended to implement three additional resistors in the schematics as shown in the recommended schematics arrangement (R11, R12 and R13).

73M2901 DESIGN COMPATIBILITY

The TERIDIAN 73M2901C/5V is an enhanced version of the 73M2901/5V and has a number of new features. Although the two parts are highly compatible, specialattention should be paid when changingan existing 73M2901 design to use the 73M2901C. From a hardware standpoint, the key differences involve the User I/O pins USR10 and USR11, and the $\overline{\text{ASRCH}}$ pin which has been removed and replaced by USR20 in the 73M2901C. I an existing 73M2901 design, the USR20 pin of the 73M2901C can safely be connected to TXD as long as no modification on the user I/O is performed by the host software (S103, S104). The functions of USR10 and USR11 are related to Caller ID and Line_In_Use/Parallel Pick-Up support.

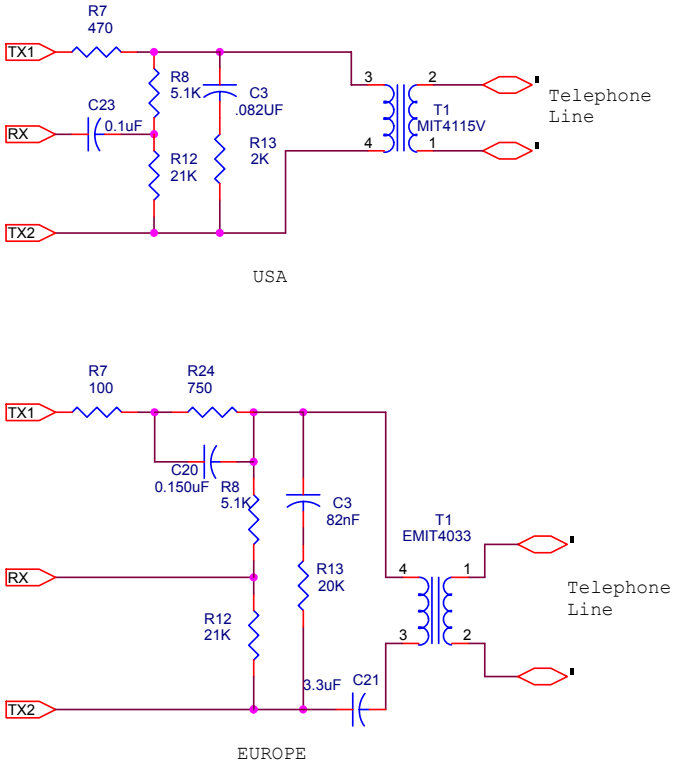
Software enhancements to the 73M2901C are typically achieved by the addition of new AT commands and so the device can be considered a superset of the 73M2901. However, the user should check all AT commands and register settings for compatibility with the intended application (refer to the TERIDIAN 73M2901C User Guide for complete details).

TELEPHONE LINE INTERFACE

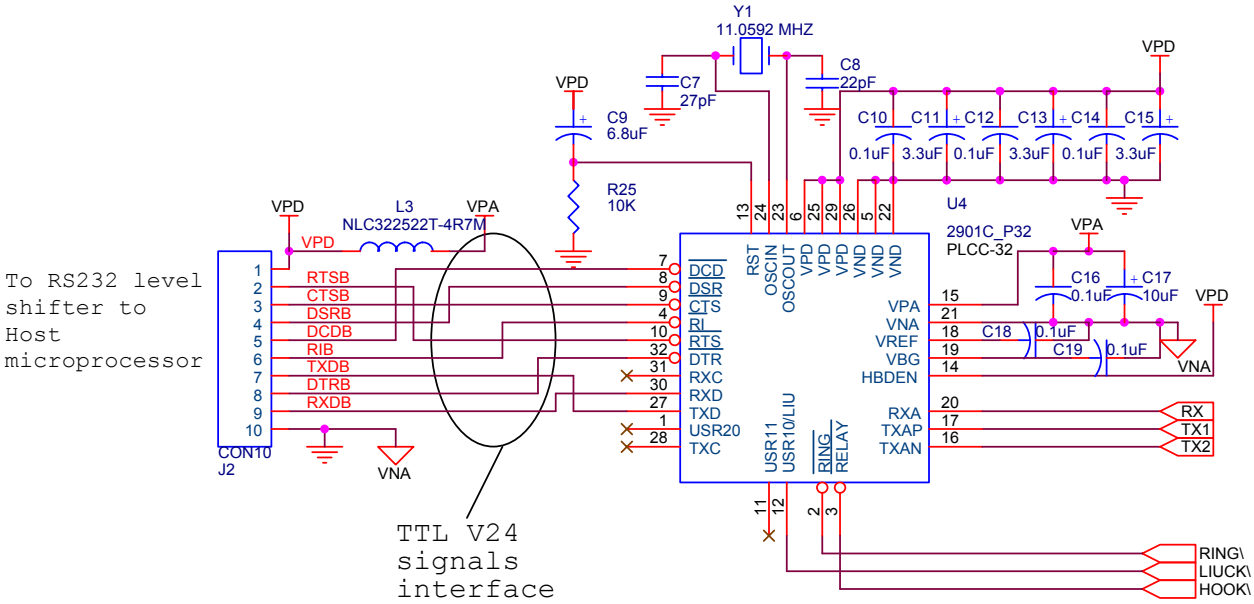
Transmit levels at the line are dependent on the interface used between the pins and the line. In order to save having to provide external op-amps to drive the line coupling transformer, the analog outputs (TXAP and TXAN) have the capability to be used as the hybrid drivers for connecting to the transformer directly (with the required impedance matching series resistor). Used in this configuration, there is loss associated in both the receive path and transmit path.

The line interface circuit shown on the following page represents the basic components and values[3] for interfacing the TERIDIAN 73M2901C/5V analog pins to the telephone line.

[3] TERIDIAN 73M2901C Demo boards use the line interface shown on the following page. Other designs may have different requirements and thus will require different component values or a different configuration. With the shown configuration, there is approximately an 8dB loss in the transmit path, and approximately a 5dB loss in the receive path.

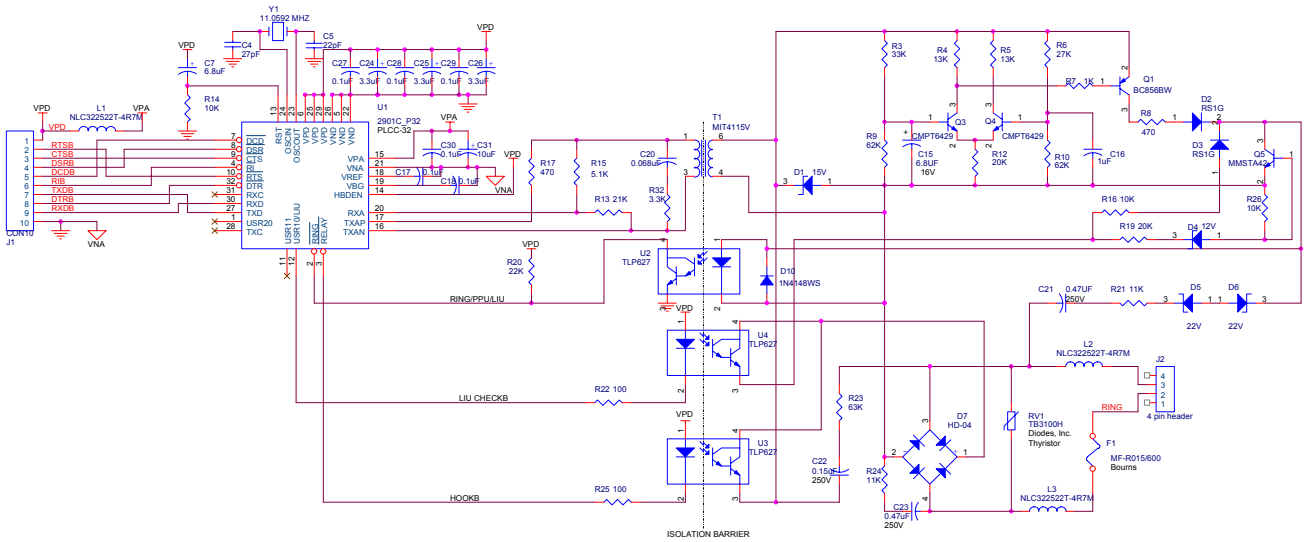


Recommended Line Interfaces



Recommended Schematics Arrangement

TYPICAL USA APPLICATION SCHEMATICS



MODEM PERFORMANCE CHARACTERISTICS

The curves presented in this data sheet define modem IC performance under a variety of line conditions typical of those encountered over public service telephone lines.

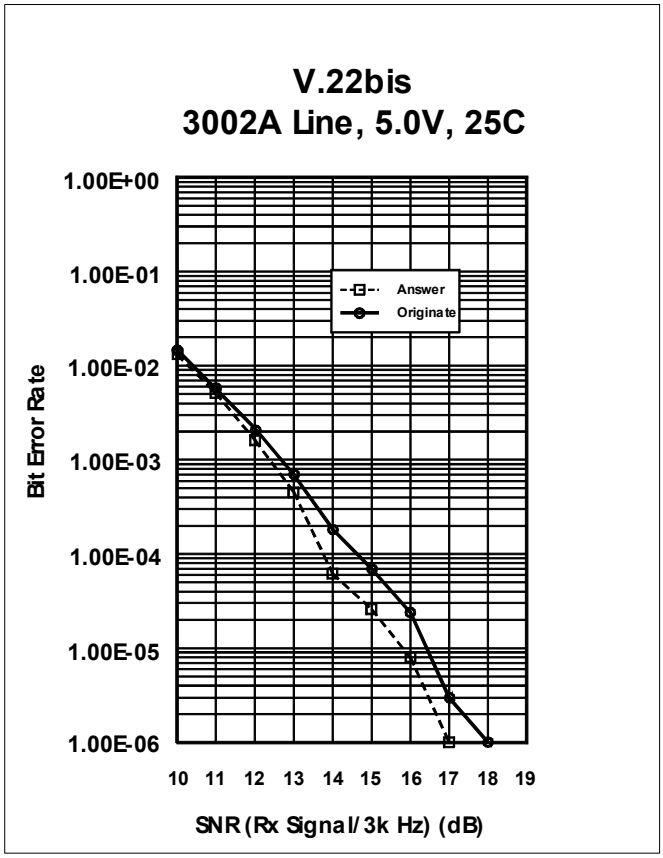
BER VS. SNR

This test represents the ability of the modem to operate over noisy lines with a minimum amount of data transfer errors. Since some noise is generated in the best dial up lines, the modem must operate with the lowest signal to noise ratio (SNR) possible. Better modem performance is indicated by test curves that are closest to the BER axis. A narrow spread between curves representing the four line parameters indicates minimal variation in performance while operating over a range of aberrant operating conditions. Typically a DPSK modem will exhibit better BER performance test curves receiving in the low band (answer mode) than in the high band (originate mode).

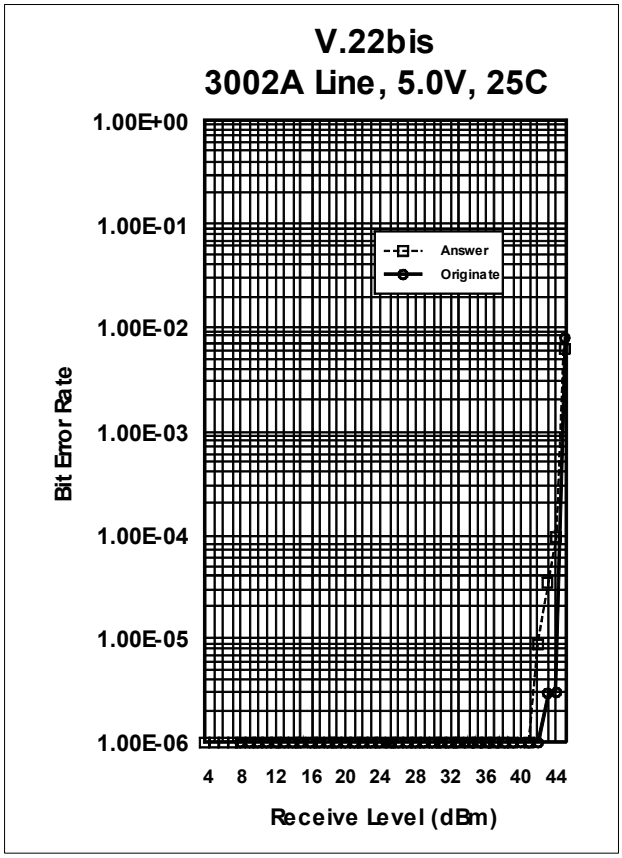
BER VS. RECEIVE LEVEL

This test measures the dynamic range of the modem. Because signal levels vary widely over dial up lines, the widest possible dynamic range is desirable. The SNR is held constant at the indicated values as the Receive level is lowered from very a very high to a very low signal level. The width of the bowl of these curves, taken at the BER point is the measure of the dynamic range.

BER VS SNR



BER VS RECEIVE LEVEL



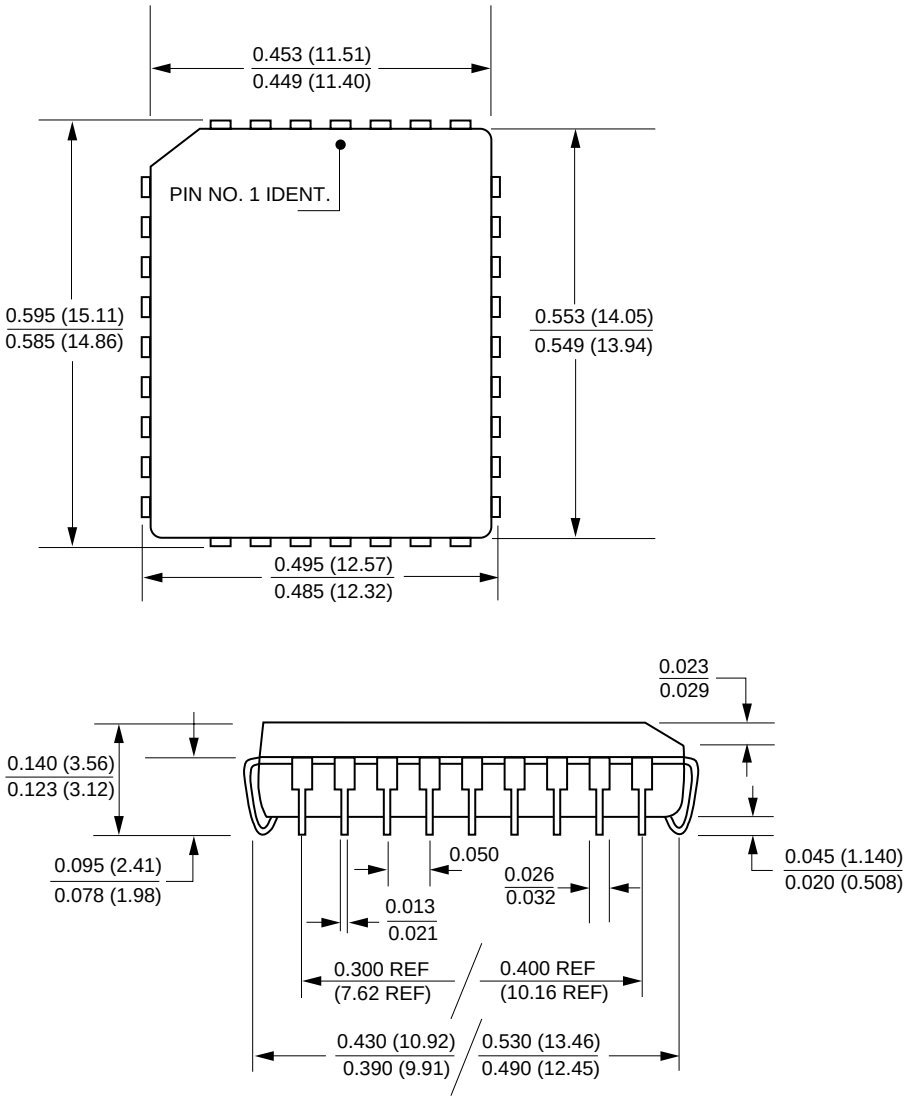
32 PIN PLCC PIN-OUT

PIN	PIN NAME	PIN	PIN NAME
1	USR20	17	TXAP
2	$\overline{\text{RING}}$	18	VREF
3	$\overline{\text{RELAY}}$	19	VBG
4	$\overline{\text{RI}}$	20	RXA
5	VND	21	VNA
6	VPD	22	VND
7	$\overline{\text{DCD}}$	23	OSCOUT
8	$\overline{\text{DSR}}$	24	OSCIN
9	$\overline{\text{CTS}}$	25	VPD
10	$\overline{\text{RTS}}$	26	VND
11	USR11	27	TXD
12	USR10	28	TXCLK
13	RESET	29	VPD
14	HBDEN	30	RXD
15	VPA	31	RXCLK
16	TXAN	32	$\overline{\text{DTR}}$

44 PIN TQFP PIN-OUT

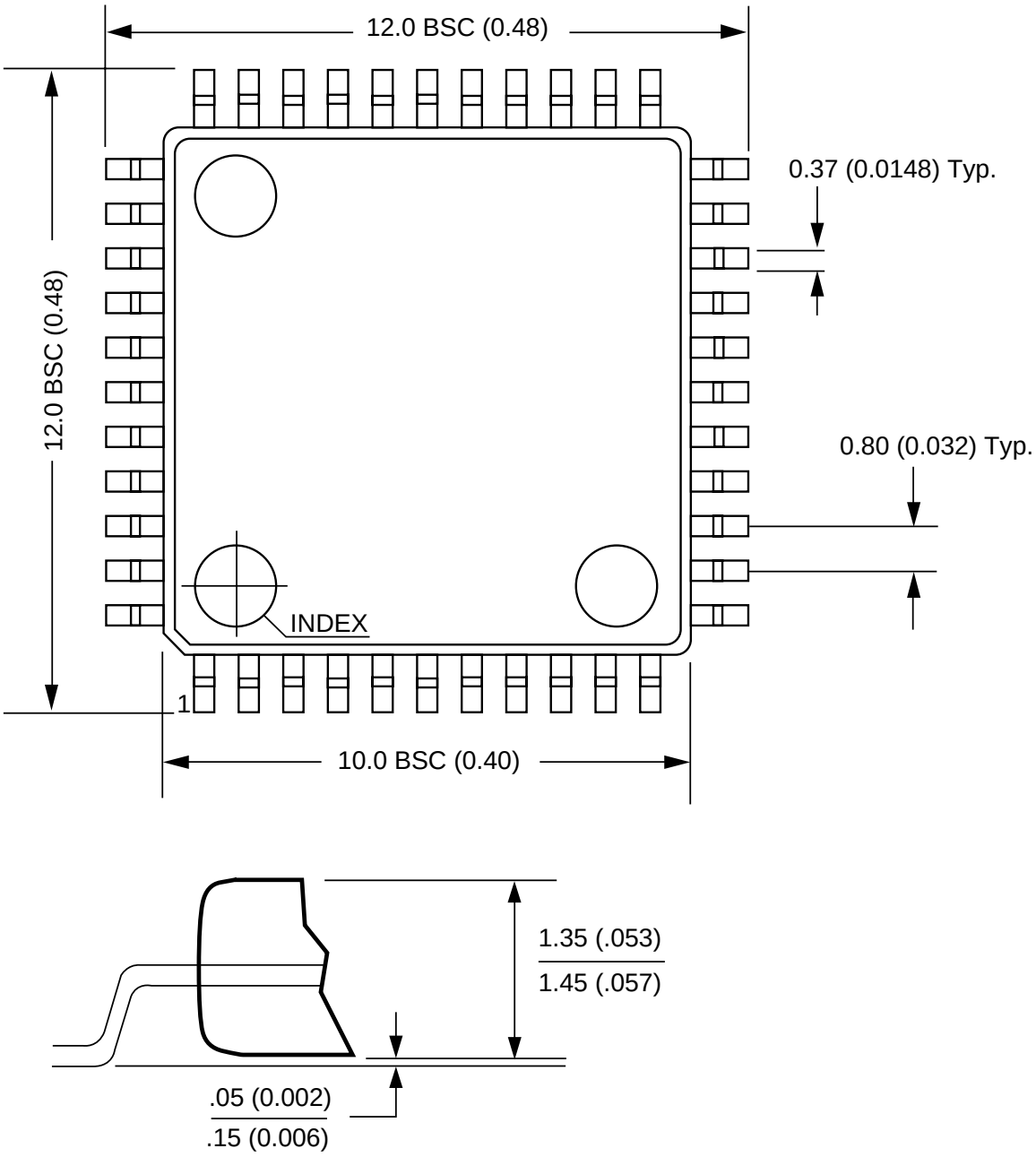
PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
1	N/C	12	VPD	23	N/C	34	N/C
2	VPD	13	N/C	24	VND	35	RXD
3	$\overline{\text{DCD}}$	14	N/C	25	OSCOUT	36	RXCLK
4	$\overline{\text{DSR}}$	15	HBDEN	26	OSCIN	37	$\overline{\text{DTR}}$
5	$\overline{\text{CTS}}$	16	VPA	27	VPD	38	USR20
6	$\overline{\text{RTS}}$	17	TXAN	28	VND	39	$\overline{\text{RING}}$
7	USR11	18	TXAP	29	N/C	40	$\overline{\text{RELAY}}$
8	USR10	19	VREF	30	TXD	41	N/C
9	RESET	20	VBG	31	TXCLK	42	N/C
10	N/C	21	RXA	32	N/C	43	$\overline{\text{RI}}$
11	VND	22	VNA	33	VPD	44	VND

MECHANICAL DRAWINGS



32-Pin PLCC

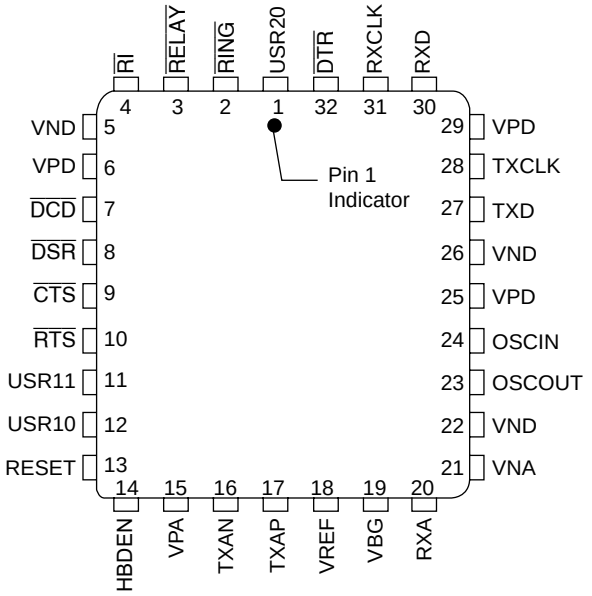
MECHANICAL DRAWINGS (continued)



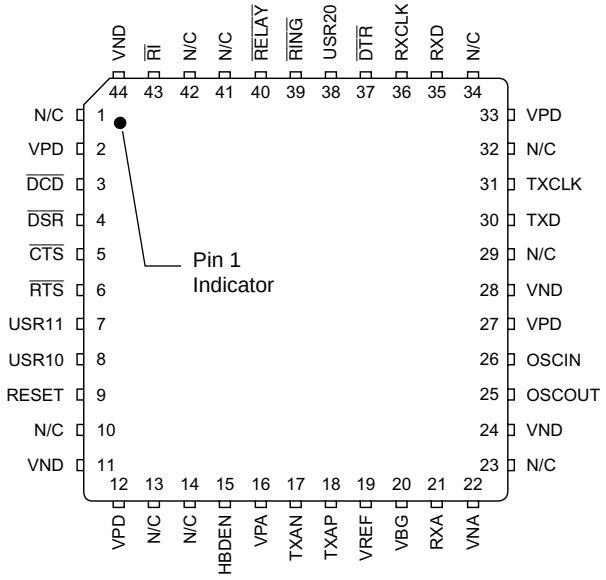
44-Pin TQFP (JEDEC LQFP)

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



32-Lead PLCC
73M2901C-32IH/5



44-Pin TQFP
73M2901C-IGT/5

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGING MARK
73M2901C 32-Pin Plastic Leaded Chip Carrier	73M2901C/5V-32IH	73M2901C-32IH
73M2901C 44-Pin Thin Quad Flat Pack	73M2901C/5V-IGT	73M2901C-IGT

TERIDIAN Semiconductor Corp., 6440 Oak Canyon Rd., Irvine, CA 92618-5201, (714) 508-8800, FAX (714) 508-8877, www.teridiansemi.com

 07/15/05 Rev 3.0