Serial Scan Shadow Register — L29C818

FEATURES

- Octal Register with Additional 8-bit Shiftable Shadow Register
- Serial Load/Verify of Writable Control Store RAM
- Serial Stimulus/Observation of Sequential Logic
- High Speed, Low Power CMOS Technology
- Available 100% Screened to MIL-STD-883, Class B
- Plug Compatible with AMD Am29818
- Package Styles Available:
  - 24-pin Plastic DIP
  - 24-pin Sidebraze, Hermetic DIP
  - 28-pin Ceramic LCC

DESCRIPTION

The **L29C818** is a high-speed octal register designed especially for applications using serial-scan diagnostics or writable control store. It is pin and functionally compatible with the AMD Am29818 bipolar device.

The L29C818 consists of an octal register (the "P" register), internally connected to an 8-bit shift register (the "S" register). Each has its own corresponding clock pin, and the P register has a three-state output control.

An input control signal MODE, in combination with the S register serial data input (SDI) pin controls data routing within the L29C818. When the MODE input is low, indicating normal operation, data present on the D7–D0 pins is loaded into the P register on the rising edge of CLK P. The contents of the P register are visible on the output pins Y7–Y0 when the $\overline{OE}$ control line is low.

Also, data present on the SDI pin is loaded into the least significant position of the S register on the rising edge of CLK S. In this mode, the S register performs a right shift operation, with the contents of each bit position replaced by the value in the next least significant location. The value in S7 is shifted out on the serial data output (SDO) pin. The SDI and SDO pins allow serial connection of multiple L29C818 devices into a diagnostic loop. When MODE is low, the operation of the P and S registers are completely independent and no timing relationship is enforced between CLK P and CLK S.

When MODE is high, the internal multiplexers route data between the S and P registers, and the Y port. The contents of the S register are loaded into the P register on the rising edge of CLK P. In diagnostic applications,

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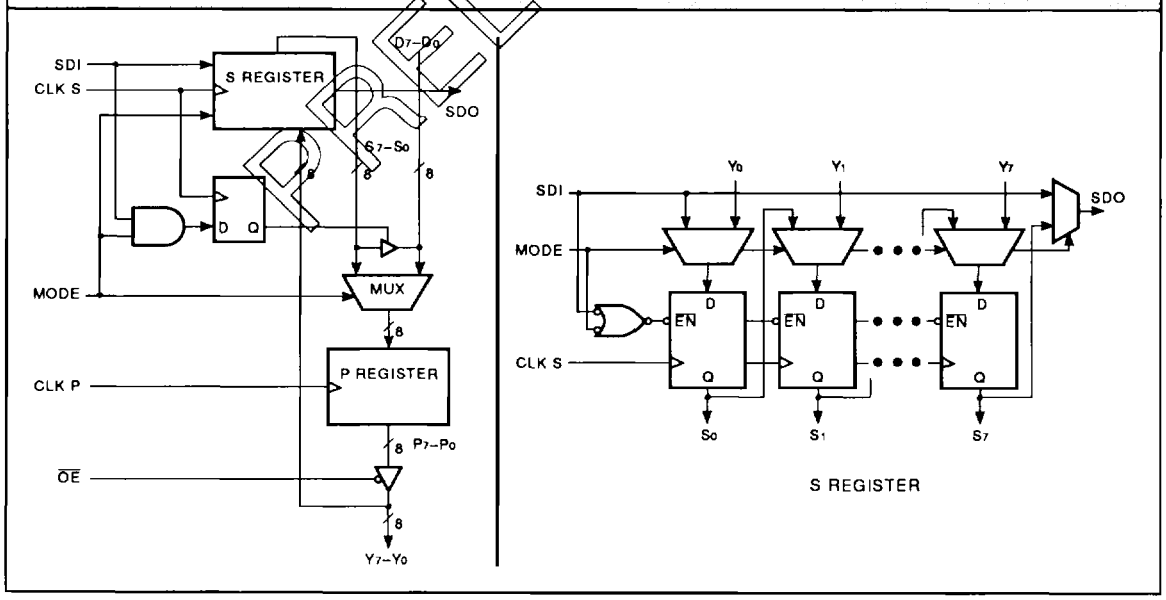
L29C818 Block Diagram



this allows a data value input via serial scan to be loaded into the active data path of the machine.

When the MODE pin is high, CLK S causes a parallel rather than serial load of the S register. In this mode, the S register is loaded from the Y_7–Y_0 pins at the rising edge of CLK S. This is useful in writable control store applications for readback of the control store via the serial path.

When MODE is high, the SDI pin is used as a control input to enable or disable the loading of the S register, and it also affects routing of the S register contents onto the D_7–D_0 outputs. When SDI is low, the S register is enabled for loading as above. When SDI is high however, CLK S is prevented from reaching the S register, and no load occurs. In order to allow the SDI pin to serve as an enable signal for all L29C818 devices in a serial configuration, special handling of the SDI input is required. When MODE is high, the SDI input drives the SDO output directly, bypassing the S register. This means that the SDI value will apply simultaneously to all L29C818s in a serial loop. However, to ensure proper operation of a given device, the user must ensure that the SDI setup time to CLK S is extended by the sum of the SDI to SDO delays of all previous devices in the serial path.

The D_7–D_0 port is normally used as the input port to the D register. For writable control store applications however, this port is connected to the I/O pins of the RAM used as a control store. In order to load this RAM through the serial path, it is necessary to drive the S register contents onto the D_7–D_0 pins. This is accomplished when MODE and SDI are high, and a CLK S rising edge occurs. Note from above that with SDI high, no loading of the S register occurs. However, a flip-flop is set which synchronously enables the D port output buffer. The D output remains enabled until the first rising edge of CLK S during which either SDI or MODE is low. Thus to load a control store RAM, data would be shifted in with MODE low. When an entire control store word was present in the serial S registers, the SDI and MODE pins are brought high for one or more cycles, preventing further shifting of the S registers and enabling the contents onto the D port for writing into the RAM.

To verify the contents of a control store RAM, the RAM is read into the D register in the normal fashion. Then, the D contents are transferred in parallel to the S register by driving MODE high with SDI low. Then, the S register contents are scanned out serially by returning MODE to low and applying CLK S pulses.

Table 1. Function Table

Inputs				Outputs		Action		
MODE	SDI	CLK S	CLK P	P REG	S REG	Y_7–Y_0	D_7–D_0	SDO
0	X	↑	X	N/A	SHIFT	Normal	Hi-Z	S_7
0	X	X	↑	LOAD D	N/A	Normal	Input	S_7
1	0	↑	X	N/A	LOAD Y	Input*	Hi-Z	SDI
1	1	↑	X	N/A	HOLD	Normal	Output	SDI
1	X	X	↑	LOAD S	N/A	Normal	Hi-Z	SDI

* If $\overline{OE}$ is 0, the P register value will be loaded into the S register. If $\overline{OE}$ is 1, a value may be applied externally to the Y_7–Y_0 pins.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature	−65°C to +150°C
Operating ambient temperature	−55°C to +125°C
V_{CC} supply voltage with respect to ground	−0.5 V to +7.0 V
Input signal with respect to ground	−3.0 V to +7.0 V
Signal applied to high impedance output	−3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	−55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

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ELECTRICAL CHARACTERISTICS *Over Operating Conditions*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −12.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 24.0 mA			0.5	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)			0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC}			±20	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC}			±20	µA
I_{OS}	Output Short Current	V_{OUT} = Ground, V_{CC} = Max (Notes 4, 8)			−250	mA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)		10	15	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			1.0	mA

SWITCHING CHARACTERISTICS — NORMAL REGISTER OPERATION

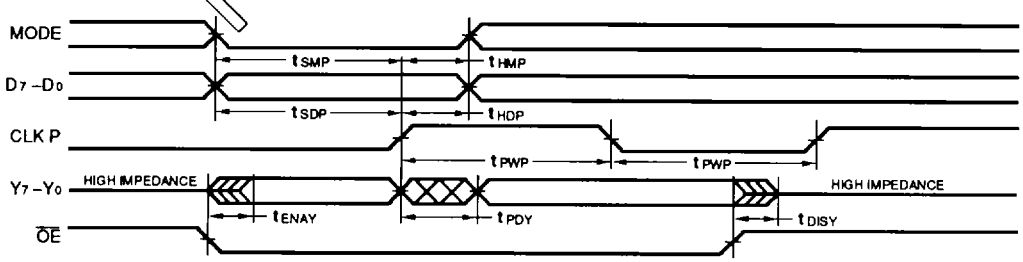
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818- 25 Min	25 Max	Min	Max
t_{PDY}	CLK P to Y_7–Y_0		13		
t_{SDP}	D_7–D_0 to CLK P Setup	8			
t_{HDP}	CLK P to D_7–D_0 Hold	2			
t_{SMP}	MODE to CLK P Setup	15			
t_{HMP}	CLK P to MODE Hold	0			
t_{PWP}	CLK P Pulse Width	15			
t_{ENAY}	$\overline{OE}$ to Y_7–Y_0 Enable (Note 11)		25		
t_{DISY}	$\overline{OE}$ to Y_7–Y_0 Disable (Note 11)		15		

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818- 30 Min	30 Max	Min	Max
t_{PDY}	CLK P to Y_7–Y_0		18		
t_{SDP}	D_7–D_0 to CLK P Setup	10			
t_{HDP}	CLK P to D_7–D_0 Hold	2			
t_{SMP}	MODE to CLK P Setup	15			
t_{HMP}	CLK P to MODE Hold	0			
t_{PWP}	CLK P Pulse Width	15			
t_{ENAY}	$\overline{OE}$ to Y_7–Y_0 Enable (Note 11)		30		
t_{DISY}	$\overline{OE}$ to Y_7–Y_0 Disable (Note 11)		20		

SWITCHING WAVEFORMS — NORMAL REGISTER OPERATION



SWITCHING CHARACTERISTICS — SERIAL SHIFT OPERATION

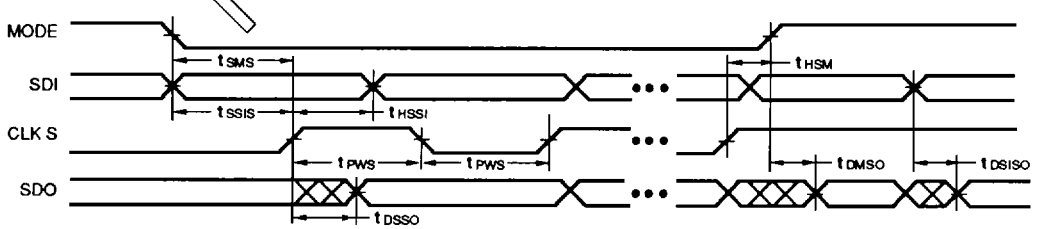
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818- 25 Min	25 Max	Min	Max
t_{DSSO}	CLK S to SDO		25		
t_{SSIS}	SDI to CLK S Setup	10			
t_{HSSI}	CLK S to SDI Hold	0			
t_{SMS}	MODE to CLK S Setup	12			
t_{HSM}	CLK S to MODE Hold	2			
t_{PWS}	CLK S Pulse Width	25			
t_{DMSO}	MODE to SDO	16			
t_{DSISO}	SDI to SDO	16			

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818- 30 Min	30 Max	Min	Max
t_{DSSO}	CLK S to SDO		30		
t_{SSIS}	SDI to CLK S Setup	12			
t_{HSSI}	CLK S to SDI Hold	0			
t_{SMS}	MODE to CLK S Setup	12			
t_{HSM}	CLK S to MODE Hold	5			
t_{PWS}	CLK S Pulse Width	25			
t_{DMSO}	MODE to SDO	18			
t_{DSISO}	SDI to SDO	18			

SWITCHING WAVEFORMS — SERIAL SHIFT OPERATION



SWITCHING CHARACTERISTICS — PIPELINE LOAD FROM SHADOW

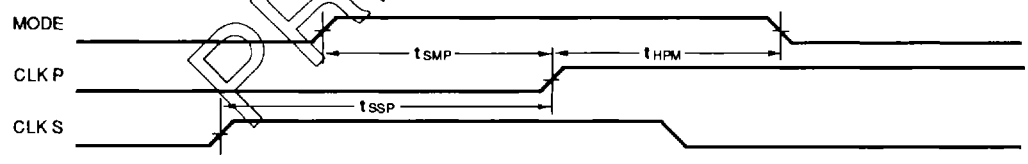
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818-25 Min	L29C818-25 Max	L29C818- Min	L29C818- Max
t_{SMP}	MODE to CLK P	15			
t_{HPM}	CLK P to MODE Hold	0			
t_{SSP}	CLK S to CLK P	10			

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818-30 Min	L29C818-30 Max	L29C818- Min	L29C818- Max
t_{SMP}	MODE to CLK P	15			
t_{HPM}	CLK P to MODE Hold	0			
t_{SSP}	CLK S to CLK P	15			

SWITCHING WAVEFORMS — PIPELINE LOAD FROM SHADOW



SWITCHING CHARACTERISTICS — SHADOW LOAD FROM 'Y' PORT

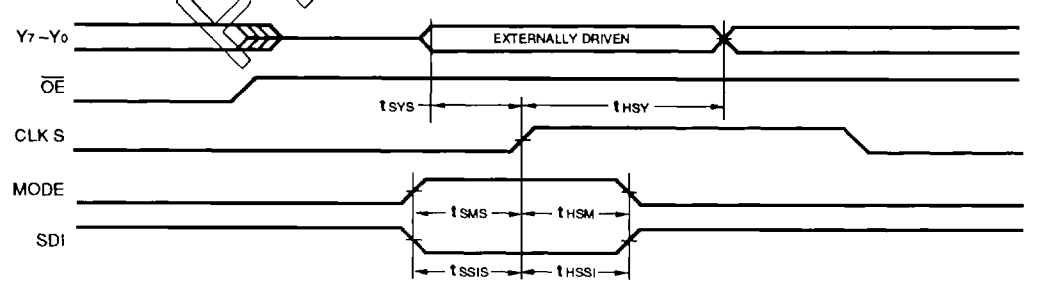
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818-25 Min	L29C818-25 Max	L29C818- Min	L29C818- Max
t_{SYS}	Y_7–Y_0 to CLK S Setup	5			
t_{HSY}	CLK S to Y_7–Y_0 Hold	5			
t_{SMS}	MODE to CLK S Setup	12			
t_{HSM}	CLK S to MODE Hold	2			
t_{SSIS}	SDI to CLK S Setup	10			
t_{HSSI}	CLK S to SDI Hold	0			

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818-30 Min	L29C818-30 Max	L29C818- Min	L29C818- Max
t_{SYS}	Y_7–Y_0 to CLK S Setup	5			
t_{HSY}	CLK S to Y_7–Y_0 Hold	5			
t_{SMS}	MODE to CLK S Setup	12			
t_{HSM}	CLK S to MODE Hold	5			
t_{SSIS}	SDI to CLK S Setup	12			
t_{HSSI}	CLK S to SDI Hold	0			

SWITCHING WAVEFORMS — SHADOW LOAD FROM 'Y' PORT



SWITCHING CHARACTERISTICS — SHADOW READ VIA 'D' PORT

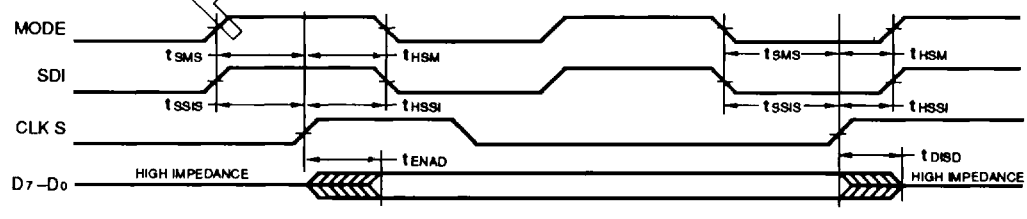
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818- 25 Min	25 Max	Min	Max
tSMS	MODE to CLK S Setup	12			
tHSM	CLK S to MODE Hold	2			
tSSIS	SDI to CLK S Setup	10			
tHSSI	CLK S to SDI Hold	0			
tENAD	CLK S TO D7–D0 Enable (Note 11)	85			
tDISD	CLK S TO D7–D0 Disable (Note 11)	30			

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

Symbol	Parameter	L29C818- 30 Min	30 Max	Min	Max
tSMS	MODE to CLK S Setup	12			
tHSM	CLK S to MODE Hold	5			
tSSIS	SDI to CLK S Setup	12			
tHSSI	CLK S to SDI Hold	0			
tENAD	CLK S TO D7–D0 Enable (Note 11)	90			
tDISD	CLK S TO D7–D0 Disable (Note 11)	35			

SWITCHING WAVEFORMS — SHADOW READ VIA 'D' PORT



NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –3.0 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Duration of the output short circuit should not exceed 30 seconds.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = suppy voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{EN}/t_{DIS} test) and input levels of nominally 0 to 3.0 V. Output loading is a resistive divider which provides for specified I_{OL} and I_{OH} plus 30 pF capacitance.

This device has high speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. Transition is measured ±200 mV from steady-state voltage with specified loading.

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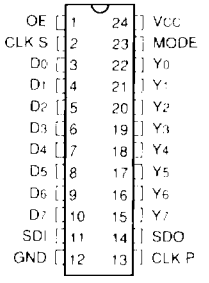
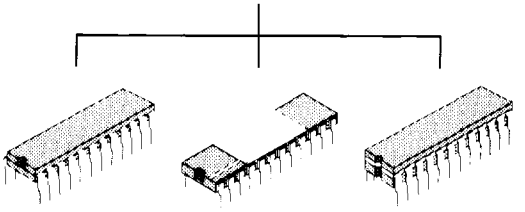
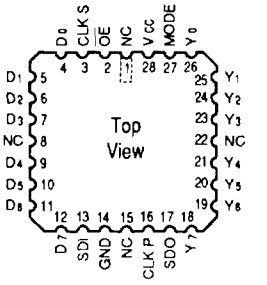
ORDERING INFORMATION

24-pin
(0.3" wide)





28-pin



Speed	Plastic DIP (P2)	Sidebraze Hermetic DIP (D2)	CerDIP (C1)	Ceramic Leadless Chip Carrier (K1)	
	0°C to +70°C — Commercial Screening				
25 ns	L29C818PC25	L29C818DC25	L29C818CC25	L29C818KC25	
	–55°C to +125°C — Commercial Screening				
30 ns		L29C818DM30	L29C818CM30	L29C818KM30	
	–55°C to +125°C — Extended Screening				
30 ns		L29C818DME30	L29C818CME30	L29C818KME30	
	–55°C to +125°C — MIL-STD-883 Compliant				
30 ns		L29C818DMB30	L29C818CMB30	L29C818KMB30	