

True logarithmic amplifier

TDA8781T

FEATURES

- 55 dB true logarithmic dynamic range
- Small-signal gain-adjust facility
- Constant limiting output voltage
- Temperature and DC power supply voltage compensation
- Easy interfacing to TDA8703 analog-to-digital converter
- Output DC level shift facility
- Additional received signal-strength indication (RSSI) output.

APPLICATIONS

- Dynamic range compression
- IF signal dynamic range reduction in GSM900 and DCS1800 receivers
- Compressive receivers.

GENERAL DESCRIPTION

The TDA8781T is a true logarithmic amplifier intended for dynamic range reduction of IF signals at 10.7 MHz in GSM900 and DCS1800 receivers. It offers true logarithmic characteristics over a 55 dB input dynamic range and has a small-signal gain-adjust facility and a

constant limiting output voltage for large input levels. It is manufactured in an advanced BICMOS process which enables high performance to be obtained with low DC power supply consumption. The true logarithmic amplifier can be driven by single-ended or differential inputs and the DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance of the true logarithmic amplifier is stabilized against temperature and DC power supply voltage variations. The differential output is converted internally to a single-ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. An additional received signal-strength indication (RSSI) output is available and a power-down facility allows the circuit to be disabled from a TTL-level compatible control input.

The device can be used to compress IF signals prior to being digitized in digital radio systems. It allows the usage of low-cost, low-power 8-bit DACs instead of the 10 or 12-bit types. In GSM systems decompression is performed by the digital signal processor such as the PCD5080. The TDA8781T interfaces directly with the ADC which is integrated on the Base Band Interface PCD5070.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	DC power supply voltage	4.5	5.0	5.5	V
I _{CC}	DC power supply current	-	-	10	mA
I _{OFF}	I _{CC} in power-down mode	-	250	400	µA
f _i	operating input frequency	0.1	10.7	15.0	MHz
T _{amb}	operating ambient temperature	-20	-	+75	°C

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8781T	14	SO14	plastic	SOT108A

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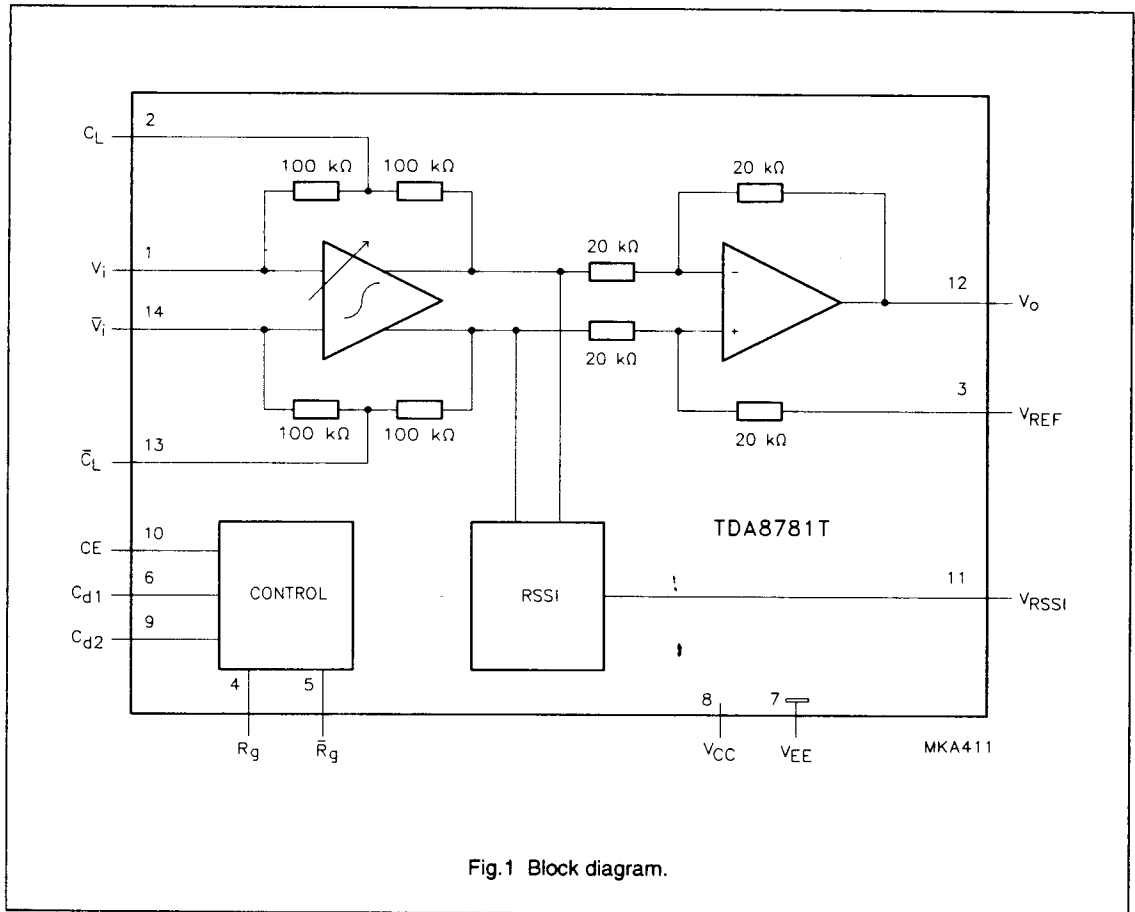


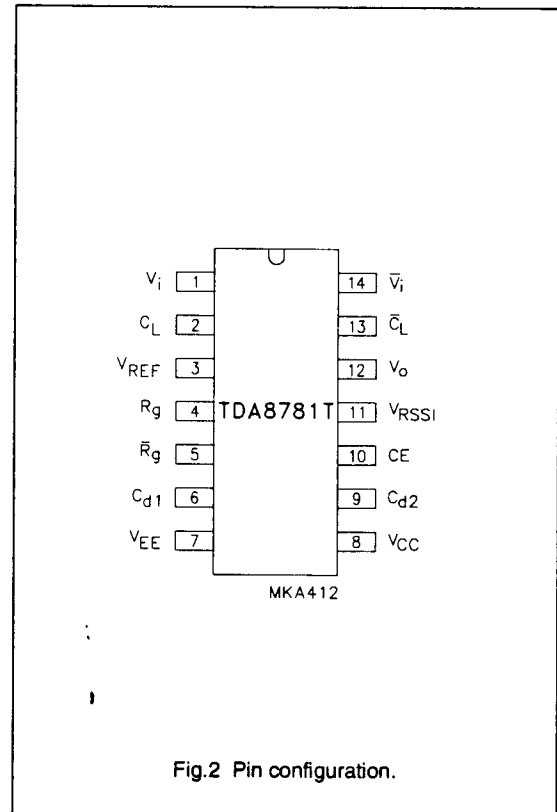
Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
V_i	1	signal input
C_L	2	low-frequency cut-off point setting capacitor connection
V_{REF}	3	external reference voltage input
R_g	4	small-signal gain-setting resistor connection
\bar{R}_g	5	complementary small-signal gain-setting resistor connection
C_{d1}	6	first control circuit decoupling capacitor and optional start-up capacitor connection
V_{EE}	7	ground
V_{CC}	8	DC power supply voltage
C_{d2}	9	second control circuit decoupling capacitor and optional start-up capacitor connection
CE	10	TTL-level-compatible circuit enable input
V_{RSSI}	11	received signal-strength indication output (RSSI)
V_o	12	true logarithmic output
\bar{C}_L	13	complementary low-frequency cut-off point setting capacitor connection
\bar{V}_i	14	complementary signal input



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FUNCTIONAL DESCRIPTION

A true logarithmic amplifier can be realized from a cascade of similar stages each of which consists of a pair of amplifiers whose inputs and outputs are connected in parallel. One of these amplifiers can be formed by an undegenerated long-tailed pair which provides high gain but a limited linear input signal-handling capability. The other amplifier can be formed by a degenerated long-tailed pair which provides a gain of unity and a much larger linear input signal-handling capability. The overall cascade amplifies very small input signals linearly but, once these reach the level at which the undegenerated long-tailed pair in the last stage is at the limit of its linear input signal-handling capability, the output voltage becomes logarithmically dependent on the input signal level. This behavior continues until the input signal reaches the level at which the undegenerated long-tailed pair in the first stage is at the limit of its linear input signal-handling capability. The transfer characteristic beyond this point then depends on the exact configuration of the degenerated long-tailed pair in the first stage.

Three stages are used in the TDA8781T to provide a 55 dB true logarithmic dynamic range. The DC bias current in the undegenerated long-tailed pair in the first stage is made externally adjustable, by means of an off-chip resistor, to provide a small-signal gain-adjust facility. A high-level limiter is inserted between the first and second stages to provide a constant limiting output

voltage which is essentially independent of the value of the gain-setting resistor. These stages can be driven by single-ended or differential inputs and the DC operating point is set by overall on-chip feedback decoupled by two off-chip capacitors which define the low-frequency cut-off point. The performance of these stages is stabilized against temperature and DC power supply voltage variations. The input to the true logarithmic amplifier is protected against damage due to excessive differential input signals by diodes.

The differential output from the true logarithmic amplifier is converted internally to a single ended output by an on-chip operational amplifier arrangement in which the DC output level is set by an externally-supplied reference voltage. The output is capable of driving loads down to 10 k Ω in parallel with 20 pF. The limiting output voltage and this output drive capability have been chosen to facilitate interfacing to a TDA8703 analog-to-digital converter. A major proportion of the DC power supply current consumption of the device is associated with provision of this output drive capability. The DC power supply consumption is significantly less when the device is driving less-highly capacitive loads.

An additional received signal-strength indication (RSSI) output is available from the true logarithmic amplifier. This output is protected against damage due to excessive current being drawn by means of a series resistor. A power-down facility allows the circuit to be disabled, from a TTL-level-compatible control input.

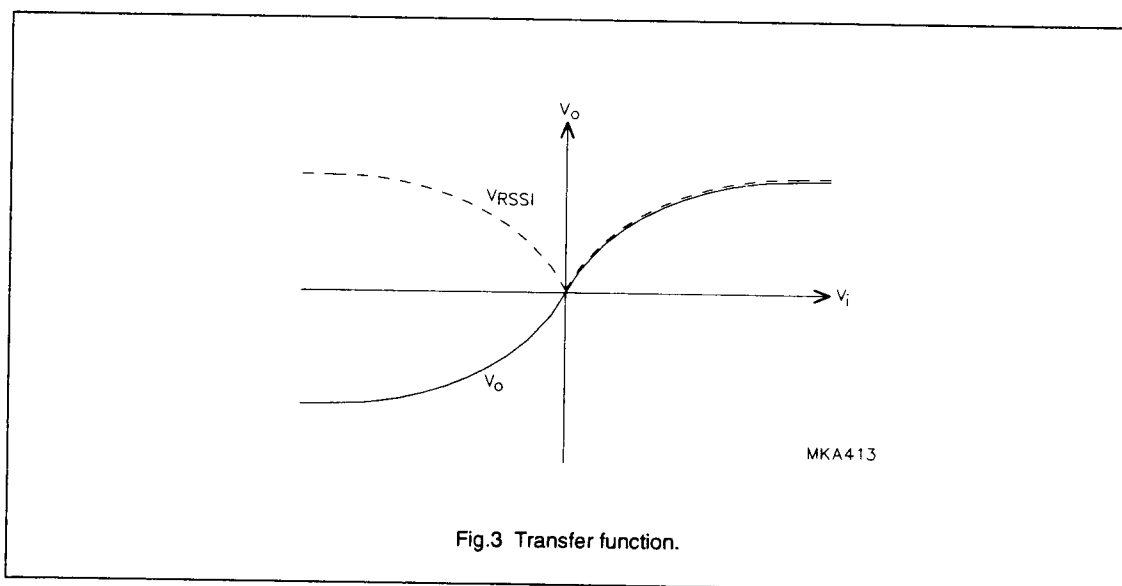


Fig.3 Transfer function.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CC}	DC power supply voltage	-0.3	+5.5	V
V_i	DC voltage at all other pins with respect to ground	-0.3	$V_{CC} + 0.3$	V
T_{stg}	storage temperature	-55	+125	°C
T_{amb}	operating ambient temperature	-20	+75	°C

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

$V_{CC} = 5.0$ V; $V_{REF} = 2.5$ V; V_i at $f_i = 10.7$ MHz; $T_{amb} = 25$ °C; nominal small-signal gain setting resistor in use; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (pin 8)						
V_{CC}	operating DC power supply voltage		4.5	5.0	5.5	V
I_{CC}	DC power supply current	$V_{CC} = 5.5$ V; $V_i = 1$ V (peak)	-	8	10	mA
I_{OFF}	DC power supply current in power-down mode	10 μ s after V_{CE} changes from $V_{CE(ON)}$ to $V_{CE(OFF)}$	-	250	400	μ A
Control: CE, R_g, \bar{R}_g, C_{d1}, C_{d2} (pins 10, 4, 5, 6 and 9)						
$V_{CE(ON)}$	circuit enable input voltage		2.0	-	V_{CC}	V
$V_{CE(OFF)}$	circuit enable input voltage in power-down mode		0	-	0.8	V
R_g	small-signal gain-setting resistor	nominal small-signal gain setting	-	3.3	-	k Ω
		total adjustment range	0	-	-	k Ω
C_{d1} , C_{d2}	control circuit decoupling capacitors		-	560	-	pF

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs: V_i, V_{REF}, C_L, \bar{C}_L (pins 1, 3, 2 and 13)						
f_i	operating input frequency		0.1	10.7	15	MHz
R_i	small-signal input resistance	differential input at $f_i = 10.7$ MHz; $V_i = 10$ mV (peak)	-	10	-	k Ω
C_i	input capacitance	differential input at $f_i = 10.7$ MHz	-	3	-	pF
$V_{i(min)}$	peak input voltage at start of true logarithmic characteristic		-	800	-	μ V
$V_{i(max)}$	peak input at end of true logarithmic characteristic		-	450	-	mV
$V_{i(lim)}$	maximum peak input signal	input protection diodes not conducting	-	1	-	V
ΔV_i	spread in true logarithmic output amplitude transfer characteristic across true logarithmic range over whole temperature and DC power supply voltage range	input spread for fixed output	-	± 2.5	-	dB
ΔG_v	small-signal gain-adjustment range		± 6	-	-	dB
C_L, \bar{C}_L	low-frequency cut-off point setting capacitors	$f = 100$ kHz at 3 dB	-	560	-	pF
R_{REF}	external reference input resistance		-	40	-	k Ω
V_{REF}	external reference voltage		2.0	2.5	$V_{CC} - 2.0$	V
Outputs: V_o, V_{RSSI} (pins 12 and 13)						
$V_{o(min)}$	peak true logarithmic output voltage relative to V_{REF} at start of true logarithmic characteristic	$V_i = 800$ μ V (peak)	-	90	-	mV
$V_{o(max)}$	peak true logarithmic output voltage relative to V_{REF} at end of true logarithmic characteristic	$V_i = 450$ mV (peak)	-	900	-	mV
V_o	true logarithmic peak output voltage across true logarithmic range	$V_i = 1$ mV (peak)	55	100	145	mV
		$V_i = 10$ mV (peak)	340	410	480	mV
		$V_i = 100$ mV (peak)	630	730	830	mV

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{o(\text{limit})}$	limiting peak output voltage	$V_i = 1 \text{ V (peak)}$	800	950	1100	mV
$V_o - V_{\text{REF}}$	DC offset voltage	$V_i = 0 \text{ V}$	-100	+35	+100	mV
ΔG_{vo}	change in small-signal true logarithmic gain referred to V_o at $V_i = 10 \text{ mV (peak)}$; $R_g = 3.3 \text{ k}\Omega$	$V_i = 5 \text{ mV (peak)}$; $R_g = 0$	0	-	+2	dB
		$V_i = 20 \text{ mV (peak)}$; $R_g = \infty$	-2	-	0	dB
ΔV_o	change in small-signal true logarithmic output voltage with frequency	$V_i = 10 \text{ mV (peak)}$; $f_i = 100 \text{ kHz}$ and 15 MHz referenced to 1 MHz	-	0.4	1.5	dB
$\Delta\phi$	spread in true logarithmic output phase transfer characteristic across true logarithmic range		-	15	-	deg
V_{RSSI}	RSSI output across true logarithmic range	$V_i = 1 \text{ mV (peak)}$	1.85	2.0	2.15	V
		$V_i = 10 \text{ mV (peak)}$	2.05	2.2	2.35	V
		$V_i = 100 \text{ mV (peak)}$	2.25	2.4	2.55	V

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APPLICATION INFORMATION

The circuit is connected as shown in the typical application circuit diagram (Fig.4). The single-ended 10.7 MHz input IF signal is applied (arbitrarily) to one of the two input pins via a ceramic filter. These inputs should not be DC coupled as this will disable the on-chip feedback which sets the DC operating point of the true logarithmic amplifier. The relatively high input impedance of these inputs facilitates correct termination of the ceramic filter by means of an off-chip resistor.

The low-frequency cut-off point is determined by the value of the capacitors which decouple the overall DC feedback as well as the value of the input coupling capacitors. The output is AC coupled to a TDA8703 analog-to-digital converter in order that the value of the voltage fed to the reference voltage input is not critical. It could be useful in other applications, where the output might be DC coupled to an alternative analog-to-digital converter, to derive this reference voltage from the centre of the input resistor chain of the analog-to-digital converter.

The additional RSSI output is required only in applications where this is not derived in subsequent digital signal processing stages. The capacitor connected to this output provides a simple peak-hold and averaging function. Excessively large values of capacitance may lead to distortion of the true logarithmic output.

It may be found advantageous to add two small capacitors to speed up the re-enabling of the circuit after it has been in power-down mode. These should be connected between the circuit enable input and the control circuit decoupling capacitors. The size of these capacitors will be related to the size of the control circuit decoupling capacitors which are required both for stability and to prevent degradation of the noise figure.

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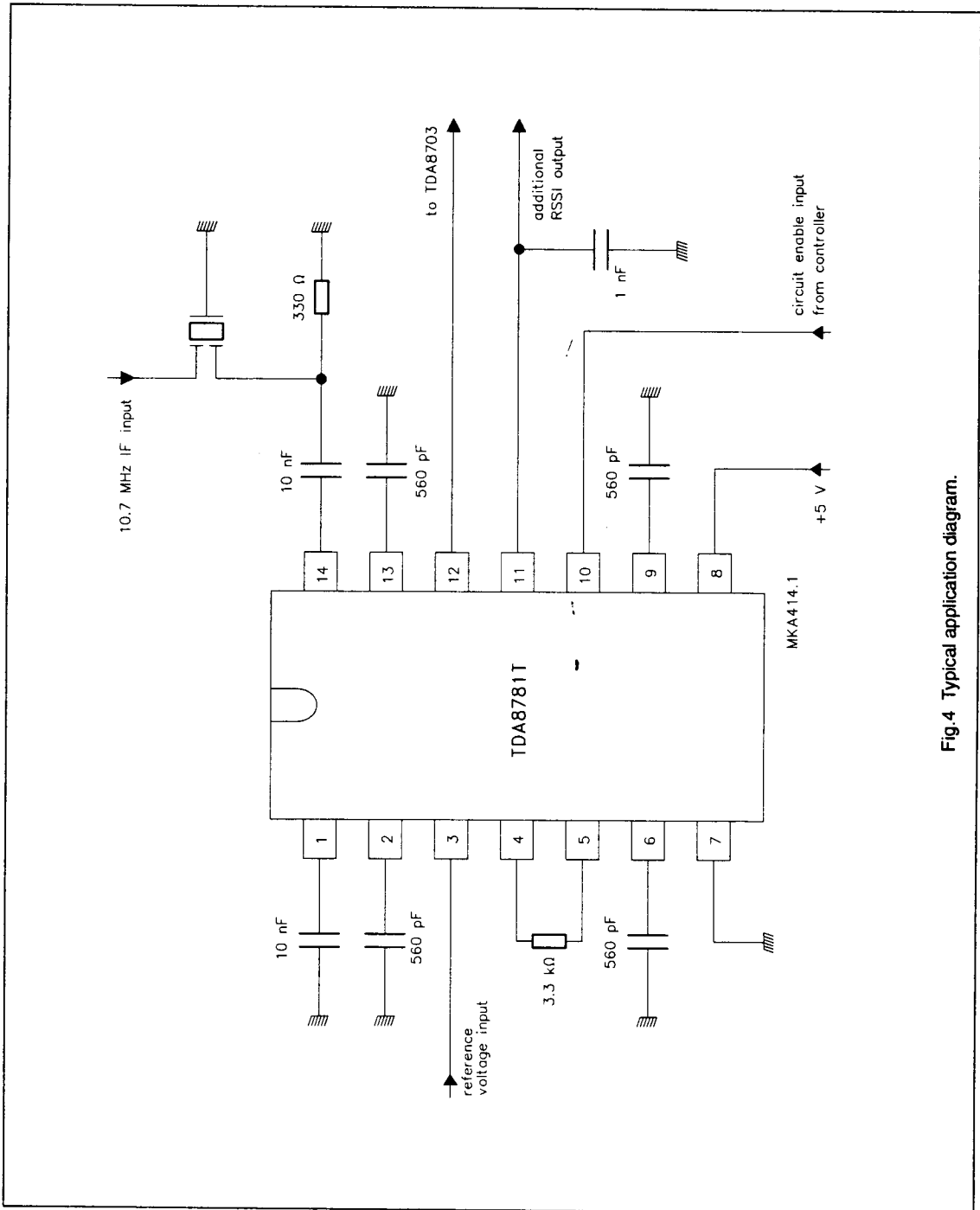


Fig. 4 Typical application diagram.