

Description

The μPD98501 has a high-performance 100 MHz MIPS® CPU as its host processor, an ATM cell processor for DSL access, a communication device class USB controller, and dual 10/100 Mbps Ethernet controllers. The ATM cell processor supports ATM adaptation layer (AAL) 0/2/5 and can handle 16 voice channels in parallel with Internet data access. The dual-channel Ethernet controller can be used in a variety of applications, such as in a SOHO router application where one channel is used for the WAN web server outside a firewall and the other channel is for the firewall-protected LAN.

Features

- ❑ High-performance V_R4120A™ 64-bit MIPS RISC processor
- ❑ Real-time operating system and network middleware on chip
- ❑ Direct connection to 16 Mb, 64 Mb, and 128 Mb SDRAM as external memory
- ❑ PROM and flash ROM interface for storing boot program
- ❑ 32-bit RISC controller as ATM cell processor
- ❑ Software SAR processing by RISC controller for flexible specification update (can support AAL 0/2/5)
- ❑ Four service classes: CBR, VBR, ABR, and UBR
- ❑ Two-channel 10/100 Mbps Ethernet controllers compliant with IEEE 802.3, 802.3u, and 802.3x
- ❑ Direct connection to external Ethernet PHY device through 3.3-volt M11 interface
- ❑ USB full-speed function controller compliant with USB specification 1.1
- ❑ Conformance to USB Communication Device Class Specification
- ❑ 8-bit, 33 MHz UTOPIA level 2 interface compliant with ATM Forum AF-PHY-003
- ❑ Micro wire interface
- ❑ 2-channel, general-purpose timers and 1-channel UART
- ❑ Serial/N-wire interface for field debugging
- ❑ Boundary scan function (JTAG) compliant with IEEE 1149.1
- ❑ 0.25 μm, 3.3-volt I/O operation
- ❑ 2.5-volt core operation
- ❑ 352-pin TBGA package

Figure 1. Internal Block Diagram

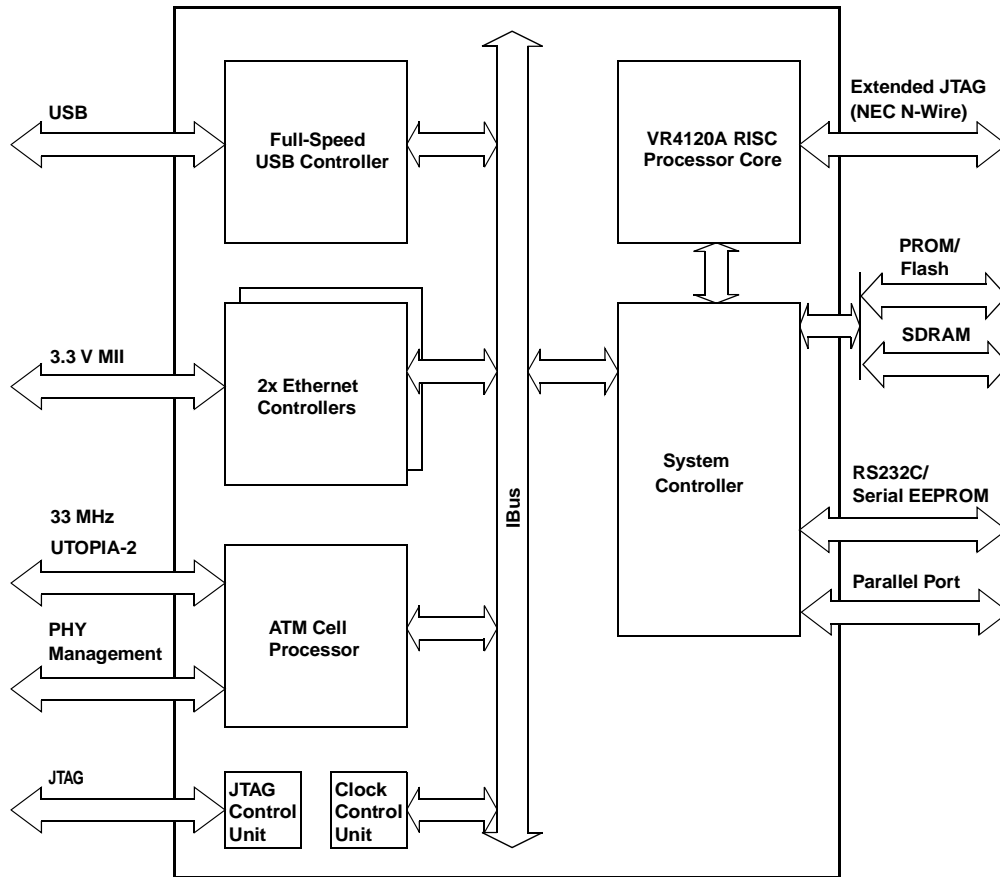
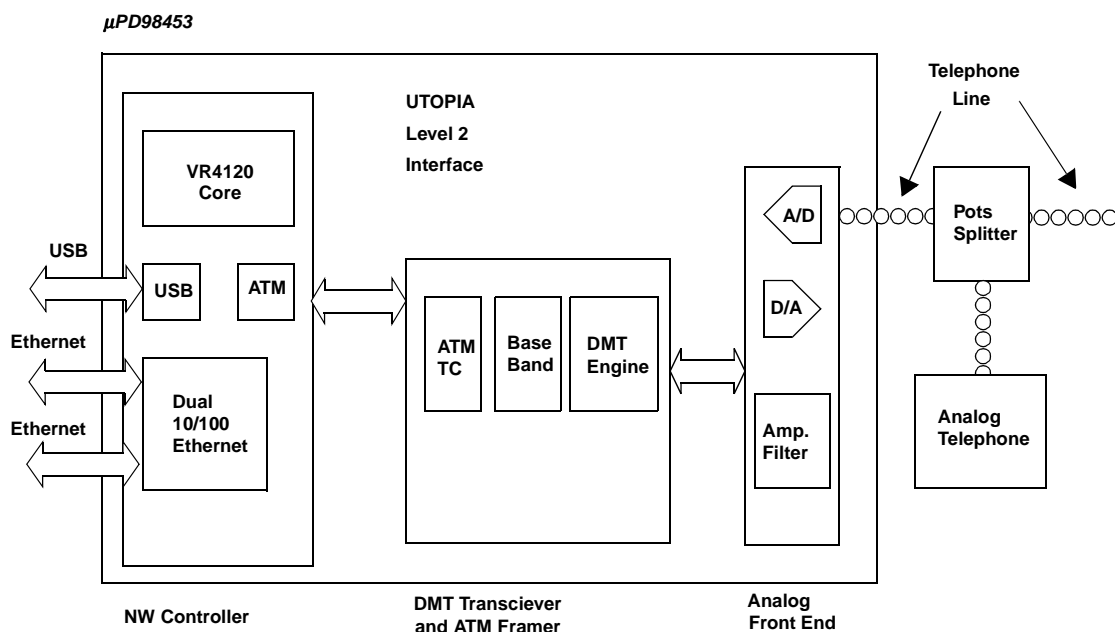


Figure 2. ADSL Chip Set Solution





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