

MOS INTEGRATED CIRCUIT
MC-458CB64SA, 458CB64LSA

8M-WORD BY 64-BIT
SYNCHRONOUS DYNAMIC RAM MODULE (SO DIMM)

Description

The MC-458CB64SA and MC-458CB64LAS are a 8,388,608 words by 64 bits synchronous dynamic RAM module (Small Outline DIMM) on which 8 pieces of 64M SDRAM : μ PD4564841 are assembled.

This module provides high density and large quantities of memory in a small space without utilizing the surface-mounting technology on the printed circuit board.

Decoupling capacitors are mounted on power supply line for noise reduction.

Features

- 8,388,608 words by 64 bits organization
- Clock frequency and Access time from CLK

Part number	/CAS Latency	Clock frequency (MAX.)	Access time from CLK (MIN.)	Power consumption (MAX.)	
				Active	Standby (CMOS level input)
MC-458CB64SA-A80	CL = 3	125 MHz	6 ns	3,888 mW	14.4 mW
	CL = 2	100 MHz	6 ns	3,744 mW	
MC-458CB64SA-A10	CL = 3	100 MHz	6 ns	3,888 mW	
	CL = 2	77 MHz	7 ns	3,744 mW	
MC-458CB64SA-A10B	CL = 3	100 MHz	7 ns	3,312 mW	
	CL = 2	67 MHz	8 ns	3,024 mW	
MC-458CB64SA-A10BL	CL = 3	100 MHz	7 ns	3,312 mW	
	CL = 2	67 MHz	8 ns	3,024 mW	
★ MC-458CB64LSA-A10B	CL = 3	100 MHz	7 ns	3,312 mW	
	CL = 2	67 MHz	8 ns	3,024 mW	
★ MC-458CB64LSA-A10BL	CL = 3	100 MHz	7 ns	3,312 mW	
	CL = 2	67 MHz	8 ns	3,024 mW	

- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1 (Bank Select)
- Programmable burst-length (1, 2, 4, 8 and Full Page)
- Programmable wrap sequence (Sequential / Interleave)
- Programmable /CAS latency (2, 3)
- Automatic precharge and controlled precharge
- CBR (Auto) refresh and self refresh
- Single +3.3 V \pm 0.3 V power supply
- LVTTTL compatible
- 4,096 refresh cycles/64 ms
- Burst termination by Burst Stop command and Precharge command
- 144-pin small outline dual in-line memory module (Pin pitch = 0.8 mm)
- Unbuffered type
- Serial PD

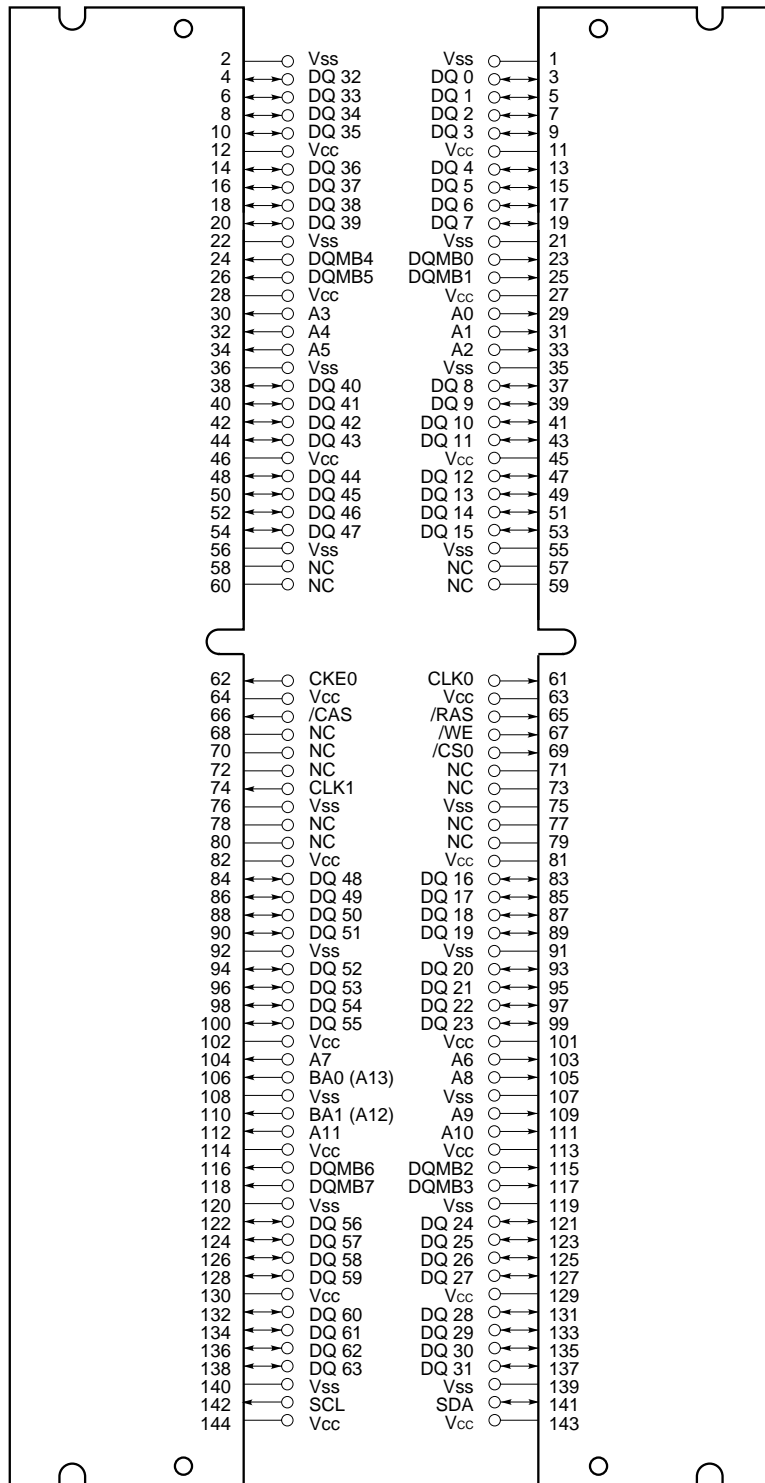
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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Ordering Information

Part number	Clock frequency MHz (MAX.)	Package	Mounted devices
MC-458CB64SA-A80	125 MHz	144-pin Small Outline DIMM (Socket Type) Edge connector : Gold plated 26.67 mm (1.05 inch) height	8 pieces of μ PD4564841G5 (Rev. E) (400 mil TSOP (II))
MC-458CB64SA-A10	100 MHz		
MC-458CB64SA-A10B	100 MHz		
MC-458CB64SA-A10BL	100 MHz		8 pieces of μ PD4564841G5 (Rev. L) (400 mil TSOP (II))
MC-458CB64LSA-A10B	100 MHz		
MC-458CB64LSA-A10BL	100 MHz		

Pin Configuration

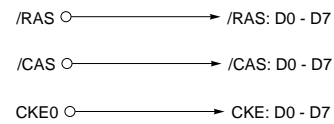
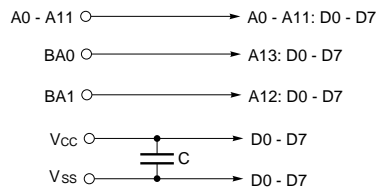
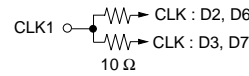
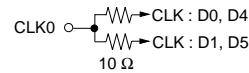
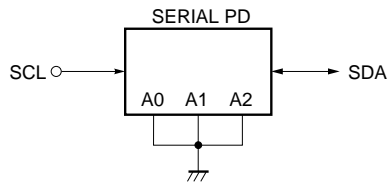
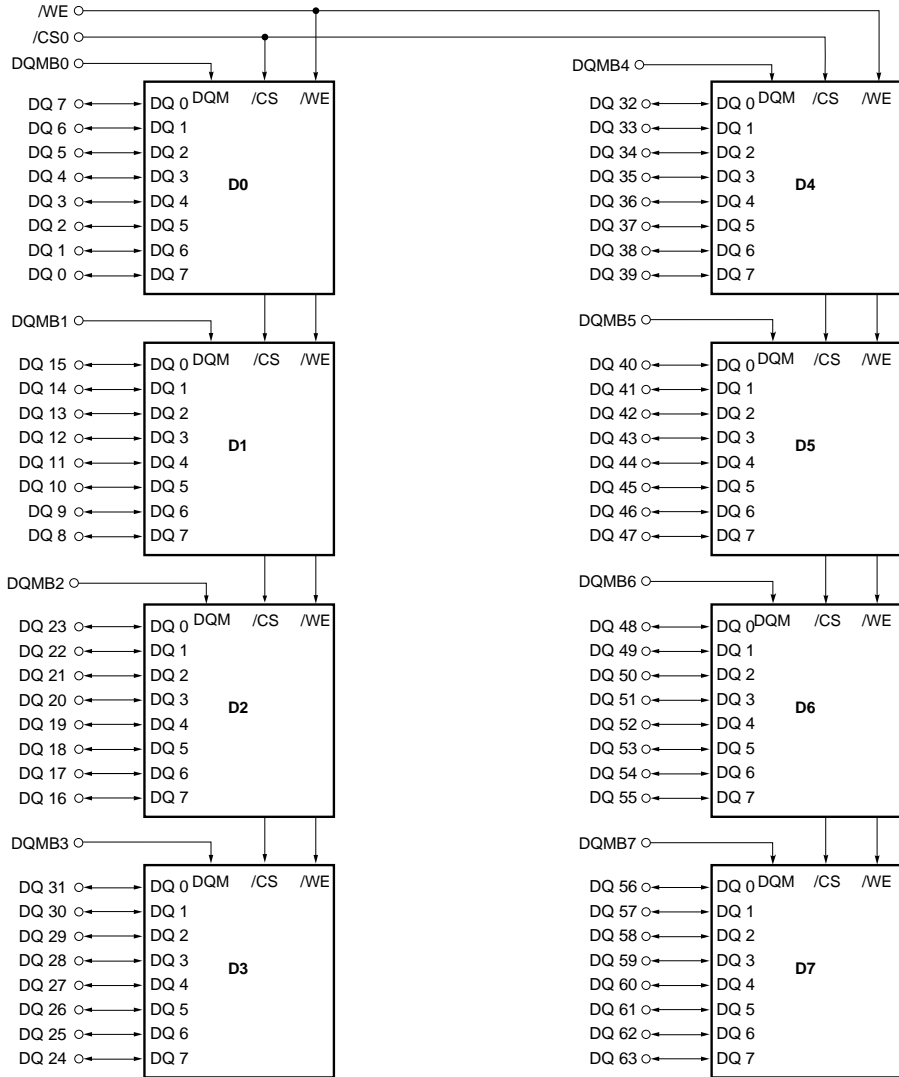
144-pin Dual In-line Memory Module Socket Type (Edge connector : Gold plated)



/xxx indicates active low signal.

- A0 - A11 : Address Inputs
- [Row : A0 - A11, Column : A0 - A8]
- BA0 (A13), BA1(A12) : SDRAM Bank Select
- DQ0 - DQ63 : Data Inputs/Outputs
- CLK0, CLK1 : Clock Input
- CKE0 : Clock Enable Input
- /CS0 : Chip Select Input
- /RAS : Row Address Strobe
- /CAS : Column Address Strobe
- /WE : Write Enable
- DQMB0 - DQMB7 : DQ Mask Enable
- SDA : Serial Data I/O for PD
- SCL : Clock Input for PD
- Vcc : Power Supply
- Vss : Ground
- NC : No Connection

Block Diagram



Remark D0 - D7 : μPD4564841(2M words × 8 bits × 4 banks)

Electrical Specifications

- All voltages are referenced to V_{ss} (GND).
- After power up, wait more than 100 μs and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V _{CC}		-0.5 to +4.6	V
Voltage on input pin relative to GND	V _T		-0.5 to +4.6	V
Short circuit output current	I _O		50	mA
Power dissipation	P _D		8	W
Operating ambient temperature	T _A		0 to +70	°C
Storage temperature	T _{stg}		-55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{CC}		3.0	3.3	3.6	V
High level input voltage	V _{IH}		2.0		V _{CC} + 0.3	V
Low level input voltage	V _{IL}		-0.3		+0.8	V
Operating ambient temperature	T _A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{I1}	A0 - A11, BA0 (A13), BA1 (A12), /RAS, /CAS, /WE			55	pF
	C _{I2}	CLK0, CLK1			36	
	C _{I3}	CKE0			55	
	C _{I4}	/CS0			55	
	C _{I5}	DQMB0 -DQMB7			10	
Data input/output capacitance	C _{I/O}	DQ0 - DQ63			10	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted)

[MC-458CB64SA]

Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Notes	
Operating current	I _{CC1}	Burst length = 1, t _{RC} ≥ t _{RC(MIN.)} I _O = 0 mA	/CAS latency = 2	-A80	640	mA	1
				-A10	560		
				-A10B	520		
			/CAS latency = 3	-A80	680		
				-A10	600		
				-A10B	600		
Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns		8	mA		
	I _{CC2PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞		4			
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.		160	mA		
	I _{CC2NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.		48			
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns		40	mA		
	I _{CC3PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞		32			
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.		200	mA		
	I _{CC3NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.		80			
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN.)} , I _O = 0 mA	/CAS latency = 2	-A80	840	mA	2
				-A10	640		
				-A10B	560		
			/CAS latency = 3	-A80	1,000		
				-A10	840		
				-A10B	840		
CBR (Auto) refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN.)}	/CAS latency = 2	-A80	1,040	mA	3
				-A10	1,040		
				-A10B	840		
			/CAS latency = 3	-A80	1,080		
				-A10	1,080		
				-A10B	920		
Self refresh current	I _{CC6}	CKE ≤ 0.2 V	-Axx	8	mA		
			-AxxL	3.2			
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V, All other pins not under test = 0 V	-8	+8	μA		
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O = 0 to 3.6 V	-1.5	+1.5	μA		
High level output voltage	V _{OH}	I _O = -4.0 mA	2.4		V		
Low level output voltage	V _{OL}	I _O = +4.0 mA		0.4	V		

- Notes**
- I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 - I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 - I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.

[MC-458CB64LSA]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I _{CC1}	Burst length = 1, t _{RC} ≥ t _{RC(MIN.)} I _O = 0 mA	/CAS latency = 2	-A10B	520	mA	1
			/CAS latency = 3	-A10B	600		
Precharge standby current in power down mode	I _{CC2P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns			8	mA	
	I _{CC2PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			4		
Precharge standby current in non power down mode	I _{CC2N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.			160	mA	
	I _{CC2NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.			48		
Active standby current in power down mode	I _{CC3P}	CKE ≤ V _{IL(MAX.)} , t _{CK} = 15 ns			40	mA	
	I _{CC3PS}	CKE ≤ V _{IL(MAX.)} , t _{CK} = ∞			32		
Active standby current in non power down mode	I _{CC3N}	CKE ≥ V _{IH(MIN.)} , t _{CK} = 15 ns, /CS ≥ V _{IH(MIN.)} , Input signals are changed one time during 30 ns.			200	mA	
	I _{CC3NS}	CKE ≥ V _{IH(MIN.)} , t _{CK} = ∞, Input signals are stable.			120		
Operating current (Burst mode)	I _{CC4}	t _{CK} ≥ t _{CK(MIN.)} , I _O = 0 mA	/CAS latency = 2	-A10B	560	mA	2
			/CAS latency = 3	-A10B	840		
CBR (Auto) refresh current	I _{CC5}	t _{RC} ≥ t _{RC(MIN.)}	/CAS latency = 2	-A10B	840	mA	3
			/CAS latency = 3	-A10B	920		
Self refresh current	I _{CC6}	CKE ≤ 0.2 V	-Axx		8	mA	
			-AxxL		3.2		
Input leakage current	I _{I(L)}	V _I = 0 to 3.6 V, All other pins not under test = 0 V		-8	+8	μA	
Output leakage current	I _{O(L)}	D _{OUT} is disabled, V _O = 0 to 3.6 V		-1.5	+1.5	μA	
High level output voltage	V _{OH}	I _O = -4.0 mA		2.4		V	
Low level output voltage	V _{OL}	I _O = +4.0 mA			0.4	V	

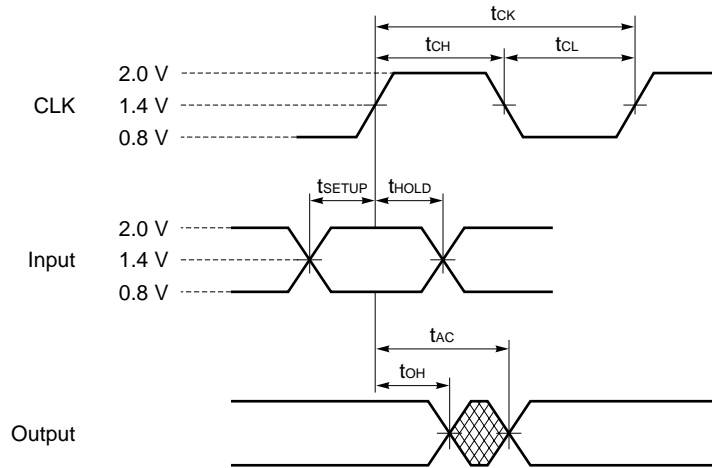
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- Notes**
- I_{CC1} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC1} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 - I_{CC4} depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.
 - I_{CC5} is measured on condition that addresses are changed only one time during t_{CK(MIN.)}.

AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

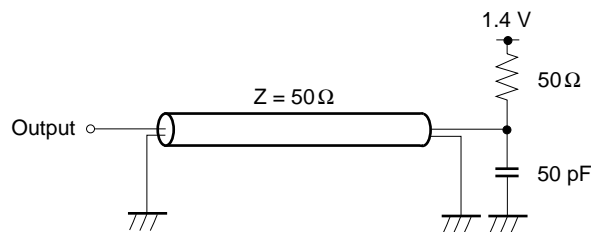
- AC measurements assume $t_{\tau} = 1 \text{ ns}$.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL} .
- If t_{τ} is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH(MIN.)}$ and $V_{IL(MAX.)}$.
- An access time is measured at 1.4 V.



Synchronous Characteristics

Parameter		Symbol	-A80		-A10		-A10B		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	/CAS latency = 3	t _{CK3}	8		10		10		ns	
	/CAS latency = 2	t _{CK2}	10		13		15		ns	
Access time from CLK	/CAS latency = 3	t _{AC3}		6		6		7	ns	1
	/CAS latency = 2	t _{AC2}		6		7		8	ns	1
CLK high level width		t _{CH}	3		3		3.5		ns	
CLK low level width		t _{CL}	3		3		3.5		ns	
Data-out hold time		t _{OH}	3		3		3		ns	1
Data-out low-impedance time		t _{LZ}	0		0		0		ns	
Data-out high-impedance time	/CAS latency = 3	t _{HZ3}	3	6	3	6	3	7	ns	
	/CAS latency = 2	t _{HZ2}	3	6	3	7	3	8	ns	
Data-in setup time		t _{DS}	2		2		2.5		ns	
Data-in hold time		t _{DH}	1		1		1		ns	
Address setup time		t _{AS}	2		2		2.5		ns	
Address hold time		t _{AH}	1		1		1		ns	
CKE setup time		t _{CKS}	2		2		2.5		ns	
CKE hold time		t _{CKH}	1		1		1		ns	
CKE setup time (Power down exit)		t _{CKSP}	2		2		2.5		ns	
Command (/CS0, /RAS, /CAS, /WE, DQMB0 - DQMB7) setup time		t _{CMS}	2		2		2.5		ns	
Command (/CS0, /RAS, /CAS, /WE, DQMB0 - DQMB7) hold time		t _{CMH}	1		1		1		ns	

Note 1. Output load



Asynchronous Characteristics

Parameter	Symbol	-A80		-A10		-A10B		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
REF to REF/ACT command period	t _{RC}	70		70		90		ns	
ACT to PRE command period	t _{RAS}	48	120,000	50	120,000	60	120,000	ns	
PRE to ACT command period	t _{RP}	20		20		30		ns	
Delay time ACT to READ/WRITE command	t _{RCD}	20		20		30		ns	
ACT(0) to ACT(1) command period	t _{RRD}	16		20		20		ns	
Data-in to PRE command period	t _{DPL}	8		10		10		ns	
Data-in to ACT(REF) command period (Auto precharge)	/CAS latency = 3	t _{DAL3}	1CLK+20		1CLK+20		1CLK+30	ns	
	/CAS latency = 2	t _{DAL2}	1CLK+20		1CLK+20		1CLK+30	ns	
Mode register set cycle time	t _{RSC}	2		2		2		CLK	
Transition time	t _T	0.5	30	1	30	1	30	ns	
Refresh time (4,096 refresh cycles)	t _{REF}		64		64		64	ms	

Serial PD

(1/2)

Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
0	Defines the number of bytes written into serial PD memory	80H	1	0	0	0	0	0	0	0	128 bytes	
1	Total number of bytes of serial PD memory	08H	0	0	0	0	1	0	0	0	256 bytes	
2	Fundamental memory type	04H	0	0	0	0	0	1	0	0	SDRAM	
3	Number of rows	0CH	0	0	0	0	1	1	0	0	12 rows	
4	Number of columns	09H	0	0	0	0	1	0	0	1	9 columns	
5	Number of banks	01H	0	0	0	0	0	0	0	1	1 bank	
6	Data width	40H	0	1	0	0	0	0	0	0	64 bits	
7	Data width (continued)	00H	0	0	0	0	0	0	0	0	0	
8	Voltage interface	01H	0	0	0	0	0	0	0	1	LVTTTL	
9	CL = 3 Cycle time	-A80	80H	1	0	0	0	0	0	0	0	8 ns
		-A10	A0H	1	0	1	0	0	0	0	0	10 ns
		-A10B/-A10BL	A0H	1	0	1	0	0	0	0	0	10 ns
10	CL =3 Access time	-A80	60H	0	1	1	0	0	0	0	0	6 ns
		-A10	60H	0	1	1	0	0	0	0	0	6 ns
		-A10B/-A10BL	70H	0	1	1	1	0	0	0	0	7 ns
11	DIMM configuration type	00H	0	0	0	0	0	0	0	0	Non-parity	
12	Refresh rate/type	80H	1	0	0	0	0	0	0	0	Normal	
13	SDRAM width	08H	0	0	0	0	1	0	0	0	x8	
14	Error checking SDRAM width	00H	0	0	0	0	0	0	0	0	None	
15	Minimum clock delay	01H	0	0	0	0	0	0	0	1	1 clock	
16	Burst length supported	8FH	1	0	0	0	1	1	1	1	1, 2, 4, 8, F	
17	Number of banks on each SDRAM	04H	0	0	0	0	0	1	0	0	4 banks	
18	/CAS latency supported	06H	0	0	0	0	0	1	1	0	2, 3	
19	/CS latency supported	01H	0	0	0	0	0	0	0	1	0	
20	/WE latency supported	01H	0	0	0	0	0	0	0	1	0	
21	SDRAM module attributes	00H	0	0	0	0	0	0	0	0		
22	SDRAM device attributes : General	0EH	0	0	0	0	1	1	1	0		
23	CL = 2 Cycle time	-A80	A0H	1	0	1	0	0	0	0	0	10 ns
		-A10	D0H	1	1	0	1	0	0	0	0	13 ns
		-A10B/-A10BL	F0H	1	1	1	1	0	0	0	0	15 ns
24	CL = 2 Access time	-A80	60H	0	1	1	0	0	0	0	0	6 ns
		-A10	70H	0	1	1	1	0	0	0	0	7 ns
		-A10B/-A10BL	80H	1	0	0	0	0	0	0	0	8 ns
25-26		00H	0	0	0	0	0	0	0	0		

(2/2)

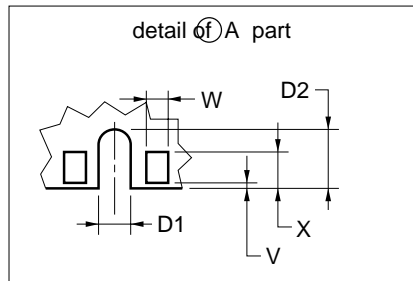
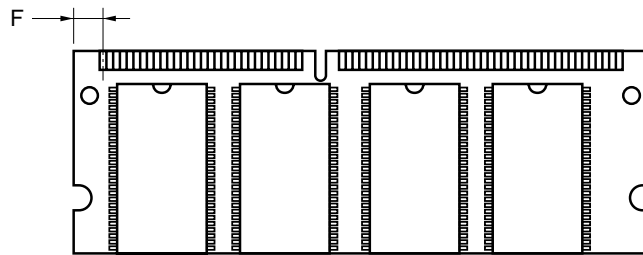
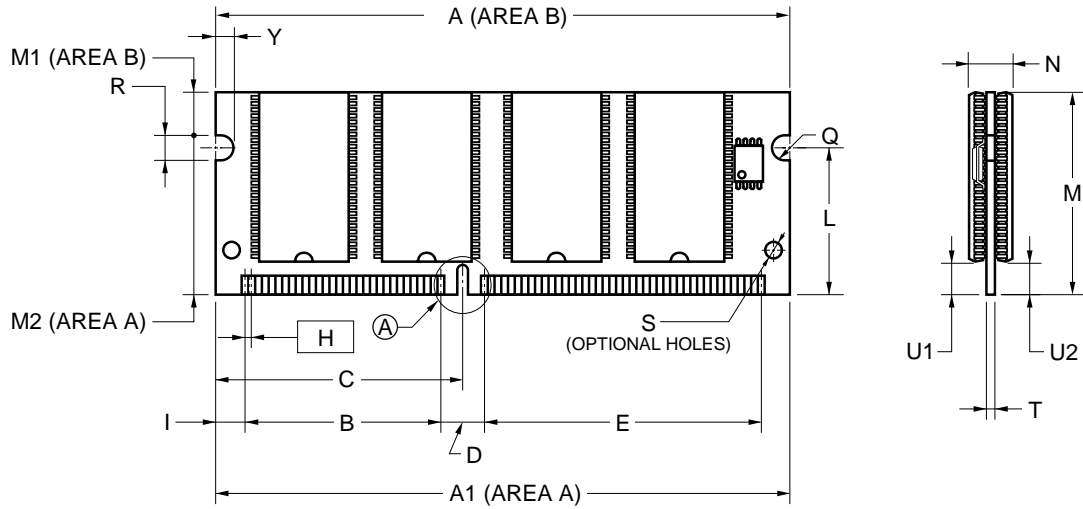
Byte No.	Function Described	Hex	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Notes	
27	tRP(MIN.)	-A80	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A10B/-A10BL	1EH	0	0	0	1	1	1	1	0	30 ns
28	tRRD(MIN.)	-A80	10H	0	0	0	1	0	0	0	0	16 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A10B/-A10BL	14H	0	0	0	1	0	1	0	0	20 ns
29	tRCD(MIN.)	-A80	14H	0	0	0	1	0	1	0	0	20 ns
		-A10	14H	0	0	0	1	0	1	0	0	20 ns
		-A10B/-A10BL	1EH	0	0	0	1	1	1	1	0	30 ns
30	tRAS(MIN.)	-A80	30H	0	0	1	1	0	0	0	0	48 ns
		-A10	32H	0	0	1	1	0	0	1	0	50 ns
		-A10B/-A10BL	3CH	0	0	1	1	1	1	0	0	60 ns
31	Module bank density	10H	0	0	0	1	0	0	0	0	64 M bytes	
32	tRP(MIN.)	-A80	20H	0	0	1	0	0	0	0	0	2 ns
		-A10	20H	0	0	1	0	0	0	0	0	2 ns
		-A10B/-A10BL	00H	0	0	0	0	0	0	0	0	
33	tRRD(MIN.)	-A80	10H	0	0	0	1	0	0	0	0	1 ns
		-A10	10H	0	0	0	1	0	0	0	0	1 ns
		-A10B/-A10BL	00H	0	0	0	0	0	0	0	0	
34	tRCD(MIN.)	-A80	20H	0	0	1	0	0	0	0	0	2 ns
		-A10	20H	0	0	1	0	0	0	0	0	2 ns
		-A10B/-A10BL	00H	0	0	0	0	0	0	0	0	
35	tRAS(MIN.)	-A80	10H	0	0	0	1	0	0	0	0	1 ns
		-A10	10H	0	0	0	1	0	0	0	0	1 ns
		-A10B/-A10BL	00H	0	0	0	0	0	0	0	0	
36-61		00H	0	0	0	0	0	0	0	0		
62	SPD revision	-A80	12H	0	0	0	1	0	0	1	0	1.2
		-A10	12H	0	0	0	1	0	0	1	0	1.2
		-A10B/-A10BL	01H	0	0	0	0	0	0	0	1	1
63	Checksum for bytes 0 - 62	-A80	DFH	1	1	0	1	1	1	1	1	
		-A10	45H	0	1	0	0	0	1	0	1	
		-A10B/-A10BL	32H	0	0	1	1	0	0	1	0	
64-71	Manufacture's JEDEC ID code											
72	Manufacturing location											
73-90	Manufacture's P/N											
91-92	Revision code											
93-94	Manufacturing date											
95-98	Assembly serial number											
99-125	Mfg specific											
126	Intel specification frequency	-A80	64H	0	1	1	0	0	1	0	0	100 MHz
		-A10	64H	0	1	1	0	0	1	0	0	100 MHz
		-A10B/-A10BL	66H	0	1	1	0	0	1	1	0	66 MHz
127	Intel specification /CAS latency support	-A80	C7H	1	1	0	0	0	1	1	1	
		-A10	C5H	1	1	0	0	0	1	0	1	
		-A10B/-A10BL	06H	0	0	0	0	0	1	1	0	

Timing Chart

Refer to the **SYNCHRONOUS DRAM MODULE TIMING CHART Information (M13348X)**.

Package Drawing

144 PIN DUAL IN-LINE MODULE (SOCKET TYPE)



ITEM	MILLIMETERS
A	67.6
A1	67.6±0.15
B	23.2
C	29.0
D	4.6
D1	1.5±0.10
D2	4.0
E	32.8
F	3.7
H	0.8 (T.P.)
I	3.3
L	20.0
M	26.67±0.15
M1	4.67
M2	22.0
N	3.8 MAX.
Q	R2.0
R	4.0±0.10
S	f 1.8
T	1.0±0.1
U1	3.2 MIN.
U2	4.0 MIN.
V	0.25 MAX.
W	0.6±0.05
X	2.55 MIN.
Y	2.0 MIN.

[MEMO]

NOTES FOR CMOS DEVICES**① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory IC, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.

When re-packing memory modules, be sure the modules are NOT touching each other. Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

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