HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7680R/81R
1K x 8 PROM

HM-7680R - Open Collector Outputs
HM-7681R - "Three State" Outputs

DECEMBER 1977 **Preliminary**

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURES AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LATCHED OUTPUTS

Description

The HM-7680R/81R is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680R) or "Three State" (HM-7681R) outputs. These PROMs are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7680R/81R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

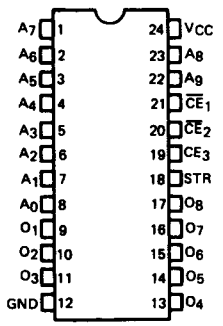
There are three chip enable inputs on the HM-7680R/81R. $\overline{CE}_1$, $\overline{CE}_2$ low and CE_3 high enables the chip.

The HM-7680R/81R is operated in the Transparent Read Mode by holding the strobe input high throughout the read operation. This is the normal read mode where the three chip enable inputs will control the outputs.

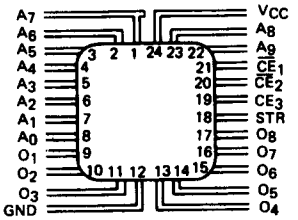
In Latched Read Mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled when the strobe input goes low, the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinouts

TOP VIEW—DIP



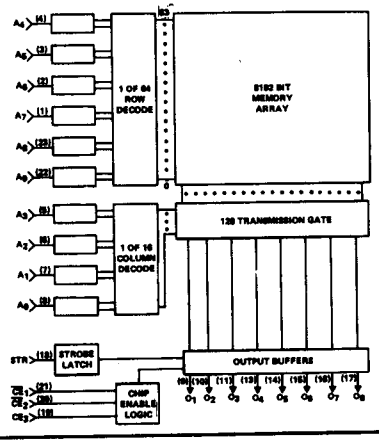
TOP VIEW – FLATPACK



PIN NAMES

A0 – A9	Address Inputs
O1 – O8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3	Chip Enable Inputs
STR	Strobe

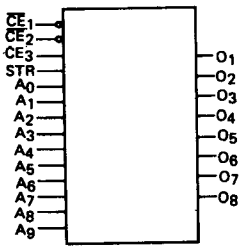
Functional Diagram



NOTE: Physical bit positions for columns are as follows:
$O_1, O_3, O_5, O_7 \rightarrow (0 \rightarrow 15)$
$O_2, O_4, O_6, O_8 \rightarrow (15, 0 \rightarrow 14)$

( ) = Pin Numbers
(24) = V_{CC}
(12) = GND

Logic Symbol



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680R/81R-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7680R/81R-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15*	-2.5	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

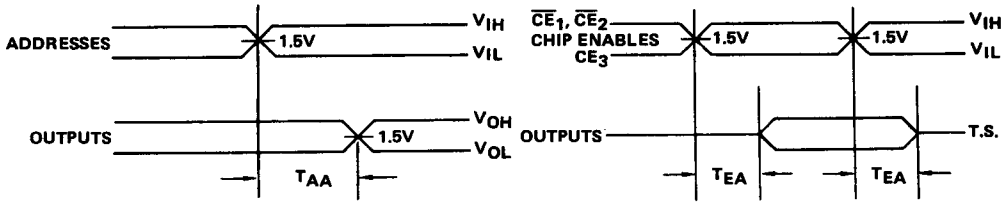
		HM-7680R/81R-5 5V ±5% 0°C to +75°C			HM-7680R/81R-2 5V ±10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA}	Address Access Time	–	45	60	–	–	80	ns	Latched or Transparent
T_{EA}	Chip Enable Access Time		30	40	–	–	50	ns	
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	10	–	40	10	–	ns	
T_{SL}	Strobe Latch Time	60	40	–	80	40	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE : T_A = 25°C

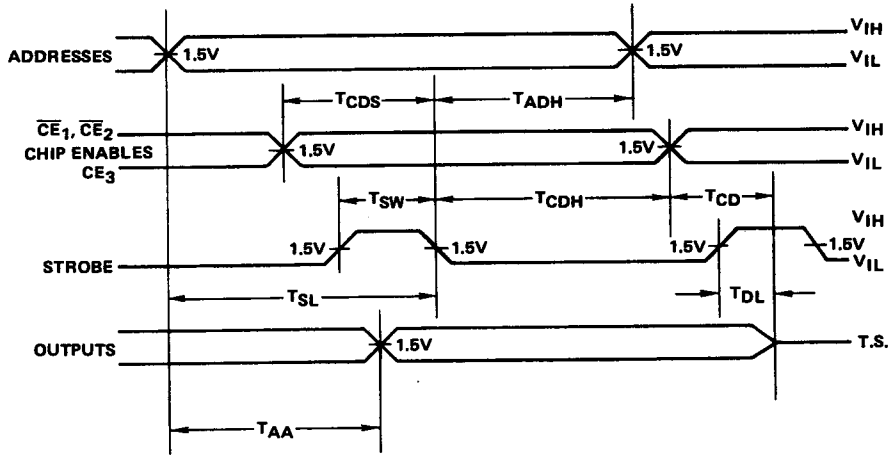
SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS (Transparent Mode)



NOTE: Strobe input must remain high throughout read cycle while in transparent mode.

SWITCHING TIME DEFINITIONS (Latched Mode)



A.C. TEST LOAD