OKI semiconductor

MSM514412A/AL

1,048,576-Word x 4-Bit DYNAMIC RAM: STATIC COLUMN/WRITE PER BIT MODE TYPE

GENERAL DESCRIPTION

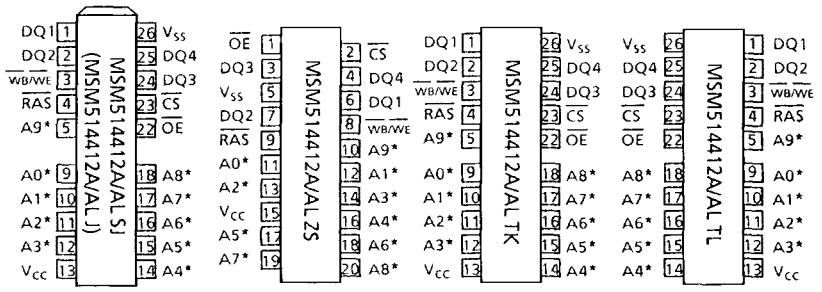
The MSM514412A/AL is a new generation dynamic RAM organized as 1,048,576-word x 4-bit. The technology used to fabricate the MSM514412A/AL is OKI's CMOS silicon gate process technology. The device operates at a single + 5 V power supply. Its I/O pins are TTL compatible.

FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 1,048,576-word x 4-bit organization
- 300/350 mil 26-pin plastic SOJ, 400 mil 20-pin plastic ZIP, 300 mil 26-pin plastic TSOP
- Single + 5 V power supply, ± 10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms, 128 ms (L-version)
- $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{CS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$-only refresh capability
- Multibit test mode capability
- Built-in V_{BB} generator circuit

Family	Access Time (Max)				Cycle Time (Min)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (Max)	Standby (Max)
MSM514412A/AL-70	70 ns	35 ns	20 ns	20 ns	130 ns	495 mW	5.5 mW/1.1 mW (L-version)
MSM514412A/AL-80	80 ns	40 ns	20 ns	20 ns	150 ns	440 mW	
MSM514412A/AL-10	100 ns	50 ns	25 ns	25 ns	180 ns	385 mW	

PIN CONFIGURATION (TOP VIEW)



26 PIN SOJ

20 PIN ZIP

26 PIN TSOP (K TYPE)

26 PIN TSOP (L TYPE)

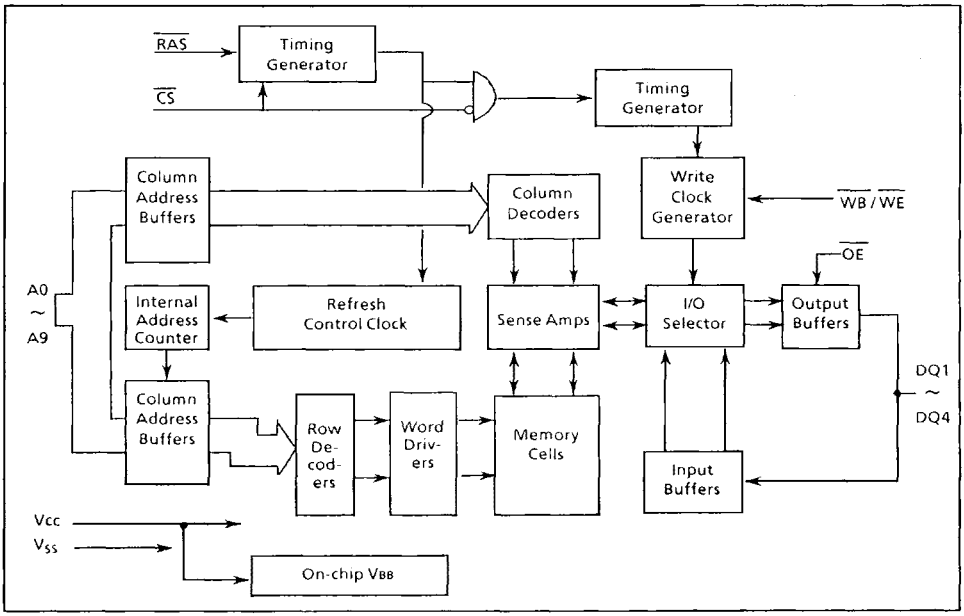
SJ : 300 mil
J : 350 mil

* Refresh Address

Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
DQ1 to DQ4	Data In/Data Out

Pin Names	Function
$\overline{OE}$	Output Enable
$\overline{WB/WE}$	Write Enable
V_{CC}	Power Supply < +5V >
V_{SS}	Ground <0V>

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit	Notes
Voltage on any pin relative to V_{SS}	VT	Ta = 25 °C	− 1.0 to + 7.0	V	1
Short circuit output current	Ios	Ta = 25 °C	50	mA	1
Power dissipation	P_D	Ta = 25 °C	1	W	1
Operating temperature	Topr	–	0 to + 70	°C	1
Storage temperature	Tstg	–	− 55 to + 150	°C	1

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	–	6.5	V	2
Input low voltage	V_{IL}	− 1.0	–	0.8	V	2

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM514412A/AL-70 Min	MSM514412A/AL-70 Max	MSM514412A/AL-80 Min	MSM514412A/AL-80 Max	MSM514412A/AL-10 Min	MSM514412A/AL-10 Max	Unit	Notes
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all other pins not under test = 0V	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	DQ_i = disable 0V ≦ VO ≦ 5.5 V	−10	10	−10	10	−10	10	μA	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC} = min	−	90	−	80	−	70	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IH}, DQ_i = Hz — TTL	−	2	−	2	−	2	mA	
		$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IH}, DQ_i = Hz — TTL	−	1	−	1	−	1	mA	
		$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IH}, DQ_i = Hz — MOS	−	200	−	200	−	200	μA	L-version
Average power supply current (RAS-only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CS}$ = V_{IH}, t_{RC} = min	−	90	−	80	−	70	mA	1, 2
Power supply current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL}, DQ_i = enable	−	5	−	5	−	5	mA	1
Average power supply current ($\overline{CS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$	−	90	−	80	−	70	mA	1
Average power supply current (Static Column mode)	I_{CC9}	$\overline{RAS}$ = V_{IL}, $\overline{CS}$ cycling, t_{PC} = min	−	80	−	70	−	60	mA	1
Battery backup current (Only L-version)	I_{CC10}	t_{RC} = 125 μs, $\overline{CS}$ before $\overline{RAS}$ $\overline{RAS}$ cycling	−	300	−	300	−	300	μA	1, 3

Notes: 1. I_{CC} depends on output loading and cycle rates. Specified values are obtained with the output open.
2. Measured by using no more than one address change while $\overline{RAS}$ = V_{IL}.
3. t_{RAS} = t_{RAS} (min) to 1 μs. Input voltage: All pins V_{IH} ≧ V_{CC} − 0.2V or V_{IL} ≦ 0.2V

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	Typ	Max	Unit
Input capacitance (A0 to A9)	C_{IN1}	−	−	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WB}$ / $\overline{WE}$, $\overline{OE}$)	C_{IN2}	−	−	7	pF
Output capacitance (DQ1 to DQ4)	$C_{I/O}$	−	−	7	pF

AC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to + 70°C)
Notes 1, 2, 3, 11

Parameter	Symbol	MSM514412A/AL-70		MSM514412A/AL-80		MSM514412A/AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	130	–	150	–	180	–	ns	
Read/write cycle time	t_{RWC}	185	–	205	–	245	–	ns	
Static column mode cycle time	t_{SC}	40	–	45	–	55	–	ns	
Static column mode read/write cycle time	t_{SRWC}	90	–	95	–	115	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	70	–	80	–	100	ns	4,5,6
Access time from $\overline{CS}$	t_{CAC}	–	20	–	20	–	25	ns	4, 5
Access time from column address	t_{AA}	–	35	–	40	–	50	ns	4,6,7
Access time from last write	t_{ALW}	–	65	–	75	–	95	ns	4, 7
Access time from $\overline{OE}$	t_{OEA}	–	20	–	20	–	25	ns	
Data output enable time reference to $\overline{WE}$	t_{OW}	–	20	–	20	–	25	ns	
Output low impedance time from $\overline{CS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Data output hold time reference to column address	t_{AOH}	5	–	5	–	5	–	ns	
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	25	ns	8
$\overline{OE}$ to data output buffer turn-off delay time	t_{OEZ}	0	20	0	20	0	25	ns	8
Transition time	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	–	16	–	16	–	16	ms	
Refresh period (only L-version)	t_{REF}	–	128	–	128	–	128	ms	
$\overline{RAS}$ precharge time	t_{RP}	50	–	60	–	70	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	70	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	20	–	25	–	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	20	–	20	–	25	–	ns	
$\overline{CS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{CS}$ pulse width	t_{CS}	20	100,000	20	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	70	–	80	–	100	–	ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	–	5	–	5	–	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	20	50	20	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	20	50	ns	6
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	10	–	10	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM514412A/AL-70		MSM514412A/AL-80		MSM514412A/AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Column address hold time reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	55	–	60	–	75	–	ns	
Column address hold time reference to $\overline{RAS}$	t_{AR}	85	–	95	–	115	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	–	40	–	50	–	ns	
Column address hold time reference to $\overline{RAS}$ precharge	t_{AH}	10	–	10	–	10	–	ns	
Column address hold time reference to $\overline{WE}$	t_{AHLW}	65	–	75	–	95	–	ns	
Last write to column address delay time	t_{LWAD}	20	30	20	35	25	45	ns	7
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	–	0	–	0	–	ns	9
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	10
Write command hold time	t_{WCH}	10	–	15	–	20	–	ns	
Write command pulse width	t_{WP}	10	–	15	–	20	–	ns	
$\overline{OE}$ command hold time	t_{OEH}	20	–	20	–	25	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	50	–	60	–	75	–	ns	
Write invalid time	t_{WI}	10	–	10	–	10	–	ns	
Write command hold time (D_{OUT} disable)	t_{WH}	0	–	0	–	0	–	ns	10
Write command to $\overline{CS}$ lead time	t_{CWL}	20	–	20	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	20	–	25	–	ns	
$\overline{CS}$ to $\overline{WE}$ delay time	t_{CWD}	50	–	50	–	60	–	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	65	–	70	–	85	–	ns	10
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	100	–	110	–	135	–	ns	10
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	55	–	60	–	75	–	ns	
$\overline{OE}$ to Data-in delay time	t_{OED}	20	–	20	–	25	–	ns	
$\overline{CS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	5	–	5	–	5	–	ns	
$\overline{RAS}$ to $\overline{CS}$ Set-up time ($\overline{CS}$ before $\overline{RAS}$)	t_{CSR}	5	–	5	–	5	–	ns	
$\overline{RAS}$ to $\overline{CS}$ hold time ($\overline{CS}$ before $\overline{RAS}$)	t_{CHR}	15	–	15	–	15	–	ns	
$\overline{CS}$ precharge time (Refresh counter test)	t_{CPT}	35	–	40	–	50	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM514412A/AL-70		MSM514412A/AL-80		MSM514412A/AL-10		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write per bit set-up time	t_{WBS}	0	–	0	–	0	–	ns	12
Write per bit hold time	t_{WBH}	10	–	10	–	10	–	ns	12
Write per bit selection set-up time	t_{WDS}	0	–	0	–	0	–	ns	12
Write per bit selection hold time	t_{WDH}	10	–	10	–	10	–	ns	12
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CS}$ before $\overline{RAS}$)	t_{WRP}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CS}$ before $\overline{RAS}$)	t_{WRH}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test mode)	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (Test mode)	t_{WHR}	10	–	10	–	10	–	ns	

Notes: 1. An initial pause of 200 us is required after power-up followed by a minimum of 8 initialization cycles (examples: $\overline{RAS}$-only Refresh or $\overline{CS}$ before $\overline{RAS}$ Refresh) before proper device operation is achieved.

2. The AC measurements assume the transition time (t_T) = 5 ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL}.

4. Measured by using an equivalent load circuit of 2 TTL loads and 100pF.

5. Operating within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RCD} (max.) is for refrence only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, the access time is controlled exclusively by t_{CAC}.

6. Operating within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. The spec. t_{RAD} (max.) is for reference only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled exclusively by t_{AA}.

7. Operating within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. The spec. t_{LWAD} (max.) is for reference only. If t_{LWAD} is greater than the specified t_{LWAD} (max.) limit, the access time is controlled exclusively by t_{AA}.

8. The t_{OFF} (max.) spec. defines at which time the output data achieves a high impedance state and is not referenced to output voltage levels.

9. Either the t_{RRH} or the t_{RCH} spec. must be satisfied for a proper read cycle.

10. The specs t_{WCS}, t_{WH}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet for reference only. If $t_{WCS} \geqq t_{WCS}$ (min.) and $t_{WH} \geqq t_{WH}$ (min.) the cycle is an Early Write cycle and the data out remains in a high impedance state throughout the entire cycle. If $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is Read-Write and data out contains data read from the selected cell. If neither of the above sets of conditions is satisfied the condition of data out is indeterminate at access time.

11. Test Mode Feature:

    The test mode is activated by executing a $\overline{CS}$ before $\overline{RAS}$ refresh cycle with $\overline{WE}$ held at a low level (V_{IL}). The device remains in the test mode until it is deactivated by executing a standard $\overline{RAS}$-only refresh or a $\overline{CS}$ before $\overline{RAS}$ refresh with $\overline{WE}$ held at a high level (V_{IH}).

    In the test mode CA0 is not used and the I/O pin now accesses 2 bit locations. Since all 4 I/O pins are used, a total of 8 data bits can be written in parallel into the memory array, reducing test time by 50%. When executing a read cycle the 2 data bits are gated throughout the internal exclusive OR logic and the result is presented at the I/O pin, thus if the 2 data bits are equal, the I/O pin indicates a logical 1. If the 2 data bits are not equal, the I/O pin indicates a logical 0. This additional internal operation delays access time by 5ns and should be added to the access time parameters if operating in the test mode.

12. Write-Per-Bit Feature:
The addition of a data write-mask register in this multibit wide memory device allows the capability of writing only to the needed data bits in a given address location while leaving the other data bits unaffected.

During execution of a write cycle, including Early Write, Delayed Write or Read-Modify-Write, if $\overline{WB/WE}$ is at a low level (V_{IL}) during the falling edge of $\overline{RAS}$, the data present on the DQi pins is latched into the write-mask register. At this time the DQi pins determine which data bits will be inhibited during the write cycle. A low level (V_{IL}) on a DQi pin indicates that the data bit will be masked or inhibited from being written into the cell during the write cycle. A high level (V_{IH}) on a DQi pin indicates that the data bit will be written into the cell during the write cycle. Refer to Table 1 and Figure 1.

Since the write-mask register is latched by the falling edge of $\overline{RAS}$, it cannot be changed during write cycles. All the write cycles use the same mask data latched at the beginning of the $\overline{RAS}$ cycle.

Table 1 Example of Write-per-Bit Operation

Falling edge of $\overline{RAS}$					Function
$\overline{WB/WE}$	DQ1	DQ2	DQ3	DQ4	
H	X	X	X	X	Normal Write mode: Write enable
L	L	H	L	H	Write-per-Bit mode: Write enable for DQ2, DQ4 Write disable for DQ1, DQ3

X = Don't care

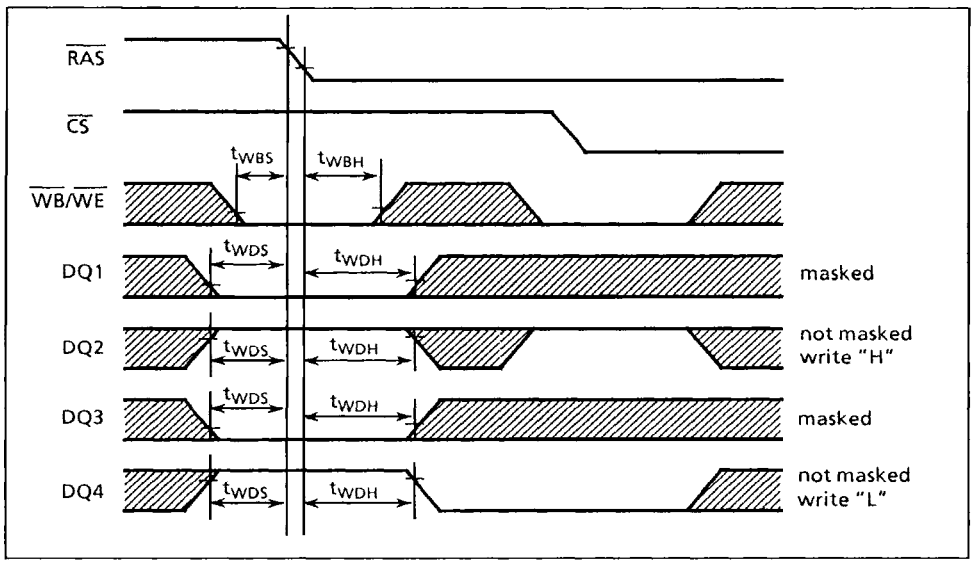
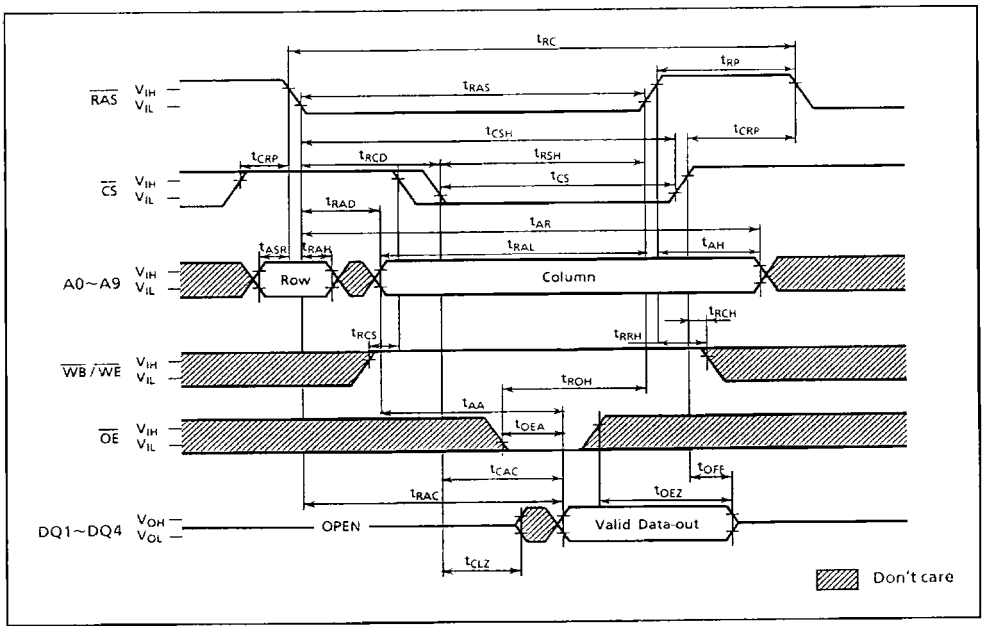
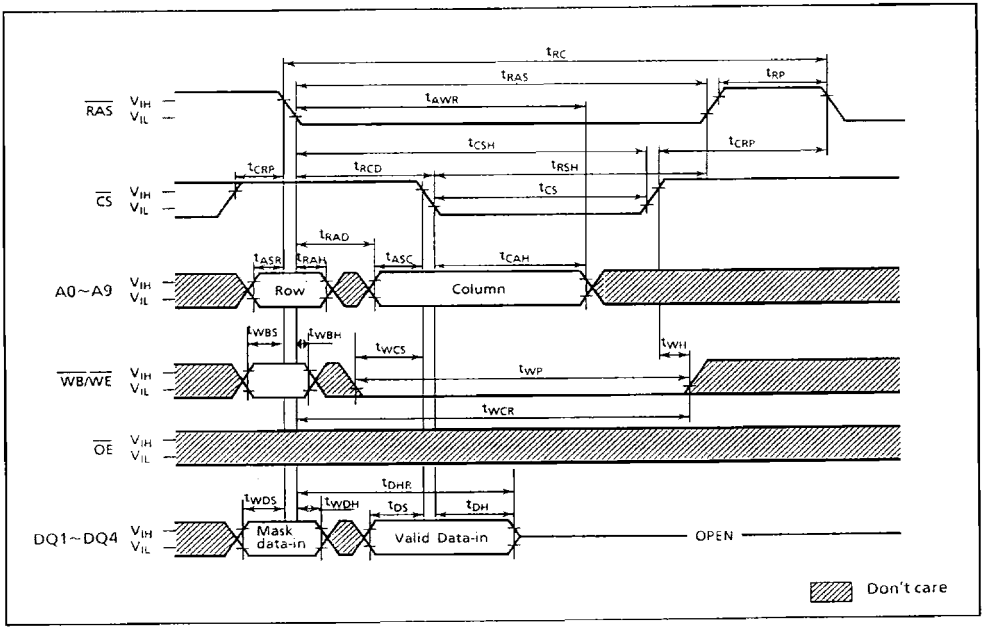


Fig. 1 Example of Write-per-Bit Operation

READ CYCLE



WRITE CYCLE (EARLY WRITE)



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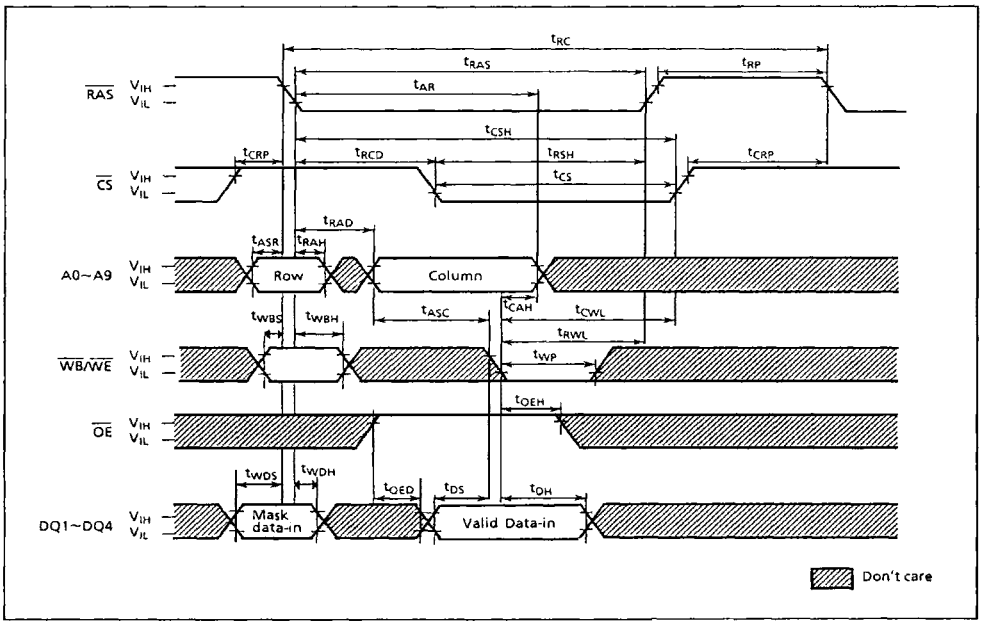
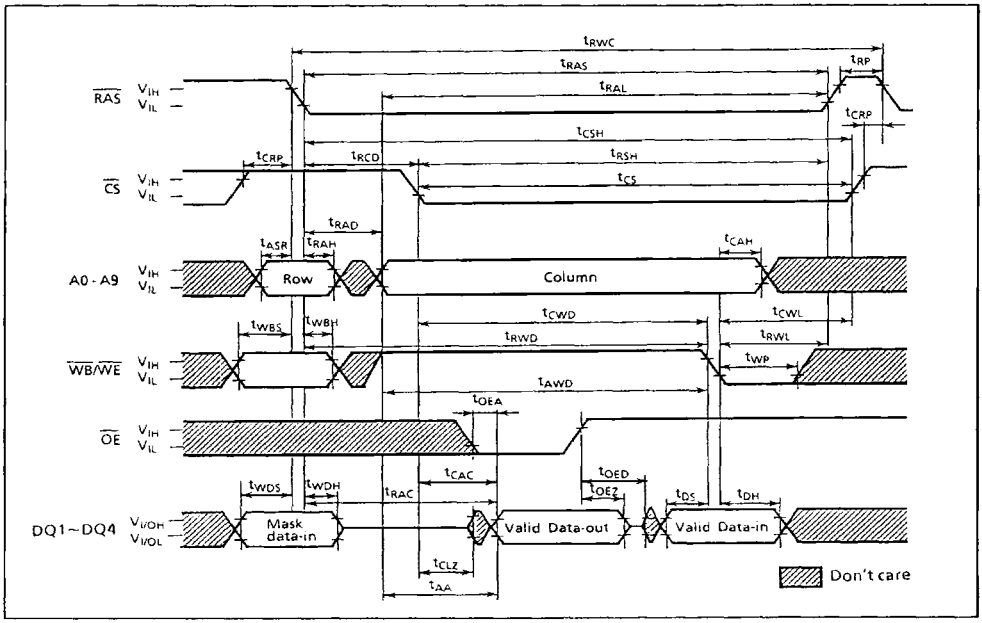
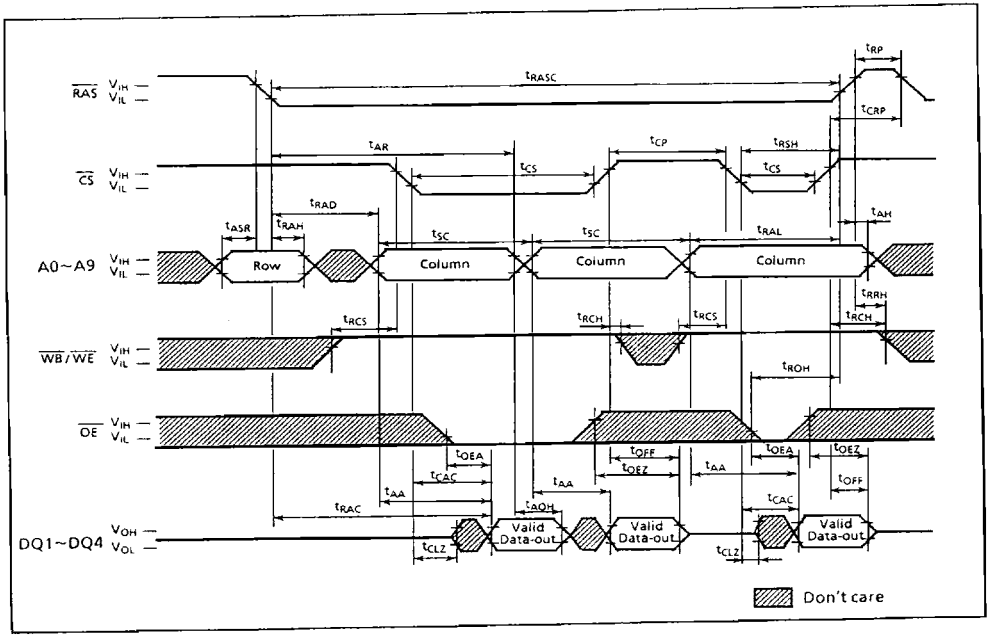
WRITE CYCLE ($\overline{OE}$ CONTROL WRITE)



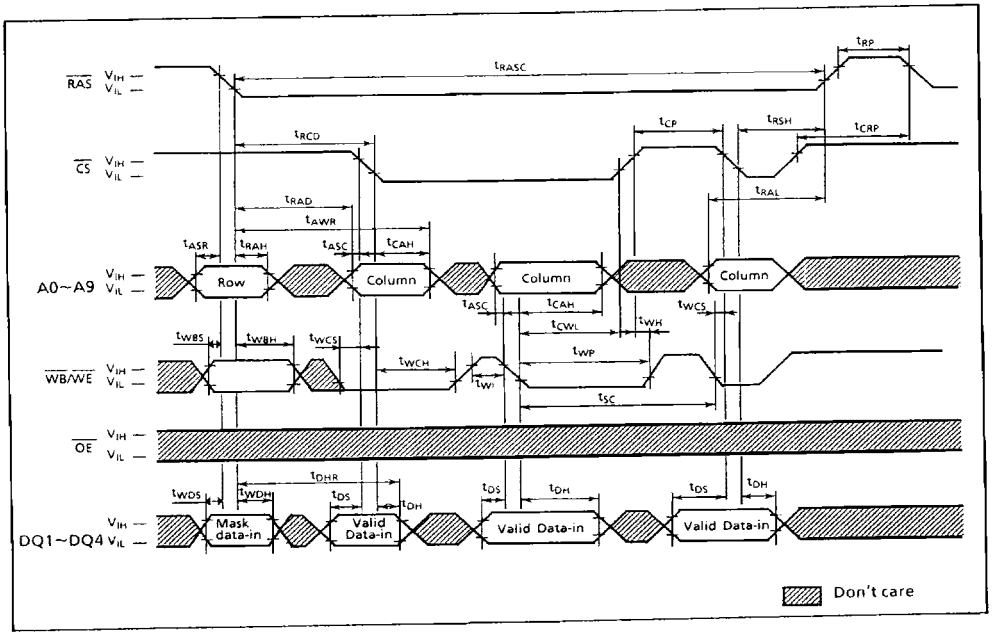
READ/WRITE CYCLE



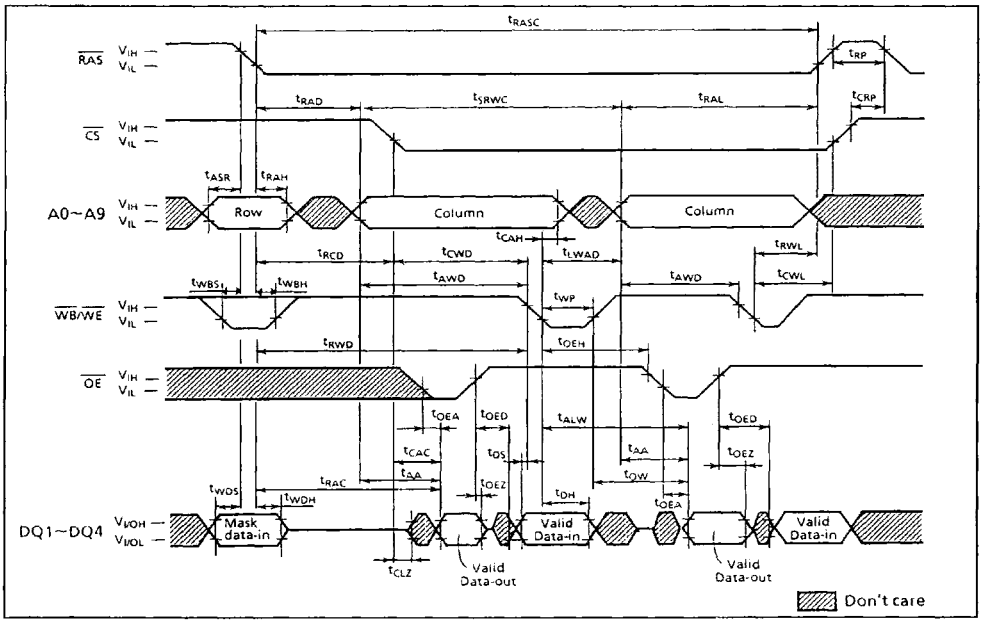
STATIC COLUMN MODE READ CYCLE



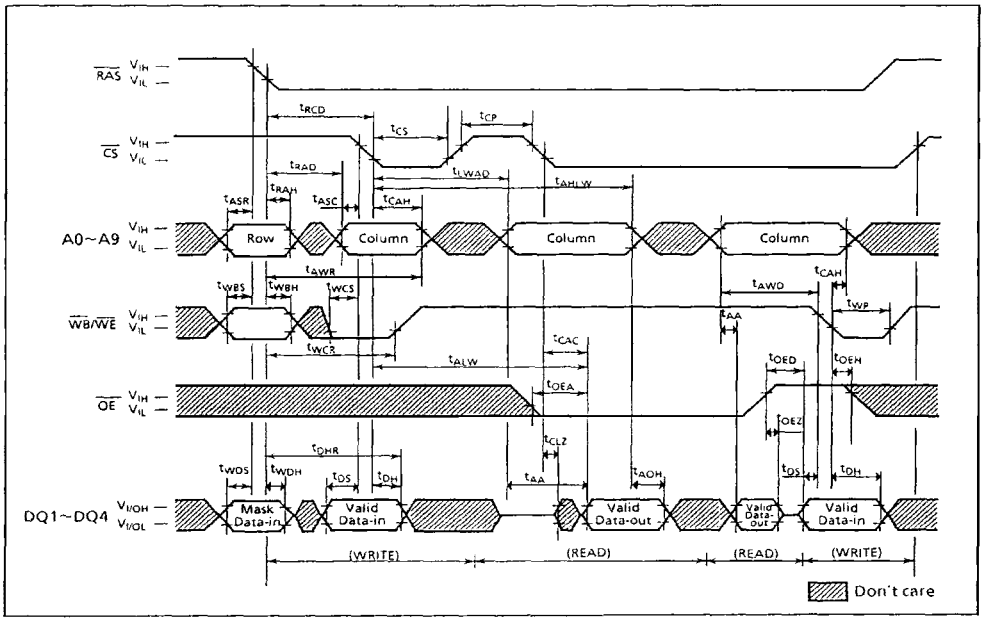
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



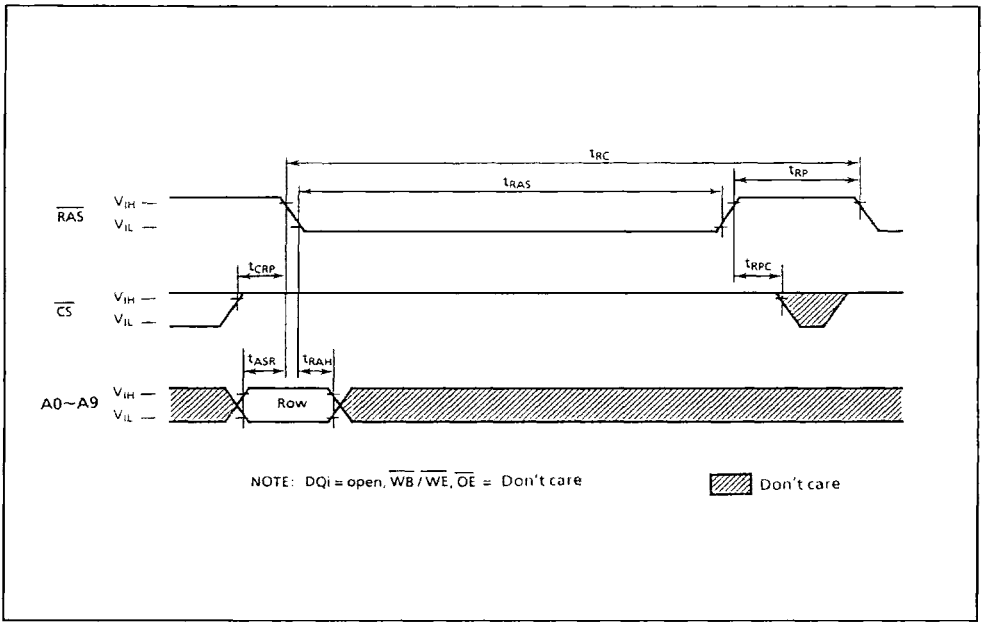
STATIC COLUMN MODE READ/WRITE CYCLE



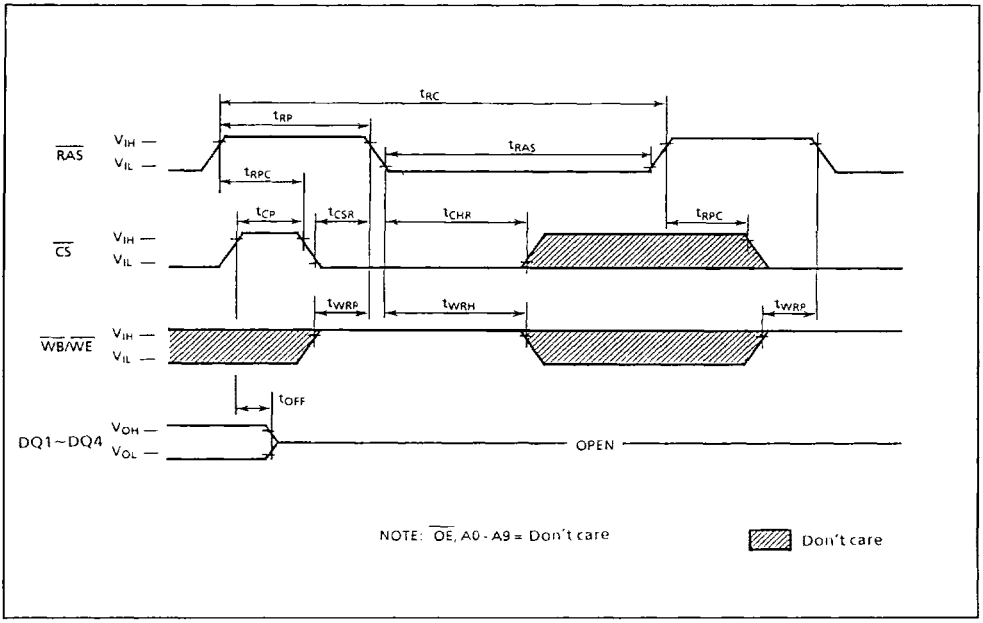
STATIC COLUMN MODE READ/WRITE MIXED CYCLE



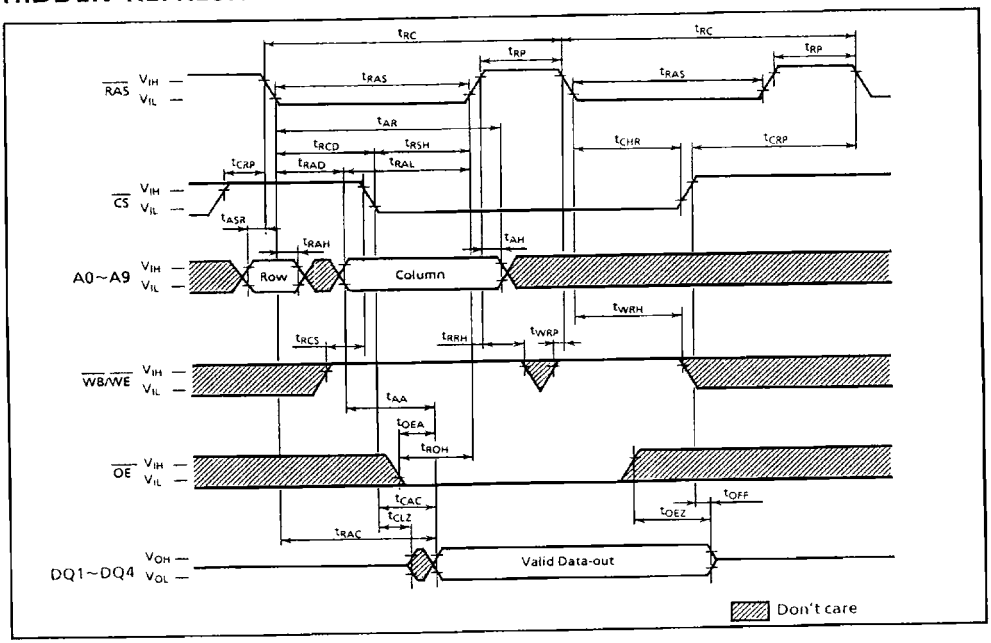
$\overline{\text{RAS}}$-ONLY REFRESH CYCLE



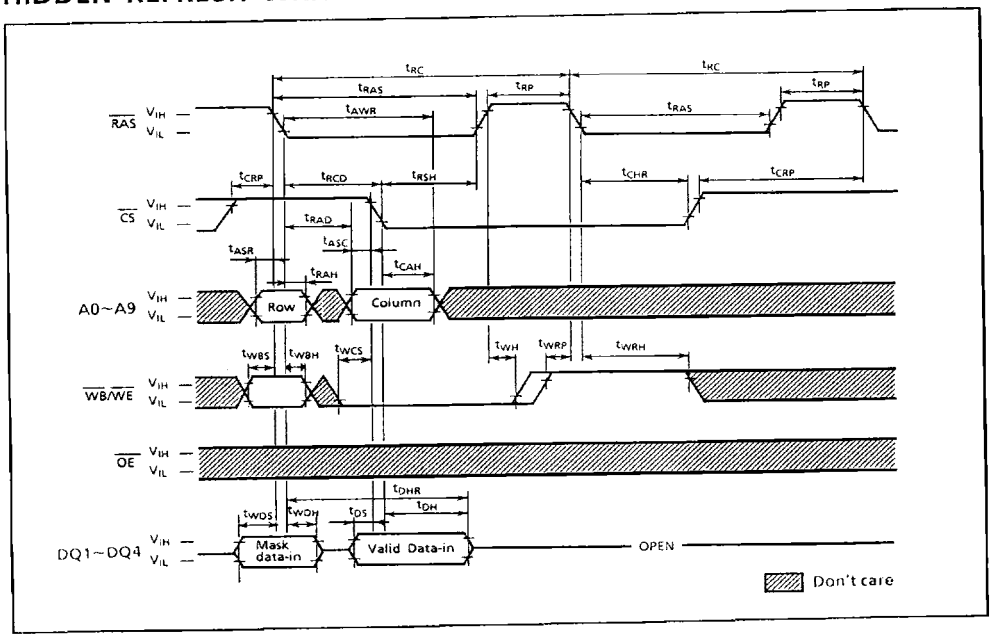
$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ AUTO-REFRESH CYCLE



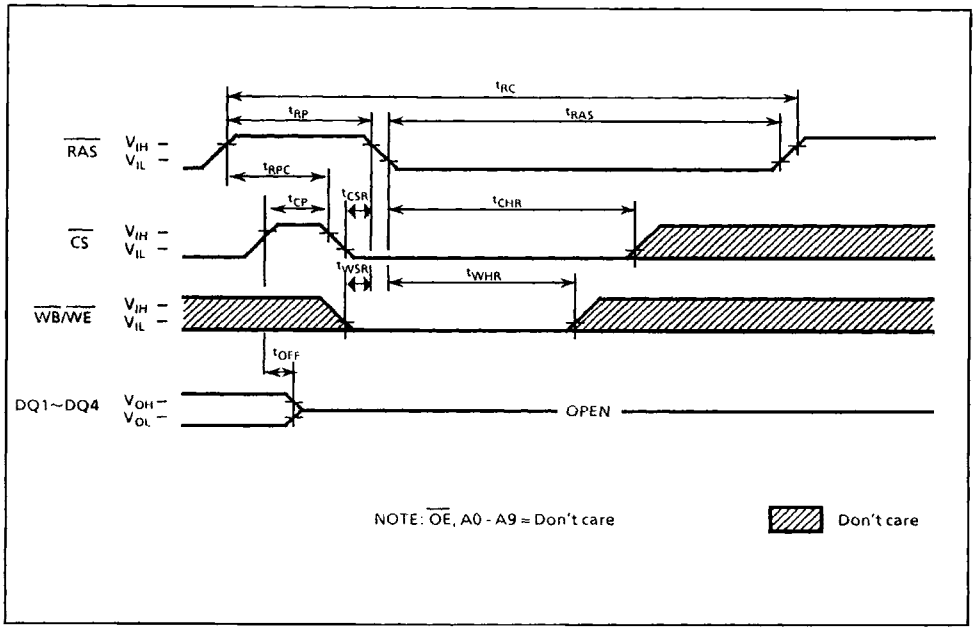
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



TEST MODE INITIATE CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE