Supertex inc.

HV04H
HV06H

64-Channel Serial To Parallel Converter With Ruggedized High Voltage CMOS Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options				
		80-Lead Quad Cerpak Gullwing	80-Lead Quad Plastic Gullwing	80-Lead 35mm TAB Tape	Die	80-Lead Quad Cerpak Gullwing (MIL-STD-883 Processed*)
HV04H	60V	HV04H06DG	HV04H06PG	HV04H06T	HV04H06X	—
	80V	HV04H08DG	HV04H08PG	HV04H08T	HV04H08X	RBHV04H08DG
HV06H	60V	HV06H06DG	HV06H06PG	HV06H06T	HV06H06X	—
	80V	HV06H08DG	HV06H08PG	HV06H08T	HV06H08X	RBHV06H08DG

* For Hi-Rel process flows, please refer to page 5-3 in the Databook.

Features

- ☐ HVCMOS® technology
- ☐ Output voltages up to 80V
- ☐ Low power level shifting
- ☐ Shift register speed 8 MHz
- ☐ Latched data outputs
- ☐ Output polarity and blanking
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}		-0.5V to +15V
Supply voltage, V_{PP}		-0.5V to +80V
Logic input levels		-0.5V to V_{DD} +0.5V
Ground current[3]		3.0A
High voltage supply current[2]		2.6A
Continuous total power dissipation[3]	Ceramic	1900mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to +125°C
Storage temperature range		-65°C to +150°C

Notes:
1. All voltages are referenced to ground.
2. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

General Description

Not recommended for new designs. Please use HV577, with improved performance.

The HV04H and HV06H are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. HVout1 is connected to the first stage of the shift register through the polarity and blanking logic. Data is shifted through the shift register on the low to high transition of the clock. The HV04H shifts data in the counterclockwise direction when viewed from the top of the package and the HV06H shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (HVout64). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) is high. The data in the latch is stored when $\overline{LE}$ is low.

The HV04H and HV06H devices are ruggedized versions of our standard HV04 and HV06. They are designed to be used in circuits where ramping of the high voltage supply is not feasible. Care must be taken to limit the load capacitance and surge current in any particular application.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 8MHz, f_{DATA} = 4MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				0.25	mA	All V_{IN} = 0V or V_{DD}
I_{PP}	High Voltage Supply Current				0.50	mA	V_{PP} = 80V All outputs high
					0.50	mA	V_{PP} = 80V All outputs low
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	µA	V_{IL} = 0V
V_{OH}	High-Level Output	HV_{OUT}	74			V	V_{PP} = 80V, IHV_{OUT} = -20mA
		Data Out	V_{DD} - 1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			6.0	V	V_{PP} = 80V, IHV_{OUT} = +10mA
		Data Out			1.0	V	ID_{OUT} = +100µA
V_{OC}	HV_{OUT} Clamp Voltage				V_{PP} + 1.5	V	I_{OL} = +10mA
					-1.5	V	I_{OL} = -20mA

AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency			8	MHz	
t_W	Clock Width High or Low	62			ns	
t_{SU}	Data Setup Time Before Clock Rises	25			ns	
t_H	Data Hold Time After Clock Rises	10			ns	
t_{WLE}	Width of Latch Enable Pulse	62			ns	
t_{DLE}	$\overline{LE}$ Delay Time Rising Edge of Clock	25			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Rising Edge of Clock	30			ns	
t_{ON}, t_{OFF}	Time from Latch Enable to HV_{OUT}			50	ns	
t_{DHL}	Delay Time Clock to Data High to Low			100	ns	
t_{DLH}	Delay Time Clock to Data Low to High			100	ns	

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	10.8	12	13.2	V
V_{PP}	High voltage supply	-0.3		80	V
V_{IH}	High-level input voltage	V_{DD} - 2V		V_{DD}	V
V_{IL}	Low-level input voltage	0		2.0	V
T_A	Operating free-air temperature	-40		+85	°C

Input and Output Equivalent Circuits

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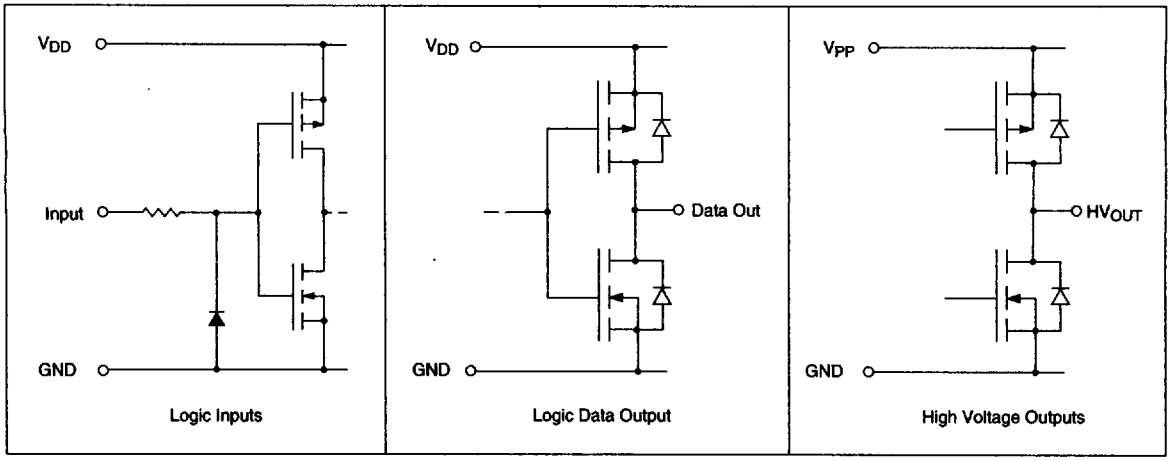
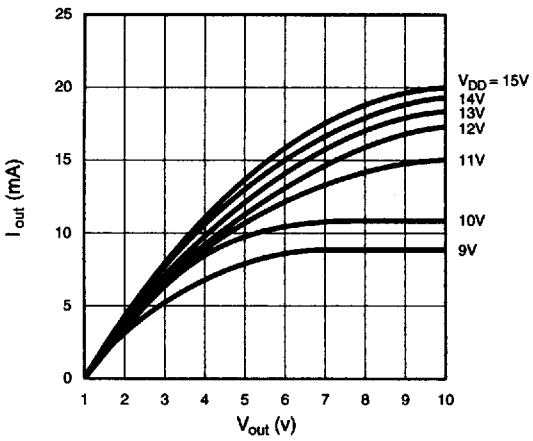
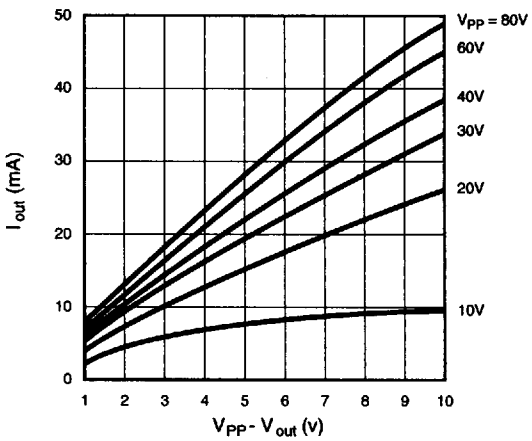


Typical Performance Curves

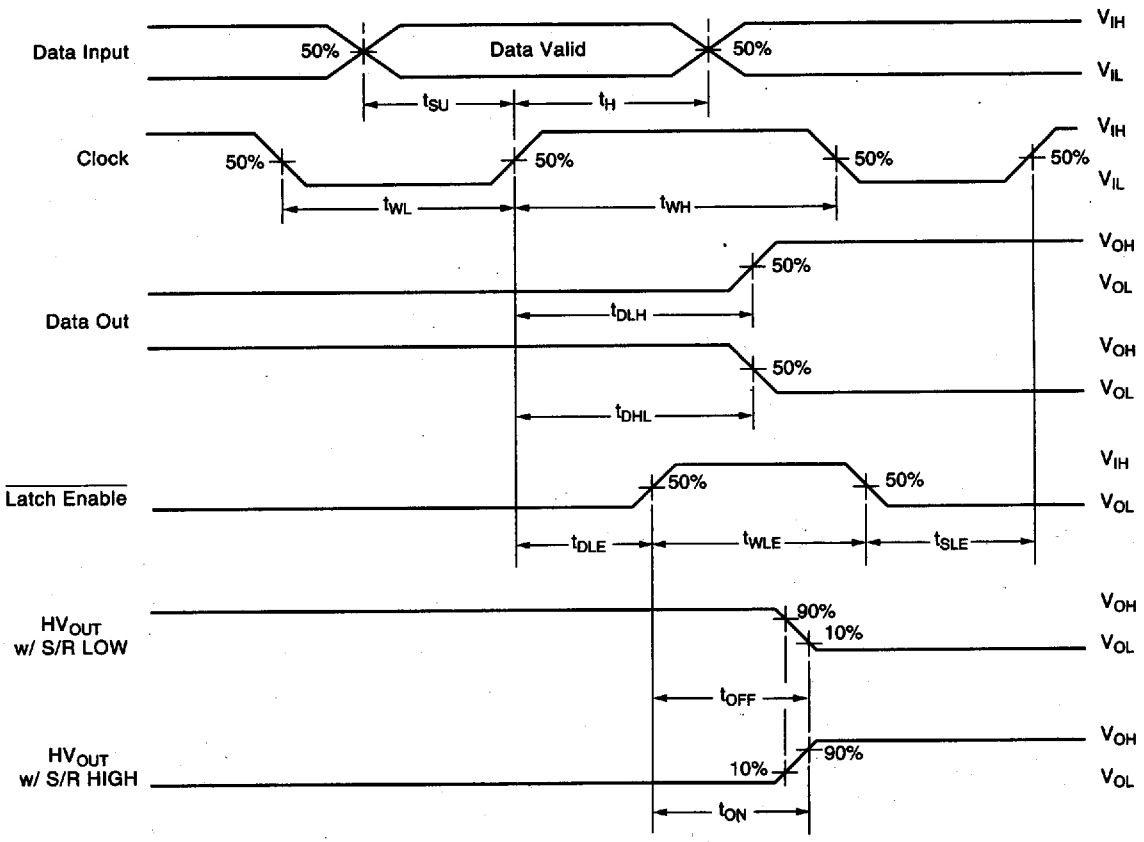
Typical HV04H/06H Source Current @ 25° C



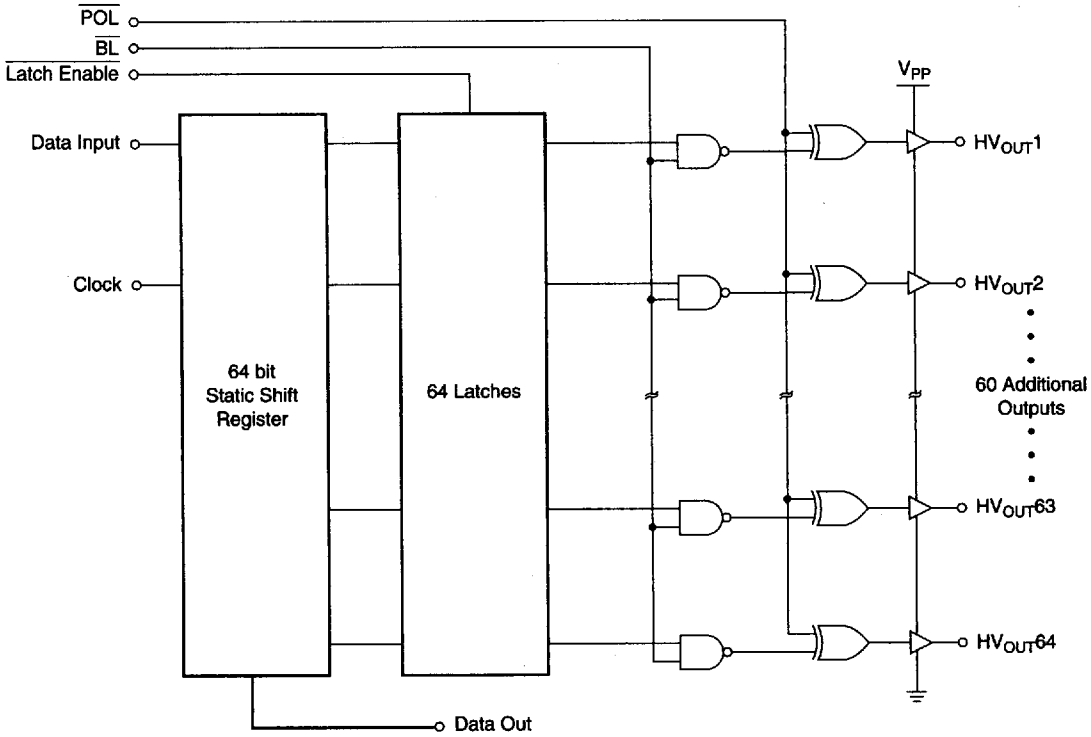
Typical HV04H/06H Source Current @ 25° C



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Outputs				
						Shift Reg		HV Outputs		Data Out
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1	2...64	1	2...64	*
All on	X	X	X	L	L	*	*...*	H	H...H	*
All off	X	X	X	L	H	*	*...*	L	L...L	*
Invert mode	X	X	L	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Load S/R	H or L	↑	L	H	H	H or L	*...*	*	*...*	*
Load Latches	X	H or L	↑	H	H	*	*...*	*	*...*	*
	X	H or L	↑	H	L	*	*...*	$\overline{*}$	$\overline{*...*}$	*
Transparent Latch mode	L	↑	H	H	H	L	*...*	L	*...*	*
	H	↑	H	H	H	H	*...*	H	*...*	*

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

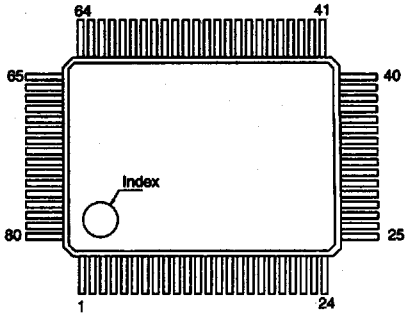
Pin Configurations

PG and DG Packages

HV04H Pin	Function	Pin	Function
1	GND	41	GND
2	V_{PP}	42	V_{PP}
3	HV_{OUT} 59	43	HV_{OUT} 23
4	HV_{OUT} 60	44	HV_{OUT} 24
5	HV_{OUT} 61	45	HV_{OUT} 25
6	HV_{OUT} 62	46	HV_{OUT} 26
7	HV_{OUT} 63	47	HV_{OUT} 27
8	HV_{OUT} 64	48	HV_{OUT} 28
9	$\overline{POL}$	49	HV_{OUT} 29
10	Data Out	50	HV_{OUT} 30
11	CLK	51	HV_{OUT} 31
12	GND	52	HV_{OUT} 32
13	V_{DD}	53	HV_{OUT} 33
14	$\overline{LE}$	54	HV_{OUT} 34
15	Data In	55	HV_{OUT} 35
16	$\overline{BL}$	56	HV_{OUT} 36
17	HV_{OUT} 1	57	HV_{OUT} 37
18	HV_{OUT} 2	58	HV_{OUT} 38
19	HV_{OUT} 3	59	HV_{OUT} 39
20	HV_{OUT} 4	60	HV_{OUT} 40
21	HV_{OUT} 5	61	HV_{OUT} 41
22	HV_{OUT} 6	62	HV_{OUT} 42
23	V_{PP}	63	V_{PP}
24	GND	64	GND
25	HV_{OUT} 7	65	HV_{OUT} 43
26	HV_{OUT} 8	66	HV_{OUT} 44
27	HV_{OUT} 9	67	HV_{OUT} 45
28	HV_{OUT} 10	68	HV_{OUT} 46
29	HV_{OUT} 11	69	HV_{OUT} 47
30	HV_{OUT} 12	70	HV_{OUT} 48
31	HV_{OUT} 13	71	HV_{OUT} 49
32	HV_{OUT} 14	72	HV_{OUT} 50
33	HV_{OUT} 15	73	HV_{OUT} 51
34	HV_{OUT} 16	74	HV_{OUT} 52
35	HV_{OUT} 17	75	HV_{OUT} 53
36	HV_{OUT} 18	76	HV_{OUT} 54
37	HV_{OUT} 19	77	HV_{OUT} 55
38	HV_{OUT} 20	78	HV_{OUT} 56
39	HV_{OUT} 21	79	HV_{OUT} 57
40	HV_{OUT} 22	80	HV_{OUT} 58

HV06H Pin	Function	Pin	Function
1	GND	41	GND
2	V_{PP}	42	V_{PP}
3	HV_{OUT} 6	43	HV_{OUT} 42
4	HV_{OUT} 5	44	HV_{OUT} 41
5	HV_{OUT} 4	45	HV_{OUT} 40
6	HV_{OUT} 3	46	HV_{OUT} 39
7	HV_{OUT} 2	47	HV_{OUT} 38
8	HV_{OUT} 1	48	HV_{OUT} 37
9	$\overline{POL}$	49	HV_{OUT} 36
10	Data Out	50	HV_{OUT} 35
11	CLK	51	HV_{OUT} 34
12	GND	52	HV_{OUT} 33
13	V_{DD}	53	HV_{OUT} 32
14	$\overline{LE}$	54	HV_{OUT} 31
15	Data In	55	HV_{OUT} 30
16	$\overline{BL}$	56	HV_{OUT} 29
17	HV_{OUT} 64	57	HV_{OUT} 28
18	HV_{OUT} 63	58	HV_{OUT} 27
19	HV_{OUT} 62	59	HV_{OUT} 26
20	HV_{OUT} 61	60	HV_{OUT} 25
21	HV_{OUT} 60	61	HV_{OUT} 24
22	HV_{OUT} 59	62	HV_{OUT} 23
23	V_{PP}	63	V_{PP}
24	GND	64	GND
25	HV_{OUT} 58	65	HV_{OUT} 22
26	HV_{OUT} 57	66	HV_{OUT} 21
27	HV_{OUT} 56	67	HV_{OUT} 20
28	HV_{OUT} 55	68	HV_{OUT} 19
29	HV_{OUT} 54	69	HV_{OUT} 18
30	HV_{OUT} 53	70	HV_{OUT} 17
31	HV_{OUT} 52	71	HV_{OUT} 16
32	HV_{OUT} 51	72	HV_{OUT} 15
33	HV_{OUT} 50	73	HV_{OUT} 14
34	HV_{OUT} 49	74	HV_{OUT} 13
35	HV_{OUT} 48	75	HV_{OUT} 12
36	HV_{OUT} 47	76	HV_{OUT} 11
37	HV_{OUT} 46	77	HV_{OUT} 10
38	HV_{OUT} 45	78	HV_{OUT} 9
39	HV_{OUT} 44	79	HV_{OUT} 8
40	HV_{OUT} 43	80	HV_{OUT} 7

Package Outline



top view

80-pin Gullwing Package