DEVICE ENGINEERING INCORPORATED

deiaz.com

# DEI1026A
# Six Channel Discrete-to-Digital Interface Sensing Open/Ground Signals

## Features

- Senses six Open/Ground Inputs
- Inputs are lightning protected to DO-160G Level 3
- ABD0100 compliant input voltage threshold
- TTL/CMOS-Compatible Tri-State Outputs
- Package / Temperature Options:
  - 16 lead .150" SOIC, -55 °C /+85 °C or 125 °C
  - 16 lead Ceramic 300 mil SOP, -55 °C /+125 °C


SOIC package option

## Functional Description

The DEI1026A is a six channel discrete-to-digital interface BiCMOS device. It senses six Open/Ground discrete signals of the type commonly found in avionic systems. The inverted 3-state outputs are TTL/CMOS compatible and are enabled by the $\overline{OE}$ and $\overline{CE}$ pins. The inputs are lightning protected to meet the requirements of DO160D Sec 22 Waveforms 3, 4, and 5, Level 3. See figures 5-7. The device is available in a 16 lead .150" SOIC and .300" Ceramic SOP.

With its reliability, low cost, operating range, and lightning protection, the DEI1026A meets a large variety of interface requirements for aerospace applications.

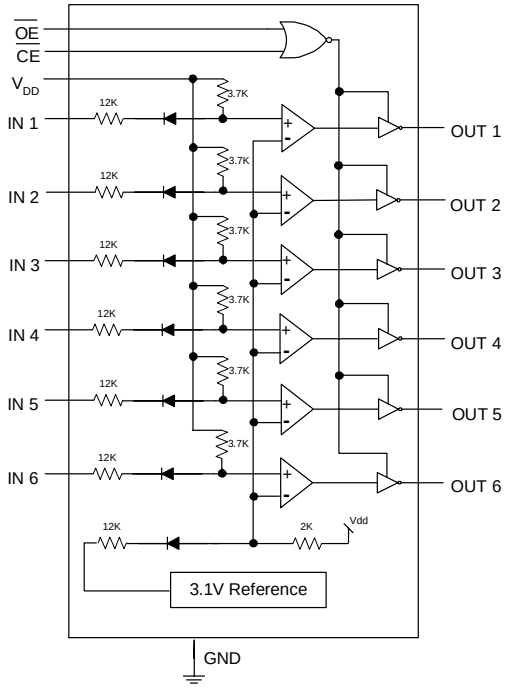



**Figure 1: Concept Drawing**

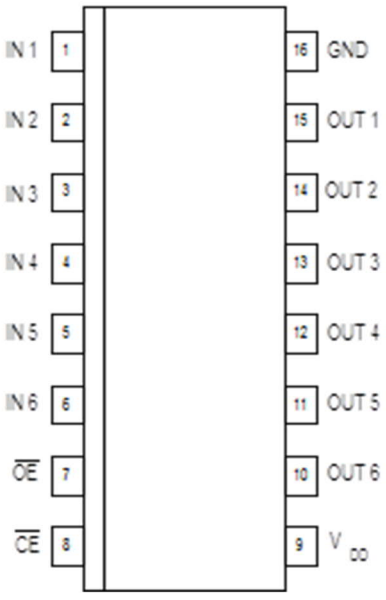



**Figure 2: Pinout Diagram**

# Electrical Characteristics

| Table 1: Absolute Maximum Ratings | | | | |
|---|---|---|---|---|
| **PARAMETER** | | **MIN** | **MAX** | **UNITS** |
| Supply Voltage $V_{DD}$ | | -0.3 | 7.0 | V |
| Discrete Input Voltage (Pins 1-6) | | -5 | +40 * | V |
| Digital Input Voltage ($\overline{CE}$ and $\overline{OE}$) | | $V_{SS}$ - 0.3 | $V_{DD}$ + 0.3 | V |
| Lightning Protection (Pins 1-6)<br>DO160G, Waveform 3; Level 3 pin injection<br>DO160G, Waveforms 4, and 5; Level 3 pin injection | | <br>-660<br>-330 | <br>+660<br>+330 | V |
| Junction Temperature | | | 145 | °C |
| Storage Temperature | Plastic<br>Ceramic | -65<br>-55 | 150<br>150 | °C |
| Operating Free Air Temperature | Plastic<br>Ceramic | -55<br>-55 | 85<br>125 | °C |
| Peak Body Temperature<br>Plastic, G Package<br>Ceramic | | | <br>260<br>240 | °C |
| The DEI1026A contains circuitry to protect inputs from damage due to electrostatic discharge. It has been characterized per JESD22-A114 Human Body Model to Class 1C. Observe precautions for handling and storing Electrostatic Sensitive Devices. | | | | |
| * The DEI1026A will withstand the transient surge DC voltage step function loci limits for category B equipment per MIL-STD-704A. | | | | |

| Table 2: DEI1026A Device Operating Characteristics | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** |
| Supply Voltage | $V_{DD}$ | | 4.5 | 5.0 | 5.5 | V |
| Free Air Operating Temp. | $T_A$ | $V_{DD}$ = 4.5 – 5.5 V<br>Plastic<br>Ceramic | <br>-55<br>-55 | | <br>85<br>125 | °C |
| Logic Output Sink Current | $I_{OL}$ | $V_{DD}$ = 4.5 – 5.5 V | | | 5.0 | mA |
| Logic Output Source Current | $I_{OH}$ | $V_{DD}$ = 4.5 – 5.5 V | -5.0 | | | mA |

| Table 3: DEI1026A Logic Truth Table | | | |
|---|---|---|---|
| **/CE<br>Chip Enable** | **/OE<br>Output Enable** | **$IN_N$<br>Discrete Input** | **$OUT_N$<br>Output** |
| 0 | 0 | Open | 0 |
| 0 | 0 | Ground | 1 |
| 1 | X | X | High Z |
| X | 1 | X | High Z |

| Table 4A: DEI1026A-SES Electrical Characteristics ($T_A$ = -55°C to +85°C , $V_{DD}$ = 4.5 to 5.5 V, Unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **Power Supply Characteristics** | | | | | | |
| Supply Current | $I_{DD}$ | $V_{IN} = V_{DD}$ (all inputs)<br>$V_{DD}$ = 5.5 V | | 5 | 10 | mA |
| **Discrete Input Characteristics** | | | | | | |
| Ground state input voltage | $V_{SG}$ | Voltage source from input terminal to ground for Logic High Output. | | | 3.5 | V |
| Open state input voltage | $V_{SO}$ | Voltage source from input terminal to ground for Logic Low Output. | 4.1 | | | V |
| Ground state input resistor | $R_{IG}$ | Resistor from input to ground to guarantee Logic High Output. | 0 | | 100 | Ω |
| Open state input resistor | $R_{IO}$ | Resistor from input to ground to guarantee Logic Low Output. | 500k | | | Ω |
| Input source current | $I_{IO}$ | Current sourced into 100 Ohm resistor to Ground. | -100 | -330 | | µA |
| Reverse leakage current | $I_{IR}$ | $V_{IN}$ = 35 V, $V_{DD}$ = 0 V | | | 100 | µA |
| **Logic Input Characteristics** | | | | | | |
| $\overline{CE}$, $\overline{OE}$ input logic 1 level | $V_{IH}$ | | 2.0 | | | V |
| $\overline{CE}$, $\overline{OE}$ input logic 0 level | $V_{IL}$ | | | | 0.8 | V |
| **DC Output Characteristics** | | | | | | |
| Output logic 1 level (TTL) | $V_{OH}$ | $I_{OH}$ = -5 mA | 2.4 | | | V |
| Output logic 0 level (TTL) | $V_{OL}$ | $I_{OL}$ = 5 mA (2) | | | 0.4 | V |
| Output logic 1 level (CMOS) | $V_{OH}$ | $I_{OH}$ = -100 µA | $V_{DD}$ – 50mV | | | V |
| Output logic 0 level (CMOS) | $V_{OL}$ | $I_{OL}$ = 100 µA | | | $V_{SS}$ + 50mV | V |
| Off-state Output Current | $I_{OZ}$ | $\overline{OE}$ = $V_{DD}$<br>$V_{DD}$ = 5.5 V<br>$V_{OUT}$ = 0 or $V_{DD}$ | | | +/-10 | µA |
| **Switching Characteristics [1]** | | | | | | |
| I/O propagation delay | $t_{HL}$, $t_{LH}$ | Refer to Figure 4. | | | 150 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output low) to output HI-Z | $t_{LZ}$ | Refer to Figure 3. | | | 25 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output low | $t_{ZL}$ | Refer to Figure 3. | | | 25 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output high) to output HI -Z | $t_{HZ}$ | Refer to Figure 3. | | | 25 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output high | $t_{ZH}$ | Refer to Figure 3. | | | 25 | ns |

| Table 4B: DEI1026A-xMx Electrical Characteristics ($T_A$ = -55°C to +125°C, $V_{DD}$ = 4.5 to 5.5 V, Unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **UNITS** |
| **Power Supply Characteristics** | | | | | | |
| Supply Current | $I_{DD}$ | $V_{IN}$ = $V_{DD}$ (all inputs)<br>$V_{DD}$ = 5.5 V | | 5 | 10 | mA |
| **Discrete Input Characteristics** | | | | | | |
| Ground state input voltage | $V_{SG}$ | Voltage source from input terminal to ground for Logic High Output. | | | 3.5 | V |
| Open state input voltage | $V_{SO}$ | Voltage source from input terminal to ground for Logic Low Output. | 4.1 | | | V |
| Ground state input resistor | $R_{IG}$ | Resistor from input to ground to guarantee Logic High Output. | 0 | | 100 | Ω |
| Open state input resistor | $R_{IO}$ | Resistor from input to ground to guarantee Logic Low Output. | 500k | | | Ω |
| Input source current | $I_{IO}$ | Current sourced into 100 Ohm resistor to Ground. | -100 | -330 | | μA |
| Reverse leakage current | $I_{IR}$ | $V_{IN}$ = 35 V, $V_{DD}$ = 0 V | | | 100 | μA |
| **Logic Input Characteristics** | | | | | | |
| $\overline{CE}$, $\overline{OE}$ input logic 1 level | $V_{IH}$ | | 2.0 | | | V |
| $\overline{CE}$, $\overline{OE}$ input logic 0 level | $V_{IL}$ | | | | 0.8 | V |
| **DC Output Characteristics** | | | | | | |
| Output logic 1 level (TTL) | $V_{OH}$ | $I_{OH}$ = -5 mA | 2.4 | | | V |
| Output logic 0 level (TTL) | $V_{OL}$ | $I_{OL}$ = 5 mA (2) | | | 0.4 | V |
| Output logic 1 level (CMOS) | $V_{OH}$ | $I_{OH}$ = -100 μA | $V_{DD}$ – 50mV | | | V |
| Output logic 0 level (CMOS) | $V_{OL}$ | $I_{OL}$ = 100 μA | | | $V_{SS}$ + 50mV | V |
| Off-state Output Current | $I_{OZ}$ | $\overline{OE}$ = $V_{DD}$<br>$V_{DD}$ = 5.5 V<br>$V_{OUT}$ = 0 or $V_{DD}$ | | | +/-10 | μA |
| **Switching Characteristics [1]** | | | | | | |
| I/O propagation delay | $t_{HL}$, $t_{LH}$ | Refer to Figure 4. | | | 170 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output low) to output HI-Z | $t_{LZ}$ | Refer to Figure 3. | | | 30 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output low | $t_{ZL}$ | Refer to Figure 3. | | | 30 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output high) to output HI -Z | $t_{HZ}$ | Refer to Figure 3. | | | 30 | ns |
| Delay from $\overline{CE}$ or $\overline{OE}$ input (with output HI-Z) to output high | $t_{ZH}$ | Refer to Figure 3. | | | 30 | ns |

Notes:

1. Guaranteed by design and not production tested.
2. Limit the sum of all IOL currents to 20 ma. The Vsg spec may exceed limit beyond this current.

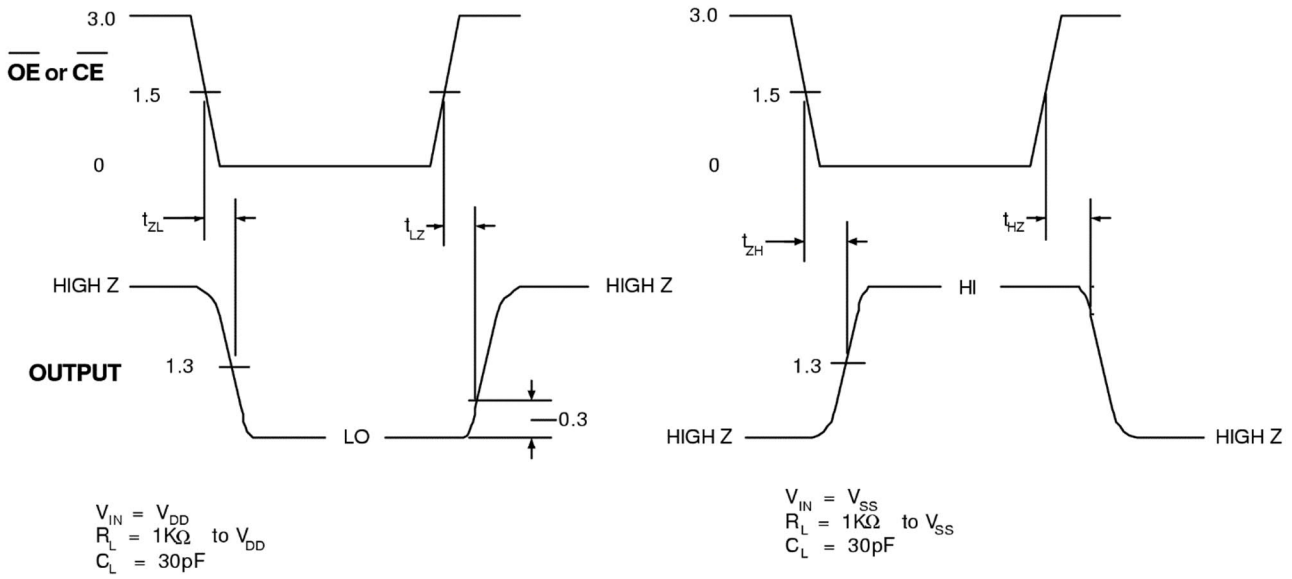
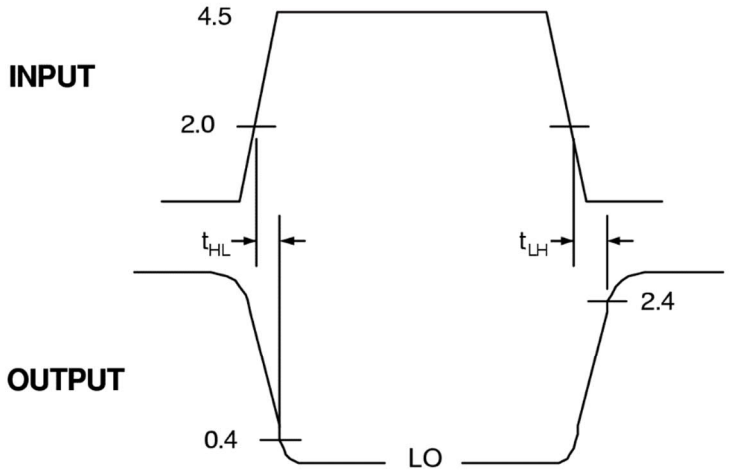



**Figure 3: Enable to Output Propagation Delay**




$R_L$ = 1K Ω to $V_{DD}$
$C_L$ = 30pF

**Figure 4: Input to Output Propagation Delay**

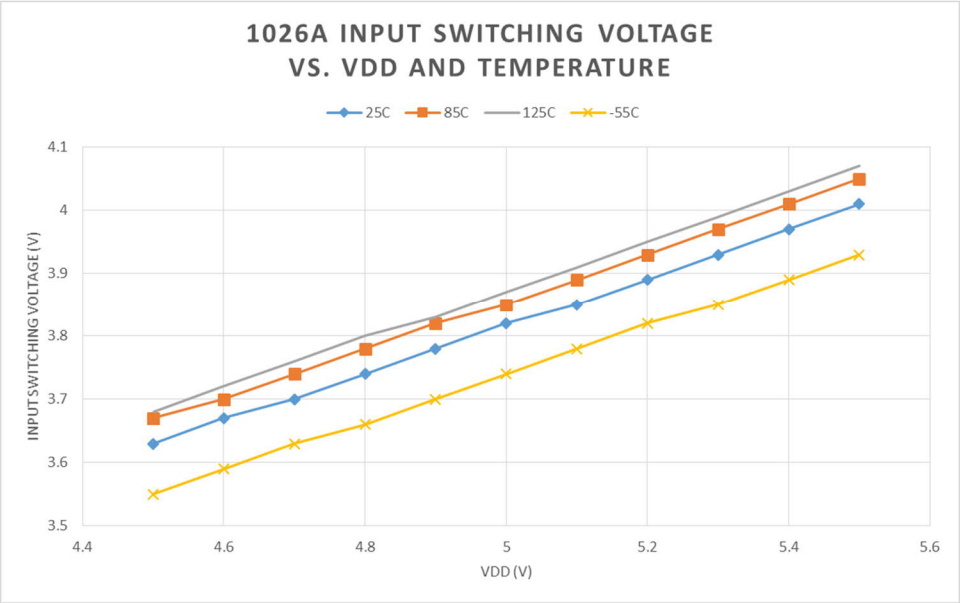



**Figure 5 Input Switching Threshold Voltage Characteristics**

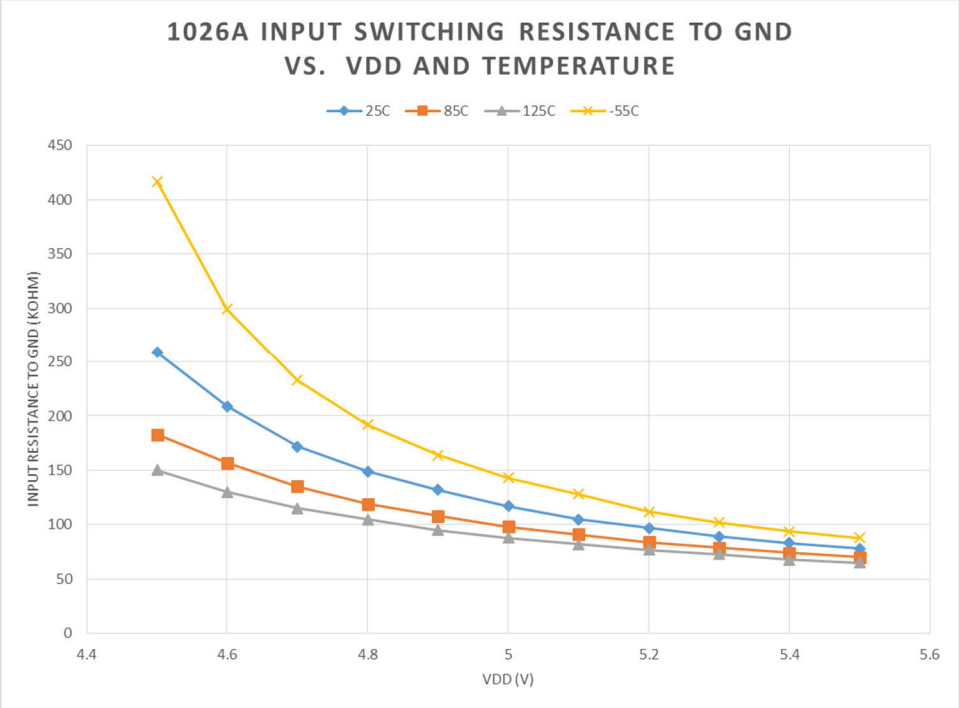
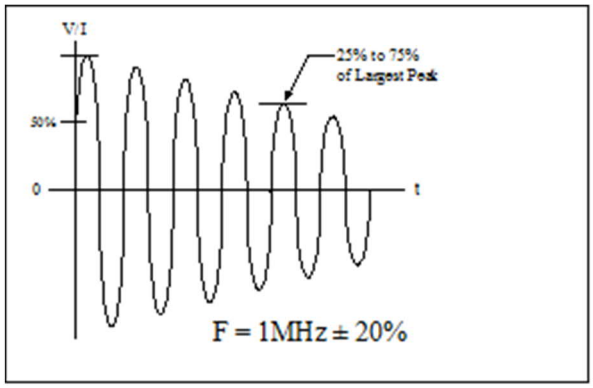
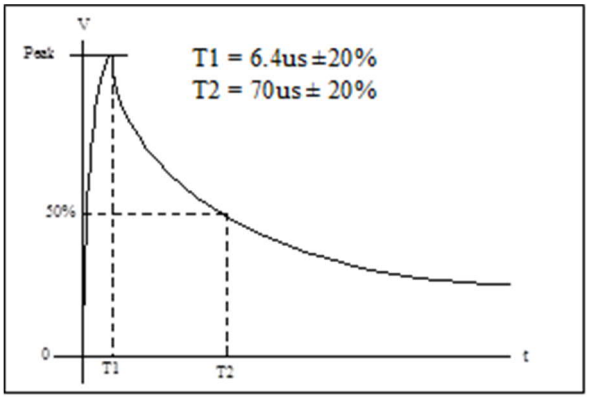



**Figure 6 Input Switching Resistance to Ground Characteristics**



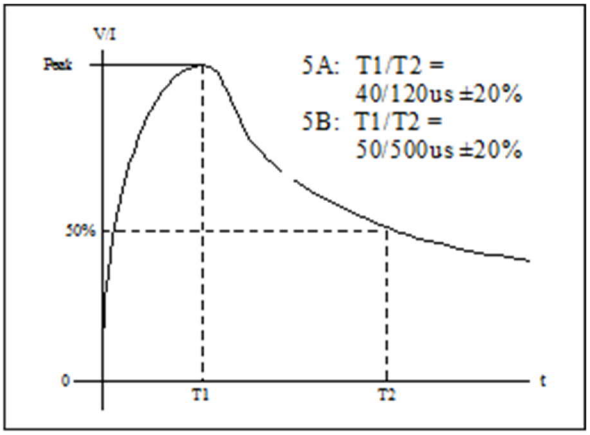

DO160 WF3 Voc/Isc Waveform




DO160 WF4 Voc/Isc Waveform

Notes:

1. DO160G pin injection Level 3 waveforms.
2. Voltage tolerance: +20%, -0%
3. Waveform Source Impedance characteristics:
   - Waveform 3 Voc/Isc = 600 V / 24 A => 25 Ω
   - Waveform 4 Voc/Isc = 300 V / 60 A => 5 Ω
   - Waveform 5A Voc / Isc = 300V / 300A => 1 Ω




DO160 WF5 Voc/Isc Waveform

**Figure 7 DO160G Pin Injection Test Waveforms**

## Package Characteristics

**Table 5: Package Characteristics**

| PACKAGE TYPE | 16 Lead SOIC Narrow Body, Green | 16 Lead Ceramic SOP |
|---|---|---|
| REFERENCE | 16L SOIC NB G | 16L CSOP |
| **THERMAL RESISTANCE:** | | |
| $\theta_{JA}$ (4 layer PCB with Power Planes) | ~74 °C/W | - |
| $\theta_{JC}$ | ~30 °C/W | 23 °C/W |
| JEDEC MOISTURE SENSITIVITY LEVEL (MSL) | MSL 1 / 260°C | Hermetic |
| LEAD FINISH MATERIAL / JEDEC Pb-free CODE | NiPdAu e4 | Au e4 |
| Pb-Free DESIGNATION | RoHS Compliant | Pb Free |
| JEDEC REFERENCE | MS-012-AC | - |

**16L SOIC NB G**

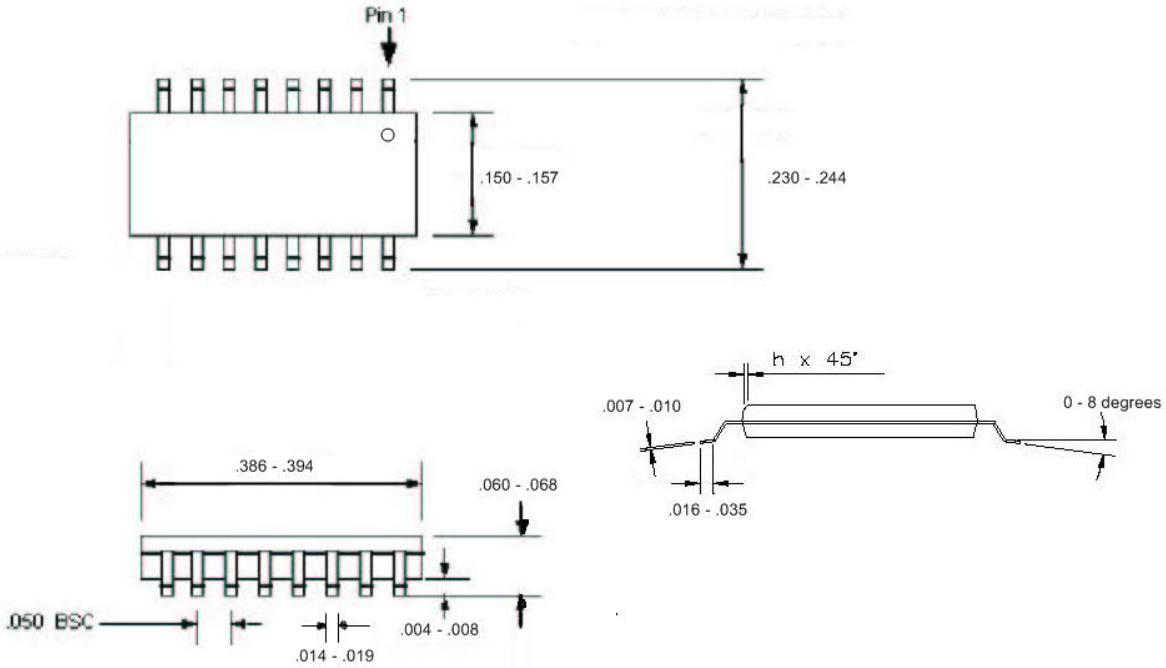



**Figure 8: 16L SOIC Mechanical Outline**

**16L CSOP**

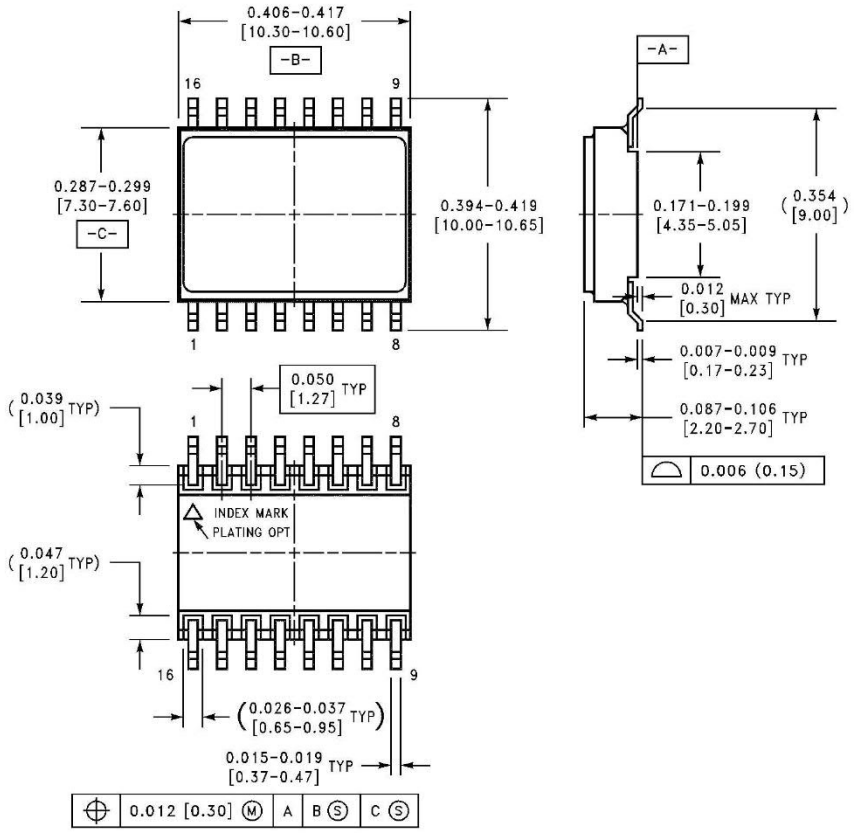



**Figure 9: 16L CSOP Mechanical Outline**

## Ordering Information

**Table 6: Ordering Information**

| DEI PART NUMBER | MARKING (1) | PACKAGE | OP. TEMP. RANGE | PROCESSING |
|---|---|---|---|---|
| DEI1026A-SES-G | DEI1026A-SES E4 | 16L SOIC NB G | -55 / +85 ºC | Standard |
| DEI1026A-SMS-G | DEI1026A-SMS E4 (3) | 16L SOIC NB G | -55 / +125 ºC | Standard |
| DEI1026A-WMS | DEI1026A-WMS | 16 lead ceramic SOP | -55 / +125 ºC | Standard |
| DEI1026A-WMB | DEI1026A-WMB | 16 lead ceramic SOP | -55 / +125 ºC | Burn In, 96 hr @ 125 ºC |

NOTES:
1. All packages marked with Lot Code and Date Code.
2. "E4" after Date Code Denotes Pb Free category.
3. Alternate marking is –SES + Blue Dot