Standard Products

ACT15530 CMOS Manchester Encoder / Decoder

www.aeroflex.com/Avionics

May 16, 2005

FEATURES

- MIL-STD-1553 Compatible
- 1.25 Megabit/sec Maximum Data Rate
- Sync Identification and Lock-in
- Clock Recovery
- Manchester II Encode / Decode
- Separate Encoder and Decoder Sections
- Low Operating Power
- Monolithic – Single Chip Construction
- Several Package and Quality Options (Consult Factory for Details)
- Direct Replacement for the Obsolete Harris HD15530-9/-2/8 and GEC Plessey Marconi MAS15530 / CT15530 parts
- Military Temperatue Range -55°C to +125°C
- Designed for Commercial, Industrial and Aerospace Applications
- Aeroflex-Plainview is a Class H & K MIL-PRF-38534 Manufacturer

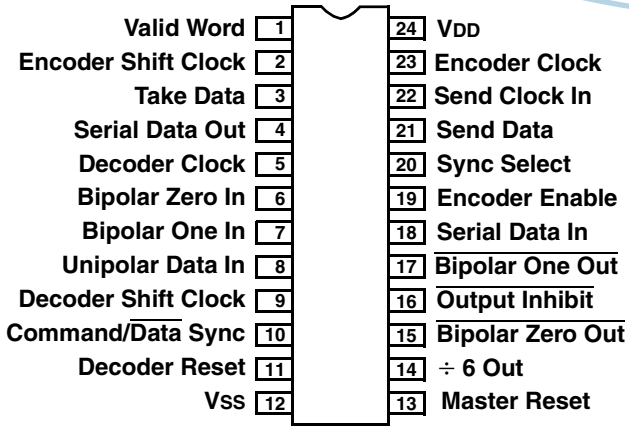
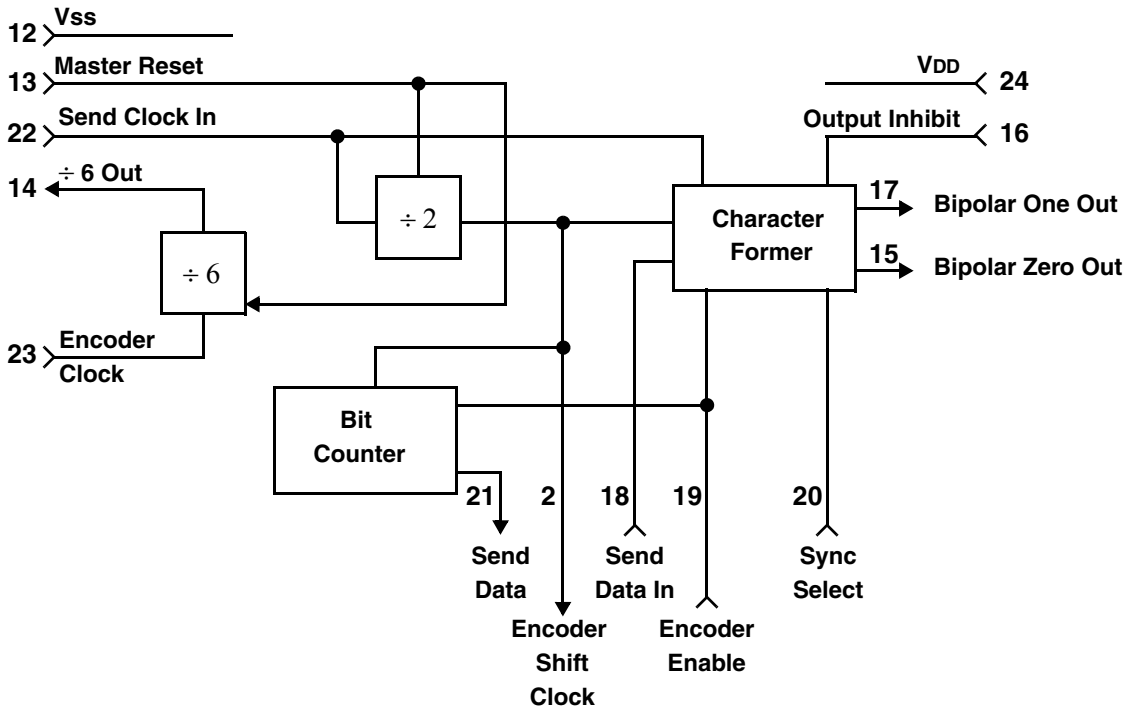


Figure 1: Pin Assignments
(24-Pin DIP/Flat Package – See Figure 18 for LCC Pkg)

DESCRIPTION

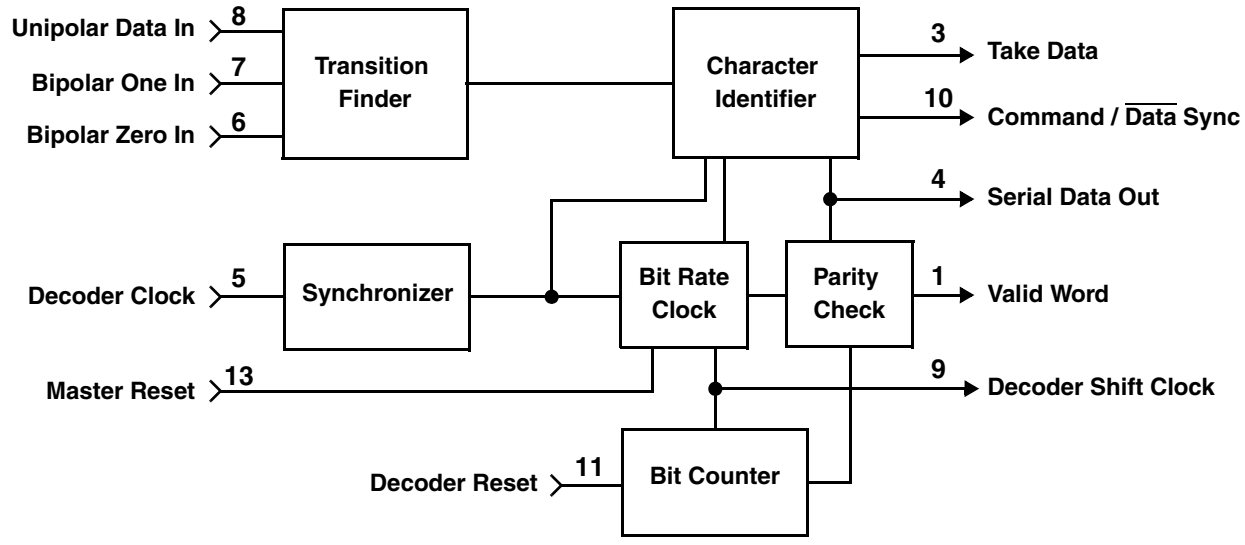
The Aeroflex-Plainview ACT15530 is a high performance CMOS integrated circuit used to implement MIL-STD-1553 and similar Manchester II encoded, time division multiplexed, serial data protocols. The device is divided into two independent sections, encoder and decoder, with a common master reset. The function of the encoder section is to produce the sync pulse and parity bit, and encode the data bits. The decoder section recognizes the sync pulse, decodes the data bits and checks for parity.

The ACT15530 is fully guaranteed to support the 1 MHz data rate of MIL-STD-1553 over the full temperature and supply voltage ranges. The device interfaces with CMOS, TTL or N-Channel support circuitry and operates from a standard 5 volt supply. The circuit can also be used in many party line digital data communications applications where high reliability command and control signals are required. Using Aeroflex transceivers products (4400 Series) the Bit Error Rates (BER) and Word Error Rates (WER) of MIL-STD-1553 can be achieved (Refer to MIL-STD-1553 Multiplex Applications Handbook "MIL-HDBK-1553").



Note: All Pin designations are for 24-Pin DIP & Flatpak

Figure 2: Encoder Block Diagram



Note: All Pin designations are for 24-Pin DIP & Flatpak

Figure 3: Decoder Block Diagram

PIN DESIGNATIONS

Pin	Input	Output	Enc	Dec	Function	Comment
1		✓		✓	Valid word	A 'high' signals the receipt of a valid word
2		✓	✓		Encoder Shift Clock	Shifts data into the encoder on a 'low' to 'high' transition
3		✓		✓	Take Data	'high' during data reception after the sync pulse is identified
4		✓		✓	Serial Data Out	NRZ output of received data
5	✓			✓	Decoder clock	Clock for the transition finder and synchronizer which generates the clock for the rest of the decoder
6	✓			✓	Bipolar Zero In	Should be 'high' when the bus is in a negative state. Must be tied 'high' when the unipolar input is used
7	✓			✓	Bipolar One In	Should be 'high' when the bus is in a positive state. Must be tied 'low' when the unipolar input is used
8	✓			✓	Unipolar Data In	Input for unipolar data to the transition finder. Must be tied 'low' when not used
9		✓		✓	Decoder Shift Clock	Provides the DECODER CLOCK divided by 12, synchronized by the recovered serial data
10		✓		✓	Command/$\overline{\text{Data}}$ Sync	This output indicates the type of synchronizing character received as follows: If a data synchronizing character was received, this pin is low while the data is decoded. If a command synchronizing character was received, this pin is high during data decoding
11	✓			✓	Decoder Reset	A 'high' during a DECODER SHIFT CLOCK rising edge resets the bit counter
12	–	–	✓	✓	V_{SS}	Ground
13	✓		✓	✓	Master Reset	A 'high" clears the counters in both sections
14		✓	✓		÷ 6 Out	Provides the ENCODER CLOCK divided by 6
15		✓	✓		$\overline{\text{Bipolar Zero Out}}$	Provides an active 'low' output to the zero or negative sense of a bipolar line driver
16	✓		✓		$\overline{\text{Output Inhibit}}$	A 'low' inhibits the $\overline{\text{BIPOLAR ZERO OUT}}$ and $\overline{\text{BIPOLAR ONE OUT}}$ by forcing them to inactive, 'high', states
17		✓	✓		$\overline{\text{Bipolar One Out}}$	Provides an active 'low' output to the one or positive sense of a bipolar line driver
18	✓		✓		Serial Data In	Receives serial data at the rate of the ENCODER SHIFT CLOCK
19	✓		✓		Encoder Enable	A 'high' starts the encode cycle provided that the previous cycle is complete
20	✓		✓		Sync Select	A 'high' selects the command sync and a 'low' selects the data sync
21		✓	✓		Send Data	Provides an active 'high' to enable the external serial data source
22	✓		✓		Send Clock In	Clock input at 2 times the data rate
23	✓		✓		Encoder Clock	Input to the divide by 6 circuit
24	–	–	✓	✓	V_{DD}	Positive Supply

Figure 4: Pin Designations (24-Pin Dip/Flat Pack)

PERFORMANCE CHARACTERISTICS AND RATINGS

Absolute Maximum Ratings

Parameter	Min	Max	Units
V_{DD}	3	7	V
Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3V	V
Operating Temperature	-55	+125	°C
Storage Temperature	-65	+150	°C

Figure 5: Absolute Maximum Ratings

DC Characteristics *

Sym	Parameter	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	70%V_{DD}	-	-	V	
V_{IL}	Logic "0" Input Voltage	-	-	30%V_{DD}	V	
V_{IHC}	Logic "1" Input Voltage (Clock)	V_{DD} - 0.5V	-	-	V	
V_{ILC}	Logic "0" Input Voltage (Clock)	-	-	V_{SS} + 0.5V	V	
I_{IL}	Input Leakage Current	-1.0		+1.0	µA	$0V \leq V_{IN} \leq V_{DD}$
V_{OH}	Logic "1" Output Voltage	2.4	-	-	V	I_{OH} = -3 mA
V_{OL}	Logic "0" Output Voltage	-	-	0.4	V	I_{OL} = 1.8 mA
I_{DDSB}	Standby Supply Current	-	0.5	2.0	mA	Output Open $V_{IN} = V_{DD} = 5.5V$
I_{DDOP}	Operating Supply Current	-	8.0	10.0	mA	V_{DD} = 5.5V, f = 1MHz
C_{IN}	Input Capacitance	-	5.0	7.0	pF	
C_{OUT}	Output Capacitance	-	8.0	10.0	pF	

* V_{DD} = 5V ±10%, over full operating temperature range.

Figure 6: DC Characteristics

AC Characteristics

Sym	Parameter	Limits		
		Min	Max	Units
fEC	Encoder clock frequency	0	15	MHz
fESC	Send clock frequency	0	2.5	MHz
tECR	Encoder clock rise time	-	8	ns
tECF	Encoder clock fall time	-	8	ns
fED	Data rate	0	1.25	MHz
tMR	Master reset pulse width	150	-	ns
tE1	Shift clock delay	-	125	ns
tE2	Serial data setup time	75	-	ns
tE3	Serial data hold time	75	-	ns
tE4	Enable setup time	90	-	ns
tE5	Enable pulse width	100	-	ns
tE6	Sync setup time	55	-	ns
tE7	Sync pulse width	150	-	ns
tE8	Send data delay	0	50	ns
tE9	Bipolar output delay	-	130	ns

Notes:
1. V_{DD} = 5V ±10%, over full operating temperature range.
2. C_L=50pF.

Figure 7: Encoder Electrical Characteristics

Sym	Parameter	Limits			
		Min	Typ	Max	Units
fDC	Decoder clock frequency	0	-	15	MHz
tDCR	Decoder clock rise time	-	-	8	MHz
tDCF	Decoder clock fall time	-	-	8	ns
fDD	Data rate	0	-	1.25	MHz
tDR	Decoder reset pulse width	150	-	-	ns
tDRS	Decoder reset setup time	75	-	-	ns
tMR	Master reset pulse width	150	-	-	ns
tD1	Bipolar data pulse width	t_{DC} + 10	-	-	ns
tD2	Sync transition span	-	18t_{DC}	-	ns
tD3	One-Zero overlap	-	-	t_{DC} - 10	ns
tD4	Short data transition span	-	6t_{DC}	-	ns
tD5	Long data transition span	-	12t_{DC}	-	ns
tD6	Sync delay (on)	-20	-	110	ns
tD7	Take data delay (on)	0	-	110	ns
tD8	Serial data out delay	-	-	80	ns
tD9	Sync delay (off)	0	-	110	ns
tD10	Take data delay (off)	0	-	110	ns
tD11	Valid word delay	0	-	110	ns

Notes:
1. V_{DD} = 5V ±10%, over full operating temperature range.
2. C_L=50pF.
3. t_{DC} = Decoder clock period = 1/f_{DC}

Figure 8: Decoder Electrical Characteristics

ENCODER OPERATION

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilised to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a failing edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word ✍. When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③. During these sixteen periods the data should be clocked into the SERIAL DATA input with every low-high transition of the ENCODER SHIFT CLOCK ③ - ④. After the sync and the Manchester II coded data are chip transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word ⑤. At any time a low in $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way. To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

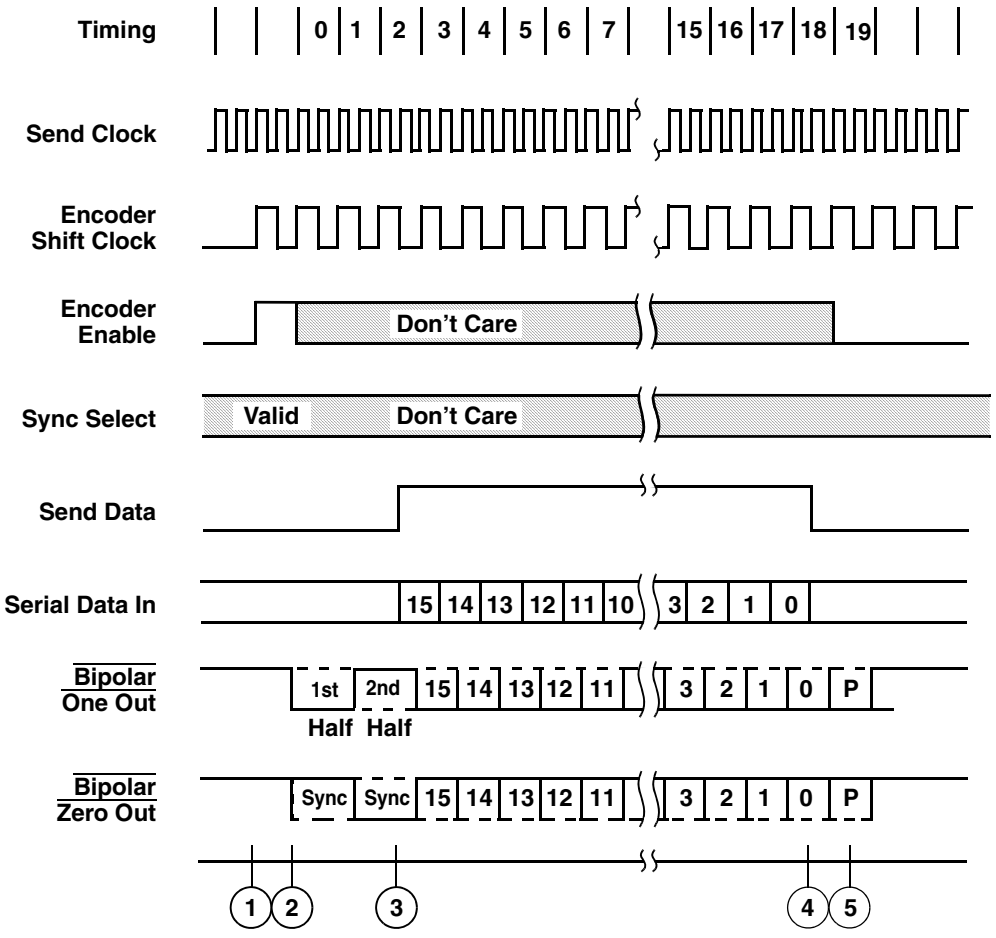


Figure 9: Encoder Operation

DECODER OPERATION

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in MIL-STD-1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ of an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ①, the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. if the sync character was a command sync, this output will go high ✍ and remain high for sixteen DECODER SHIFT CLOCK periods ③, otherwise it will remain low. The TAKE DATA output will go high and remain high ✍ - ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in a NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ✍ - ③.

After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

At any time in the above sequence, a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

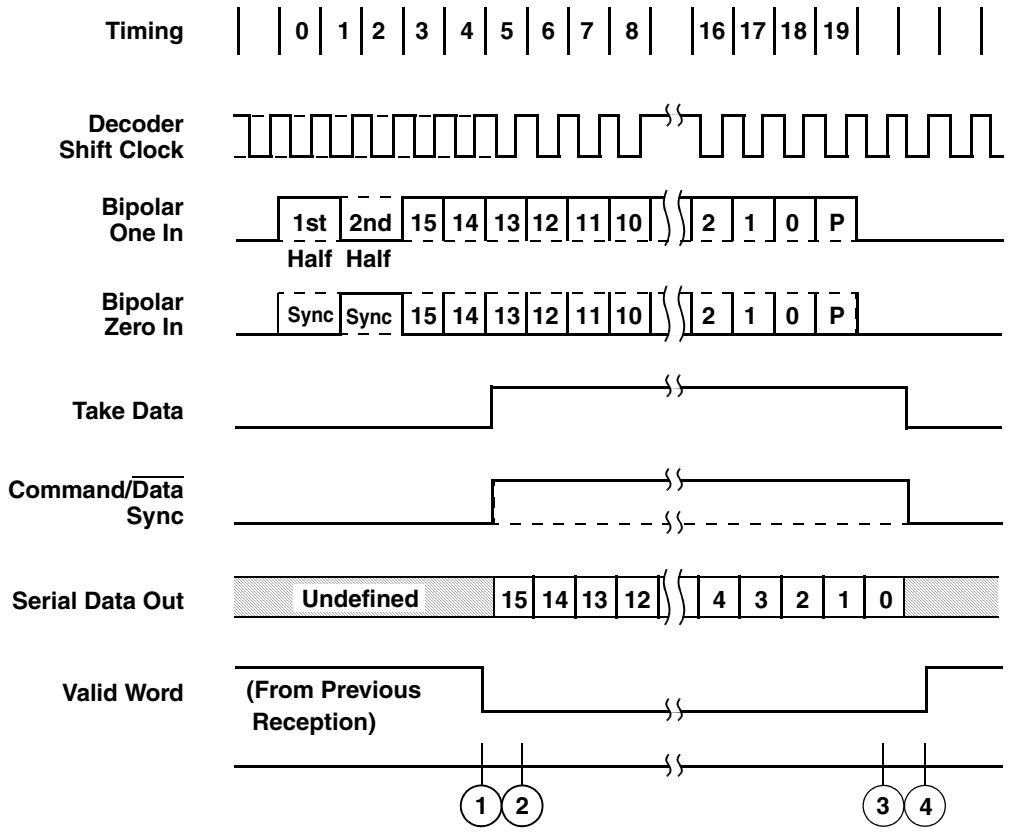


Figure 10: Decoder Operation

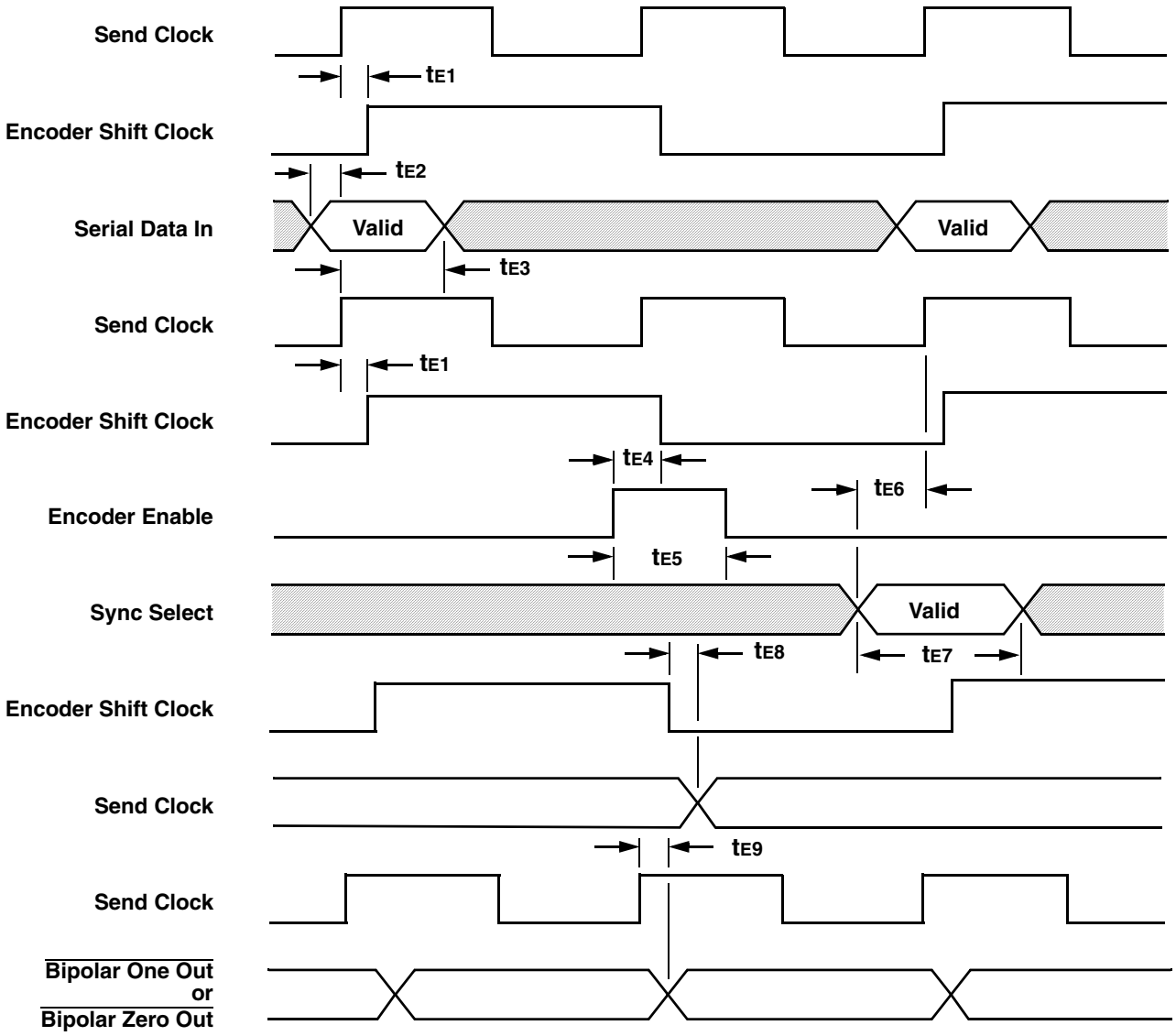
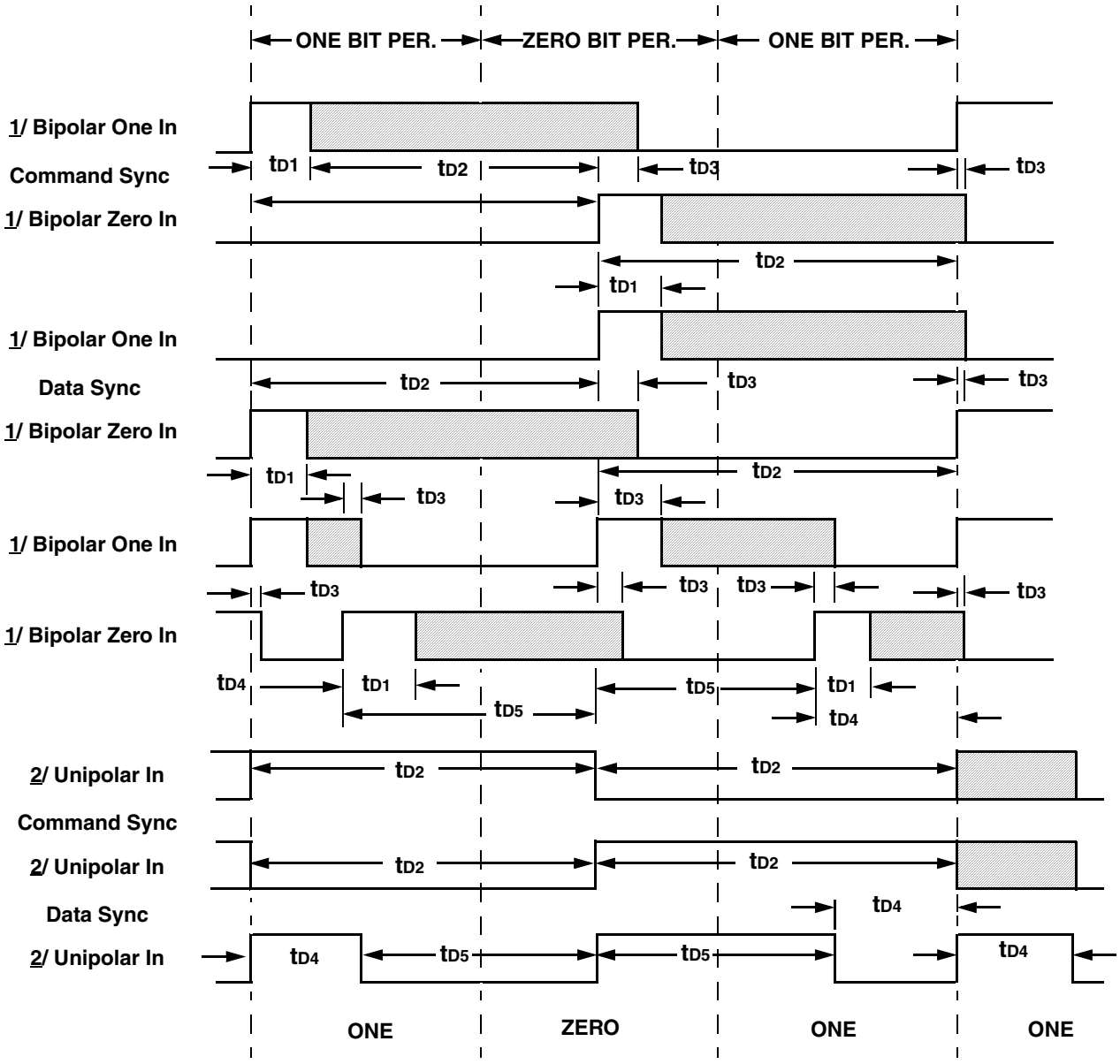


Figure 11: Encoder Timing Diagram



Notes: 1. Unipolar In = 0
2. Bipolar One In = 0
Bipolar Zero In = 1

Figure 12: Decoder Timing Diagram

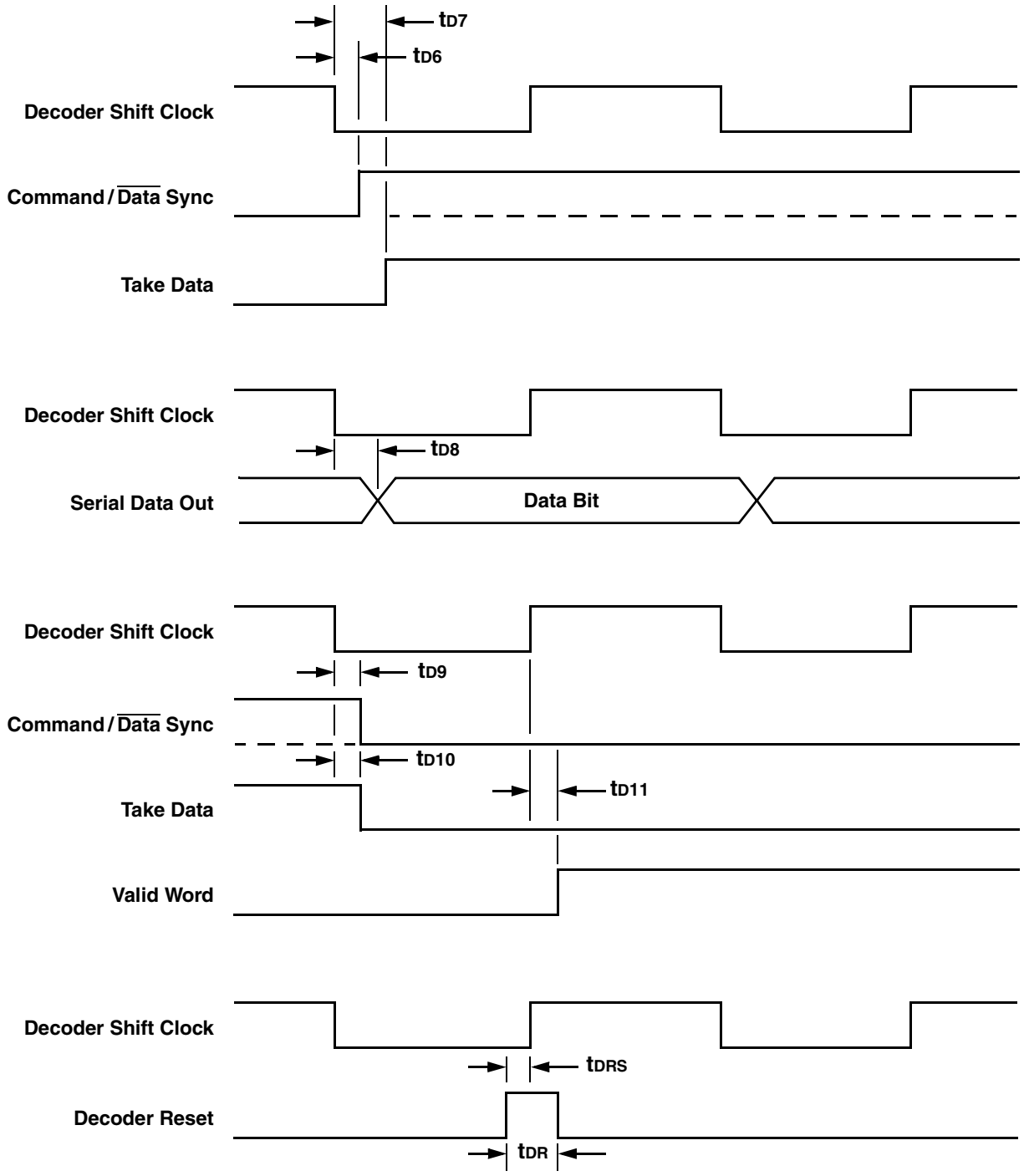


Figure 13: Decoder Timing Details

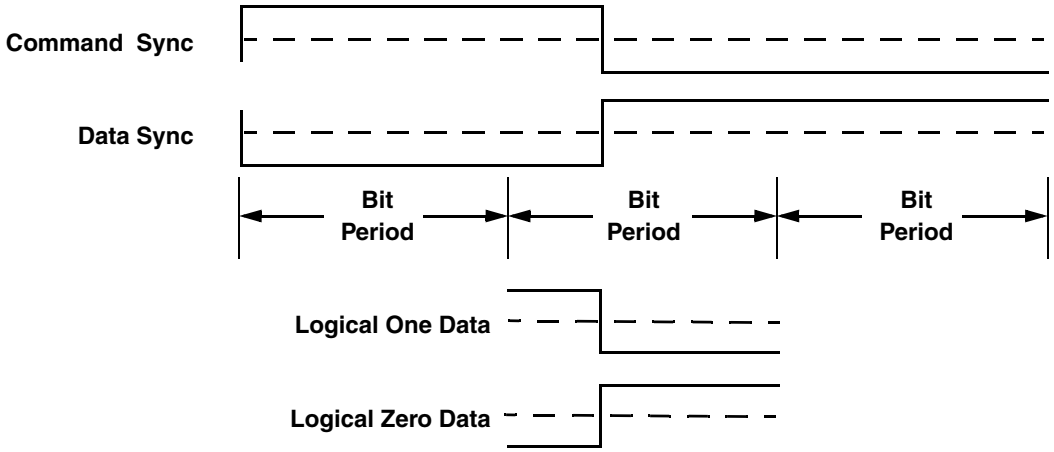


Figure 14: Character Formats

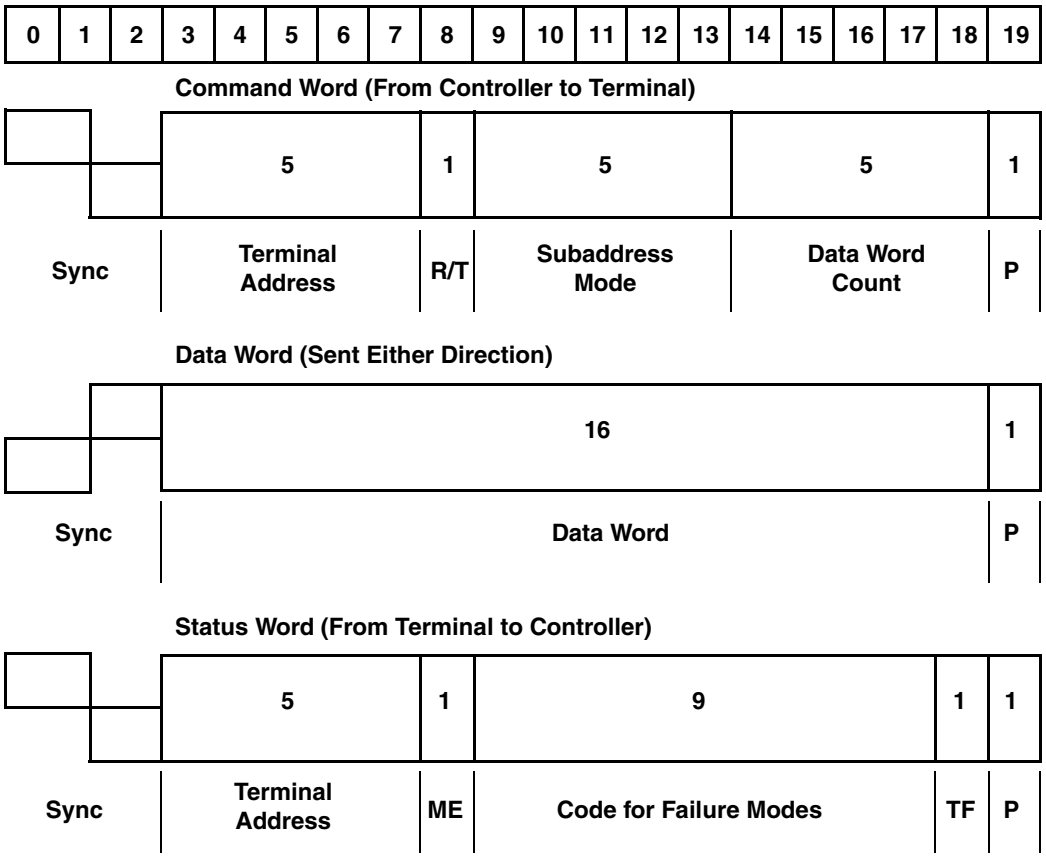
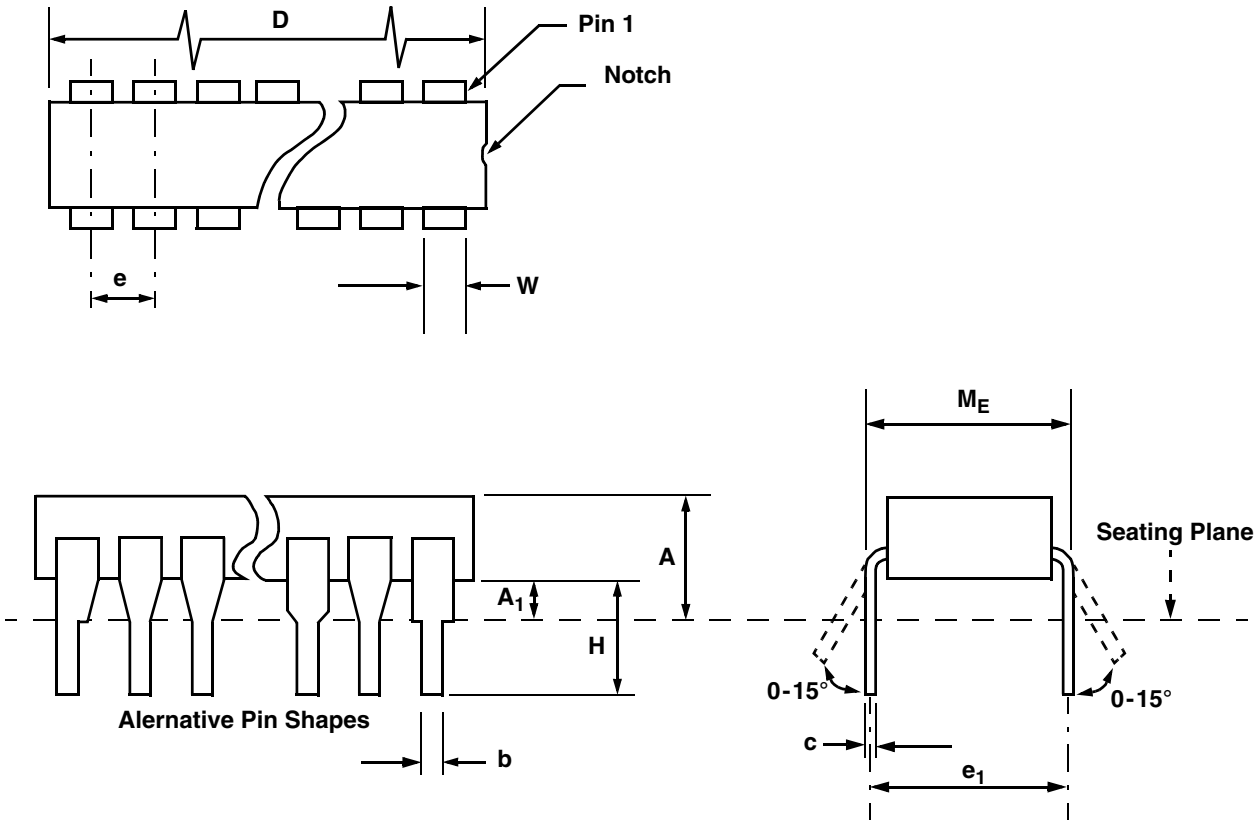
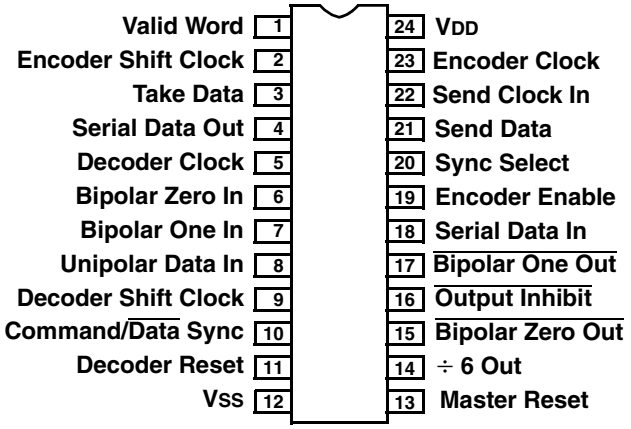


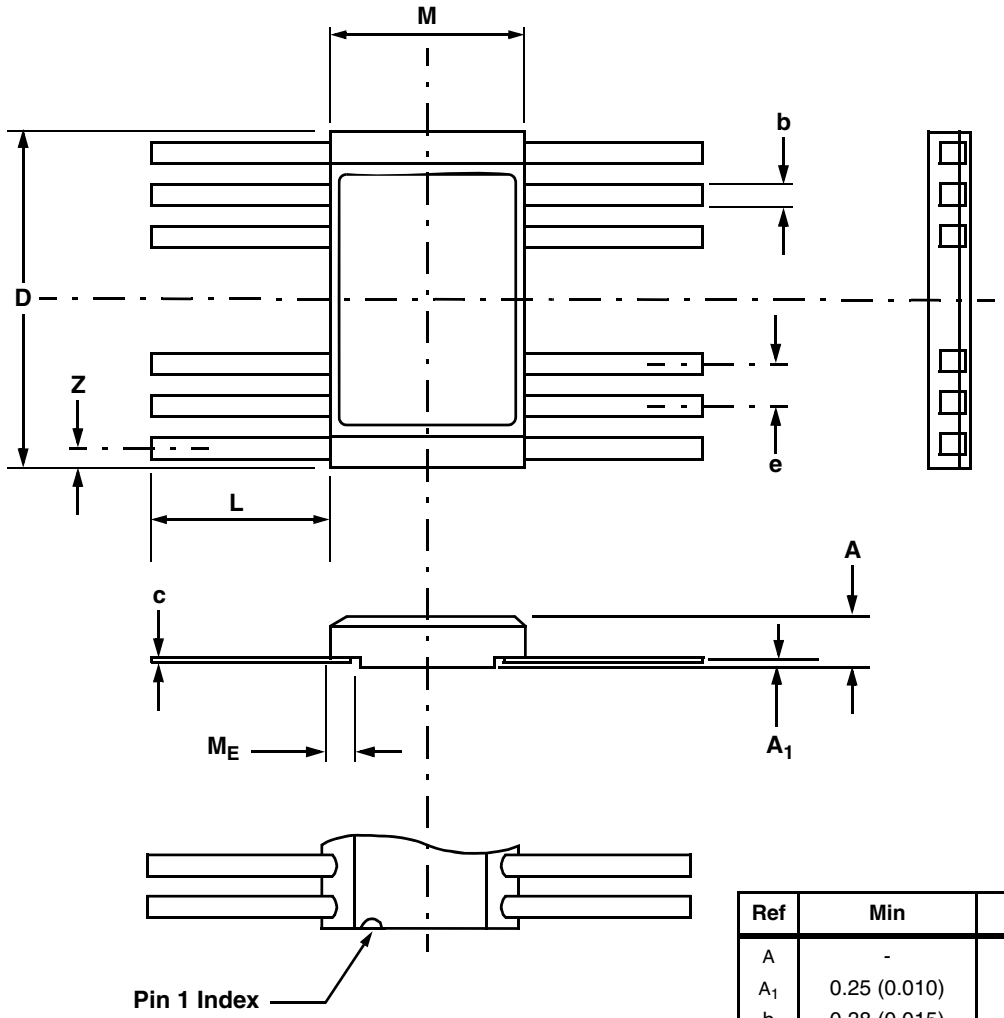
Figure 15: Word Formats





Ref	Min	Nom	Max
A	-	-	5.60 (0.220)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	30.79 (1.212)
e	-	2.54 (0.100) Typ	-
e_1	-	15.24 (0.600) Typ	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

Figure 16: 24-Lead Ceramic DIL (Solder Seal) - Package Style C



Ref	Min	Nom	Max
A	-	-	2.67 (0.105)
A_1	0.25 (0.010)	-	1.02 (0.040)
b	0.38 (0.015)	-	0.48 (0.019)
c	0.10 (0.004)	-	0.18 (0.007)
D	14.86 (0.585)	-	15.62 (0615)
e	-	1.275 (0.050)	-
L	6.73 (0.265)	-	7.75 (0.305)
M	9.91 (0.390)	-	10.41 (0.410)
M_E	7.6 (0.30)	-	-
Z	0.13 (0.005)	-	1.14 (0.045)

Dimensions in mm (inches)

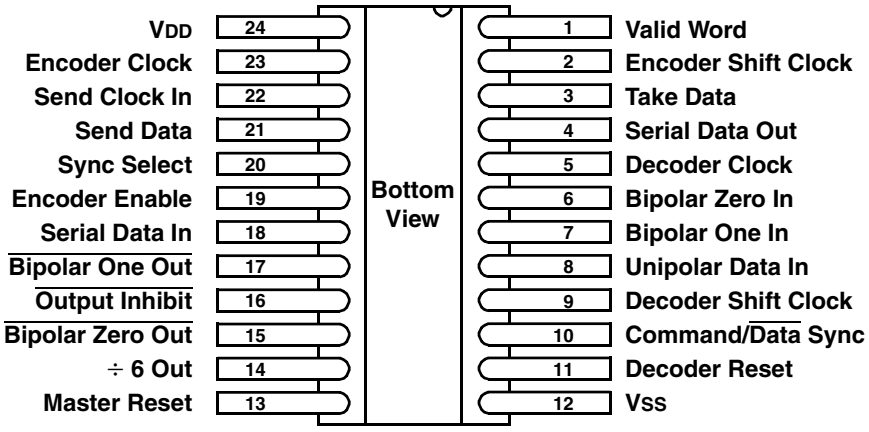
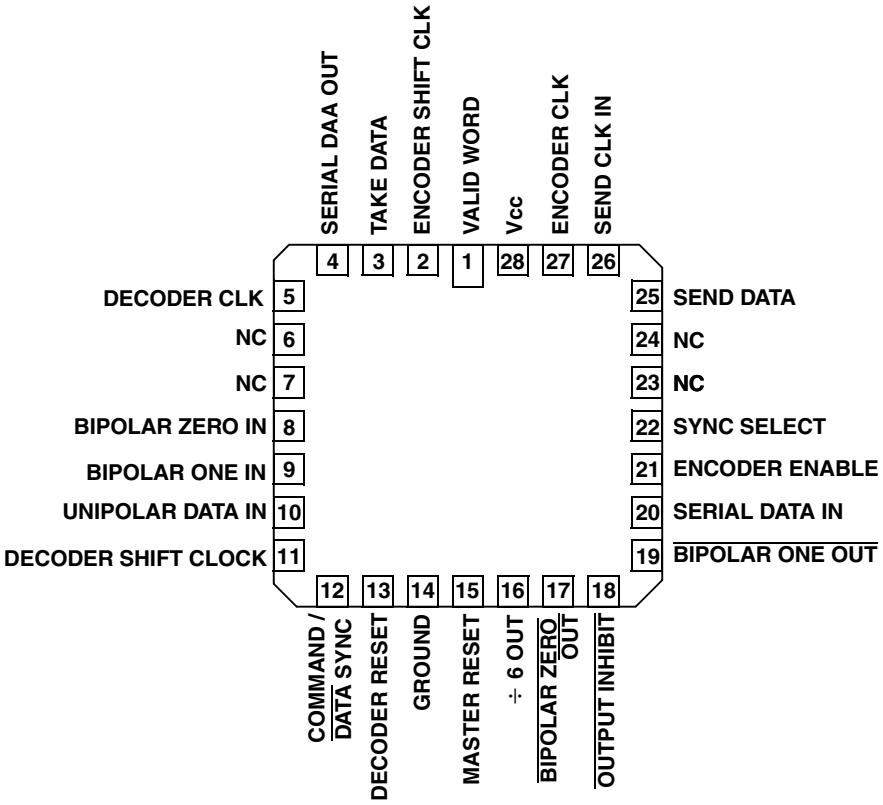


Figure 17: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style F

TOP VIEW



BOTTOM VIEW

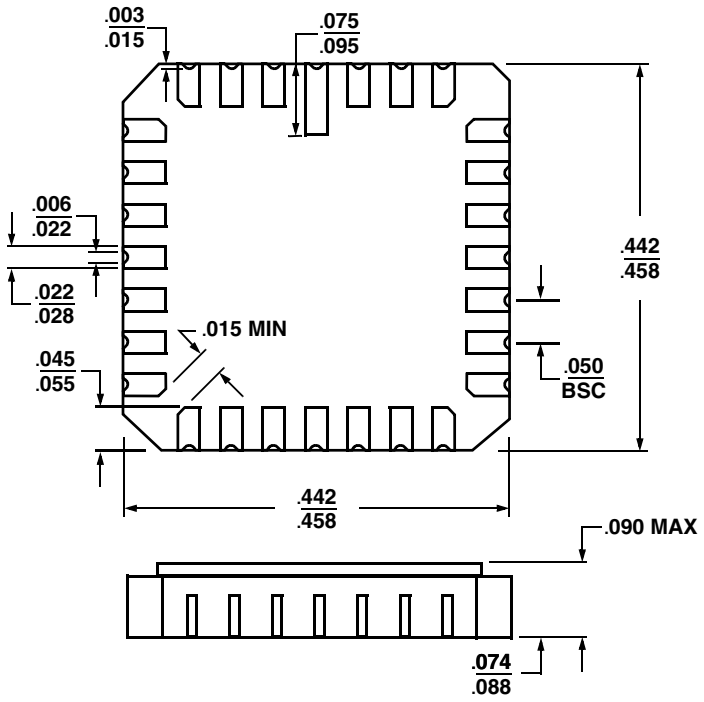


Figure 18: 28-Leadless Ceramic Chip Carrier - Package Style L

ORDERING INFORMATION

Model Number	Part Number
ACT15530XX	See Below or Contact Factory

AEROFLEX PART NUMBER BREAKDOWN

ACT15530 X X

Package Type

C = Ceramic DIL (Figure 16)
F = Flatpack (Figure 17)
L = LCC (Figure 18)
N = Naked Die *
P = Plastic DIP *

Rel Level

B = Commercial Screening, Operating Temperature -55°C to +125°C
C = Commercial Screening, Operating Temperature 0°C to +70°C
I = Commercial Screening, Operating Temperature -40°C to +85°C
M = Full Military Screening, Operating Temperature -55°C to +125°C
Space *

*** Contact Factory for Details**

PLAINVIEW, NEW YORK
Toll Free: 800-THE-1553
Fax: 516-694-6715

INTERNATIONAL
Tel: 805-778-9229
Fax: 805-778-1980

NORTHEAST
Tel: 603-888-3975
Fax: 603-888-4585

SE AND MID-ATLANTIC
Tel: 321-951-4164
Fax: 321-951-4254

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