TOSHIBA

TMP3912U 32-Bit MIPS RISC Processor

Description

The TMP3912U is a single-chip, highly integrated Application Specific System Product (ASSP) developed specifically for Personal Digital Assistant (PDA) applications.

The TMP3912U integrates a high performance, low power MIPS RISC processor core with the necessary support logic and peripherals functions needed to develop a complete PDA solution. This highly integrated solution supports the Microsoft® Windows™ CE v2.0 operating system that includes color display capability.

Branch-likely and multiply-add instructions have been added along with hardware interlock and cache locking ability to allow critical path code optimization and reduce overall code requirements.

Features

- TX39 Core based on R3000A architecture
- 74MHz performance
- Single cycle multiply/accumulate (MAC) for integrated DSP functions such as V.34 compatible 28.8Kbps soft modem
- Five-stage pipeline
- Instruction cache: 4KB
- Data cache: 1KB, 2-way associative
- Integrated Translation Lookaside Buffer (TLB)
- Low Power
  - 3.3V operation
  - 300mW operating current (typical)
  - 10µA Standby current (typical)
  - CPU clock stop mode
  - Power down modes for individual internal peripheral modules
- Package: 208-pin low profile QFP

On-Chip Peripherals

- Clock generator with built in 8x frequency phase-locked loop (PLL)
- Four stage write buffer
- Multiple DMA channels
- Memory controllers for
  - DRAM, HDRAM, SDRAM,
  - SRAM, ROM, FLASH, PCMCIA
- Integrated power management unit

Development Tool Support

The TX39 family supports a wide range of development tools available from both Toshiba and third party partners.

Language Tools

- Compilers
  - Toshiba
  - Green Hills Software
  - Cygnus
- Emulators
  - HP
  - KMC (Rom Emulator)

Operating Systems

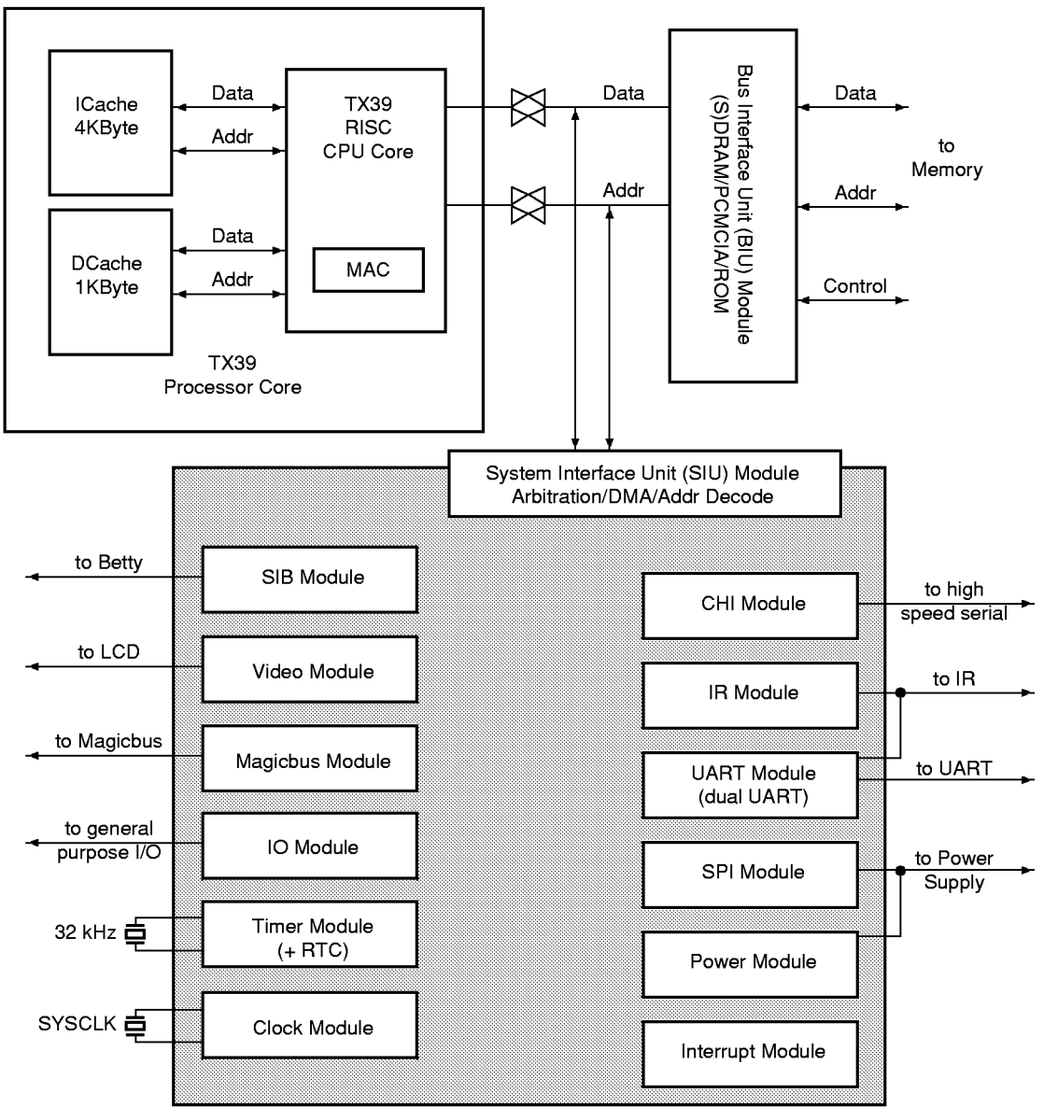
- µITRON
- ISI (pSOS)
- Wind River Systems (VxWorks)
- Microsoft Windows CE

Evaluation Boards

- Cogent Computer Systems, Inc.
- Densan
- Toshiba
- Midas

Reference Platform

- A complete development system for Windows CE v2.0 applications is available from Toshiba



TMP3912U Block Diagram

Electric Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	V_{SS}–0.5 to 4.5	V
Input voltage	V_{IN}	VSS–0.5 to V_{PP}+0.5	V
Storage temperature	T_{STG}	–55 to 125	°C
Maximum Dissipation (T_A = 70°C)	P_D	1	W

NOTE Use at specifications higher than the maximum ratings can cause permanent damage. For normal operation, use under the recommended operating conditions. Exceeding the recommended operationg conditions may affect reliability.

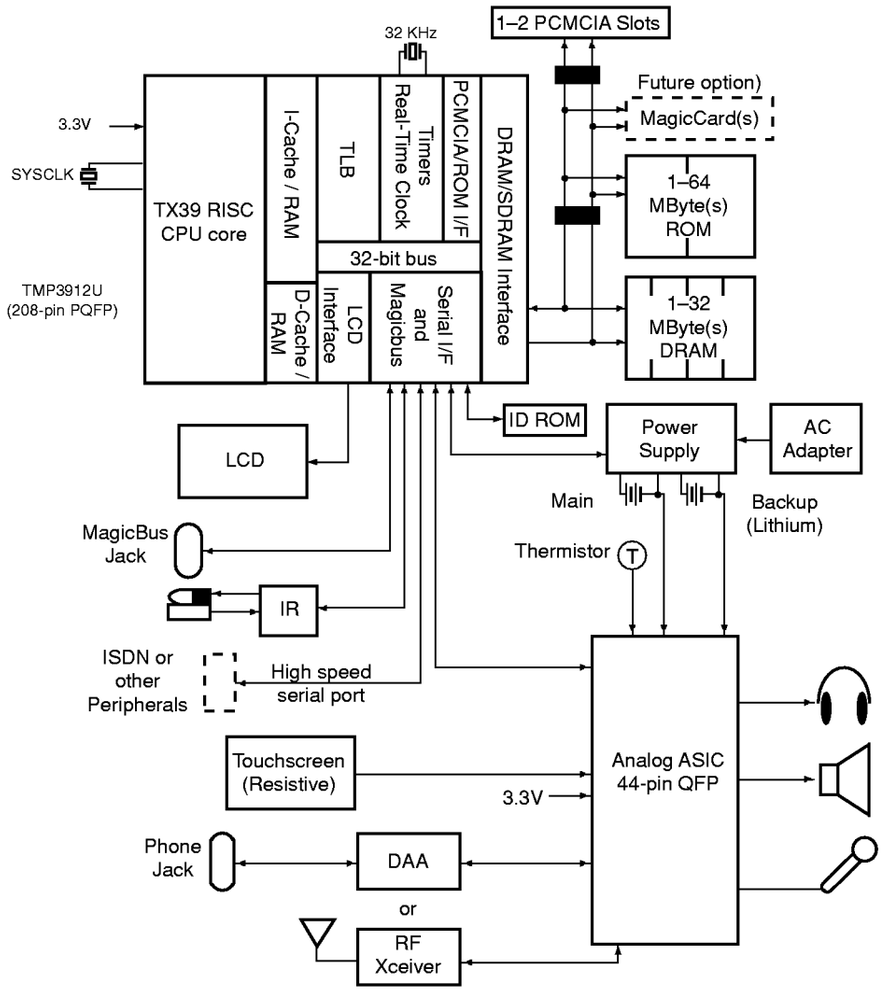
Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply voltage	V_{DD}		3.0	3.3	3.6	V
Operating temperature	T_{OPR}		0	—	70	°C

DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating current	I_{DD}	V_{IN} = V_{DD} or V_{SS} V_{DD} = Max. I_{OH} = I_{OL} = 0 mA fIn(7) = 10 MHz	—	110	TBD	mA
Static current	I_{DD3}	V_{IN} = V_{DD} or V_{SS} V_{DD} = Max. I_{OH} = I_{OL} = 0 mA SLEEP mode & RTC stop mode	—	10	100	µA
Input Leakage current	I_{IN}	V_{IN} = V_{DD} or V_{SS}	–10	—	10	µA
Input voltage (1)	V_{IH1}	V_{DD} = 3.6V	V_{DD}x0.8	—	V_{DD}+0.3	V
	V_{IL1}	V_{DD} = 3.0V	–0.3	—	V_{DD}x0.2	V
Input voltage (2)	V_{IH2}	V_{DD} = 3.6V	2.4	—	V_{DD}+0.3	V
	V_{IL2}	V_{DD} = 3.0V	–0.3	—	0.6	V
Input voltage (3)	V_{OH1}	V_{DD} = 3.0V, I_{OH} = –4mA	V_{DD}–0.6	—	—	V
	V_{OL1}	V_{DD} = 3.0V, I_{OL} = –4mA	—	—	V_{DD}+0.4	V
Input voltage (4)	V_{OH2}	V_{DD} = 3.0V, I_{OH} = –8mA	V_{DD}–0.6	—	—	V
	V_{OL2}	V_{DD} = 3.0V, I_{OL} = –8mA	—	—	V_{DD}+0.4	V
Input voltage (5)	V_{OH3}	V_{DD} = 3.0V, I_{OH} = –16mA	V_{DD}–0.6	—	—	V
	V_{OL3}	V_{DD} = 3.0V, I_{OL} = –16mA	—	—	V_{DD}+0.4	V
Input voltage (6)	V_{OH4}	V_{DD} = 3.0V, I_{OH} = –24mA	V_{DD}–0.6	—	—	V
	V_{OL4}	V_{DD} = 3.0V, I_{OL} = –24mA	—	—	V_{DD}+0.4	V
Input current (Pull-down resistor)	I_{IHP}	V_{DD} = MAX, V_{IN} = V_{DD}	20	—	120	µA

(1) SYSCLKIN
(2) OTHER INPUT
(3) D[31:0], RASO*, RAS1*, DCSO*, DCKE*, DQMH, DQML, DREQ*, DGRNT*, BC32K, VDAT[3:0], CP, LOAD, DF, FRAME, DISPON, VIDDONE, PWRCS, TXD RXD, CS3–0*, CHIFS, CHICLK, CHIDOUT, CHIDIN, IO[6:0], SPICLK, SPIOUT, SPIIN, SIBSYNC, SIBDOUT, SIBMCLK, SIBCLK, RXPWR, IROUT, CARD1WAIT*, CARD2WAIT*, MIOX[2:0],
(4) A[12:0], ALE, RD*, WE*, CAS3–0*, CARDREG*, CARDIOWR*, CARDICSL*, CARD1CSH*, CARD2CSL*, CARD2CSH*
(5) DCLKOUT
(6) MBUSCLK, MBUSDATA



Windows CE v2.0 HIPC Application Example

www.toshiba.com/ taec

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