## Description

The µPD72061 is a hard-disk controller featuring low power consumption and high-speed data transfers. Based on the µPD7261A/B, it provides control signals for interfacing SMD/SMD-E and ST506/412 type drives. The sophisticated instruction set minimizes the software overhead for the host microprocessor and gives the user flexibility in selecting operating parameters.

The DMA interface signals of the µPD72061 facilitate multisector and multitrack data transfers. Extensive error reporting, verify commands, and CRC/ECC data error checking assure reliable controller operation.

An 8-byte FIFO is used for loading command parameters and obtaining command results. This makes structuring of drivers a simple task. The FIFO also buffers data during DMA read/write operations.
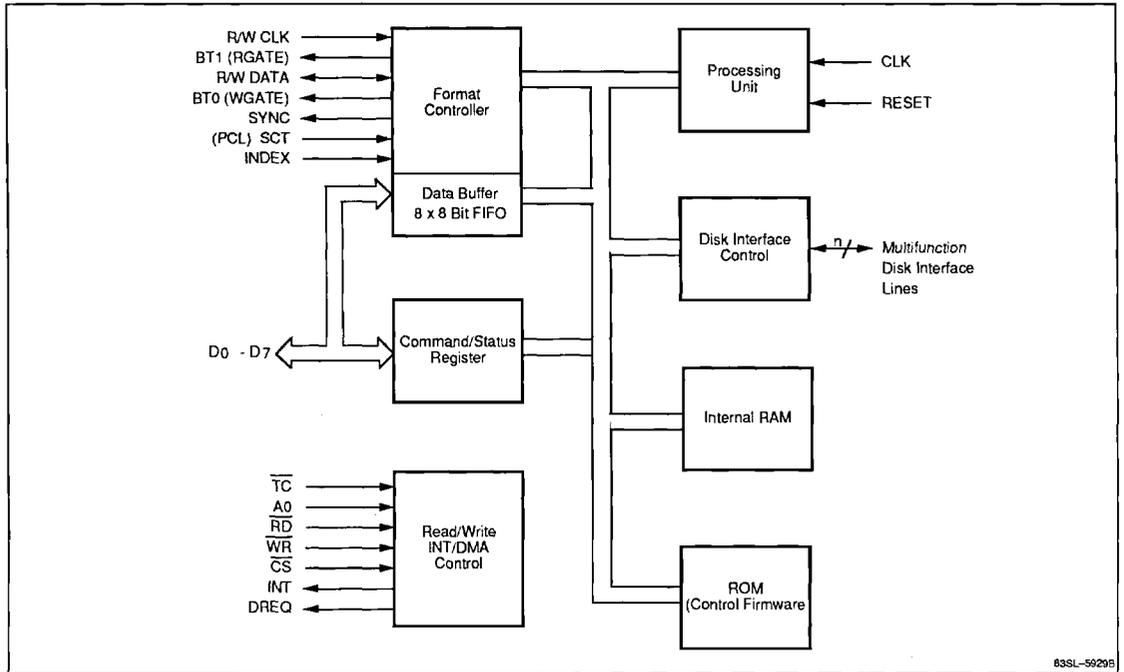
## Features

- Flexible interface supports SMD/SMD-E and ST506/412 type drives
- Programmable track format
- Controls up to eight drives in SMD-type mode, four drives in ST506-type mode
- Parallel seek operation
- Multisector and multitrack transfer
- Data scan and data verify
- High-level commands, including:
  - Read Data, Write Data, Scan Data, Verify Data
  - Read ID, Verify ID
  - Check, Seek (normal or buffered), Specify
  - Read Diagnostic (SMD only), Detect Error
  - Format
- NRZ or MFM format
- Read/write clock frequency: 24 MHz max
- Error detection and correction
- CMOS
- µPD7261A/B compatible
- Single +5-volt power supply
- 40-pin plastic DIP, 52-pin plastic miniflat, 52-pin PLCC

## Ordering Information

| Part Number | Package |
|---|---|
| µPD72061C | 40-pin plastic DIP |
| µPD72061GC-3B6 | 52-pin plastic miniflat |
| µPD72061L | 52-pin PLCC |

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## μPD72061 Block Diagram



R/W CLK
BT1 (RGATE)
R/W DATA
BT0 (WGATE)
SYNC
(PCL) SCT
INDEX

Format Controller

Data Buffer 8 x 8 Bit FIFO

D0 - D7

Command/Status Register

Processing Unit

CLK

RESET

Disk Interface Control

n/ Multifunction Disk Interface Lines

Internal RAM

TC
A0
RD
WR
CS
INT
DREQ

Read/Write INT/DMA Control

ROM (Control Firmware)

83SL-5929B