2080MX
20 Gbps 4:1 Multiplexer
Data Sheet

Applications

- Broadband test and measurement
- SONET OC-192 equipment
- Telecom transmission systems

Features

- Supports data rates from DC to 20 Gbps
- Low power consumption: 1.4 W typical
- CML parallel inputs 300 - 2000 mVpp diff
- CML serial output 1200 mVpp diff typical
- Fast rise and fall times: 17 ps typical
- Single power supply +3.3 V
- Available in a QFN plastic package
- Evaluation board available

Description

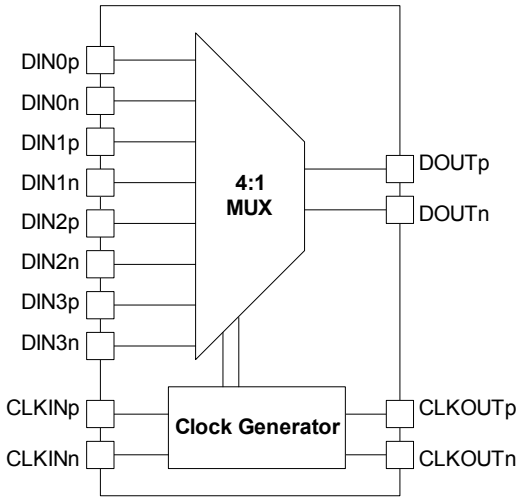
The 2080MX is a very broadband 4:1 multiplexer (mux) operating at rates up to 20 Gbps for use in SONET OC-192 applications, broadband test and measurement equipment, and telecom transmission systems. The MUX accepts four differential data channels at data rates up to 5 Gbps and combines them into a serial data stream suitable for transmission over high-speed networks.

The 2080MX requires an input clock whose frequency is equal to the serial output data bit rate. The input clock is divided on-chip to generate the clocks needed for multiplexing the data and for clocking the low-speed data inputs of the mux.

All data and clock I/O use +3.3 V current mode logic (CML) buffers and include on-chip terminations to +3.3V. Inputs and outputs may be AC-coupled.

The 2080MX operates from a single +3.3 V power supply and is available in a QFN plastic package.

Block Diagram



Absolute Maximum Ratings

- Stresses beyond those listed here may cause permanent damage to the device.
- These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the "Operating Conditions" and "Electrical Specifications" of this datasheet is not implied.
- Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	V_{CC}		-0.5	3.6	V
Junction Temperature – Die	T_J		---	+175	°C
Case Temperature – Packaged	T_C		---	+125	°C
Storage Temperature	T_{STORE}		---	+125	°C
Humidity	RH		0	100	%
ESD protection (HBM)	V_{ESD}		TBD	---	V

Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{CC}	± 5% Tolerance	+3.135	+3.300	+3.465	V
Power Supply Current	I_{CC}		---	415	485	mA
Power Dissipation	P_D		---	1.4	1.7	W
Operating Temperature (Junction) - Die	T_J		+15	---	+125	°C
Operating Temperature (Case) - Packaged	T_C		-5	---	+85	°C

Notes:

[1] For BER < 10^{-12}. Assumes presence of 0.1 µF decoupling capacitors on all power supply pins.

Electrical Specifications

WARNING – To prevent damage to the part:

- DC power must be turned off prior to connecting or disconnecting any cables.
- All input and output pins include on-chip 50 Ω back terminations to V_{CC}. Pins must be AC coupled for ground reference.

Electrical specifications guaranteed when the part is operated within the specified operating conditions.

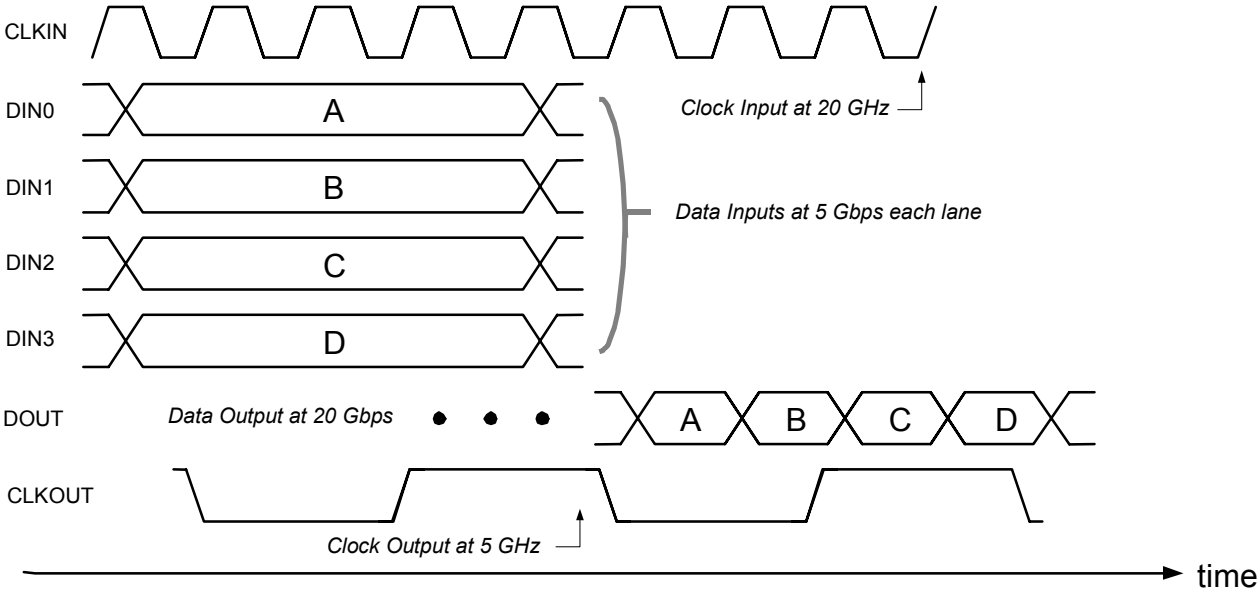
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
High Speed Clock Inputs (CLKINp, CLKINn)						
Input Clock Frequency	f_{CLKIN}		---	---	20	GHz
Input Slew Rate	SR		1	---	---	V/ns
Input Voltage Amplitude	V_{CLKIN}	Single-ended peak-to-peak	300	---	1000	mVpp
Input High Level	V_{IH}		V_{CC}-0.5	---	V_{CC}+0.5	V
Input Low Level	V_{IL}		V_{CC}-1.0	---	V_{CC}	V
Worst Case Input Return Loss[1]	RL_{IN}	25 kHz < f < 12.5 GHz	---	10	---	dB
Input Clock Duty Cycle	ICDC		45	50	55	%
Data Inputs (DIN[0-3]p, DIN[0-3]n)						
Input Voltage Amplitude	V_{DIN} (diff)	Differential peak-to-peak	300	---	2000	mVpp
	V_{DIN} (SE)	Single-ended peak-to-peak	300	---	1000	mVpp
Input High Level	V_{IH}		V_{CC}-0.5	---	V_{CC}+0.5	V
Input Low Level	V_{IL}		V_{CC}-1.0	---	V_{CC}	V
Input Return Loss[1]	RL_{IN}	25 kHz < f < 5 GHz	---	10	---	dB
High Speed Data Outputs (DOUTp, DOUTn)						
Maximum Data Rate[3]	f_{Max}	10^{-12} BER	20	---	---	Gbps
Output Voltage Amplitude	V_{DOUT}	Differential peak-to-peak	1000	1200	1300	mVpp
Output High Voltage[1]	V_{OH}	DC coupled, V_{CC} referenced	V_{CC}-50	V_{CC}-5	V_{CC}	mV
Output Common Mode	V_{OCM}	DC coupled, V_{CC} referenced	---	V_{CC}-300	---	mV
Rise/Fall Time	t_r/t_f	Measured from 20% - 80%	---	12	17	ps
Pulse Width	PW%	Relative to bit period	95	100	105	%
Worst Case Output Return Loss[1]	RL_{OUT}	25 kHz < f < 12.5 GHz	---	10	---	dB
Deterministic Jitter (peak-to-peak)	J_D	Measured with 2^7–1 PRBS	---	2.5	6	ps
Random Jitter (RMS)	J_R	Measured with 1010 pattern	---	0.5	1	ps
Clock Outputs (CLKOUTp, CLKOUTn)						
Output Voltage Amplitude	V_{CLKOUT}	Differential peak-to-peak	1000	1200	1400	mVpp
Output High Voltage[1]	V_{OH}	DC coupled, V_{CC} referenced	V_{CC}-50	V_{CC}-5	V_{CC}	mV
Output Common Mode	V_{OCM}	DC coupled, V_{CC} referenced	---	V_{CC}-300	---	mV
Rise/Fall Time	t_r/t_f	Measured from 20% - 80%	---	25	30	ps
Output Clock Duty Cycle	OCDC		45	50	55	%
Worst Case Output Return Loss[1]	RL_{OUT}	25 kHz < f < 5 GHz	---	10	---	dB
Random Jitter	J_R	Measured with 0101 pattern	---	0.5	1	ps rms

Notes:

[1] Single-ended measurement made on one pin of the differential pair.

[2] Data is NRZ format.

Timing Information



Typical DC Operating Characteristics

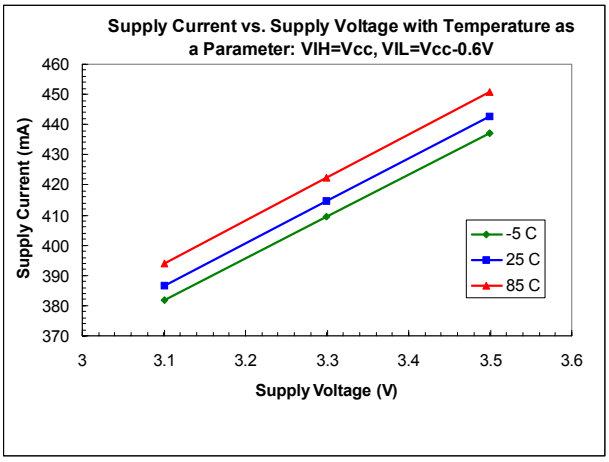


Figure 1. Supply current vs. power supply potential with temperature as parameter.

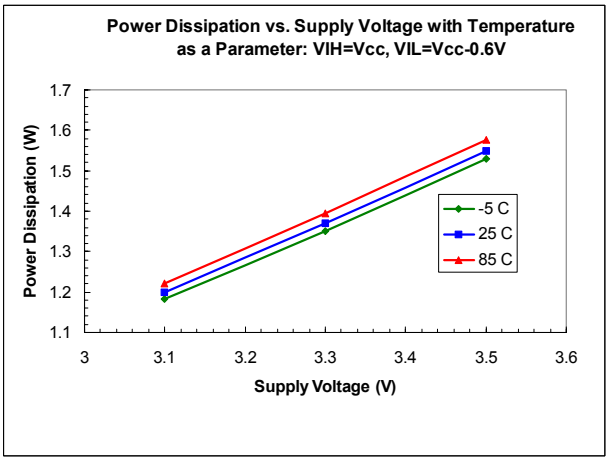


Figure 2. Power dissipation versus power supply with temperature as parameter.

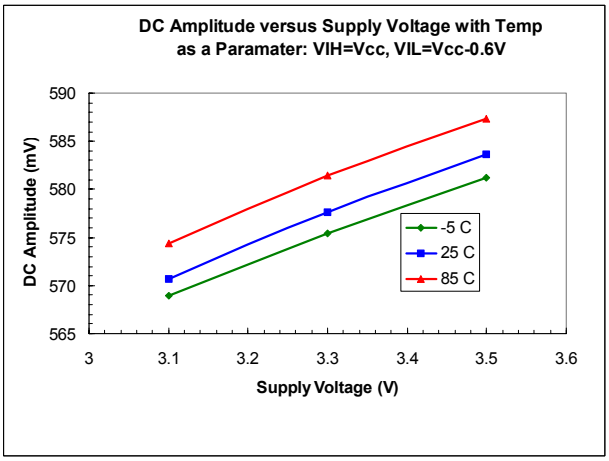


Figure 3. Single-ended data output amplitude measured statically with a DC voltmeter over power supply and temperature.

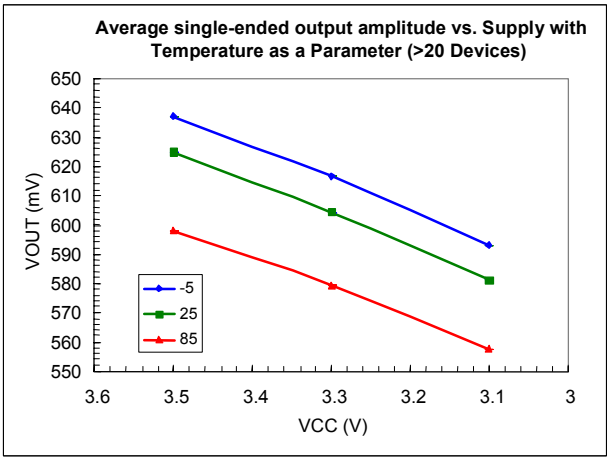


Figure 4. Single-ended clock output amplitude measured statically with a DC voltmeter over power supply and temperature.

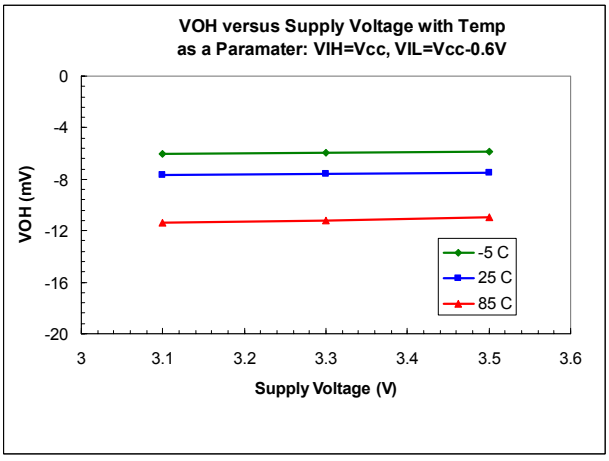


Figure 5. Data output high level (V_{OH}) measured over power supply and temperature.

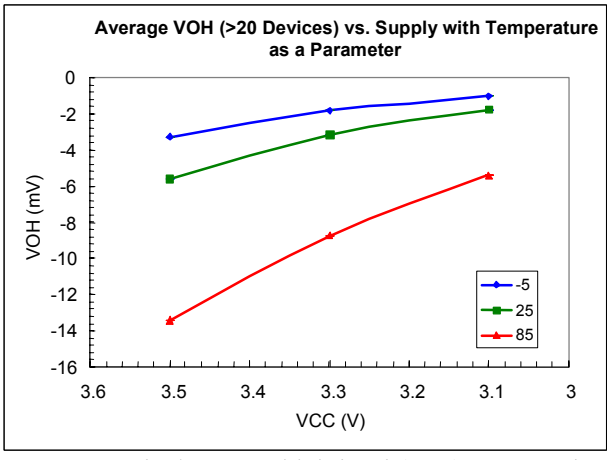


Figure 6. Clock output high level (V_{OH}) measured over power supply and temperature.

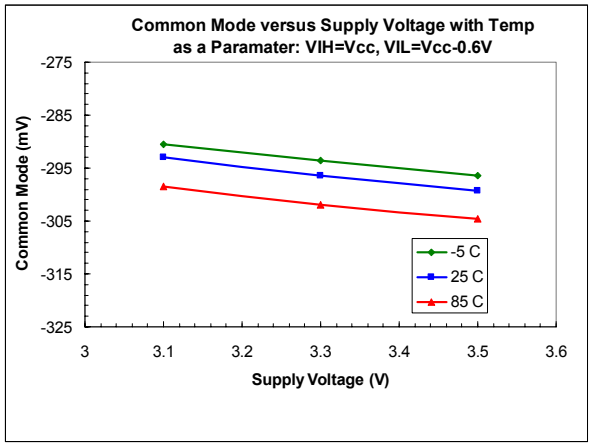


Figure 7. Data output common mode (V_{OCM}) measured over power supply and temperature.

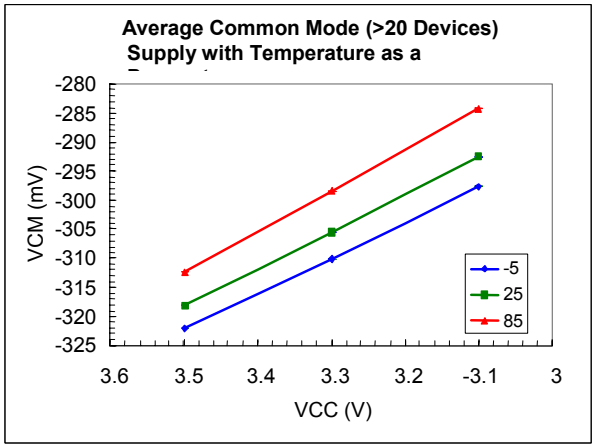


Figure 8. Clock output common mode (V_{OCM}) measured over power supply and temperature.

Typical Time Domain Operating Characteristics

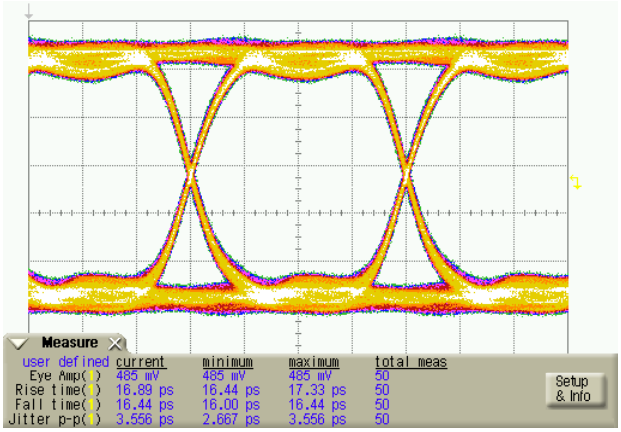


Figure 9. Typical DOUTp eye diagram at 25 Gbps, 27-1 PRBS, 100 mV/div, 10 ps/div. Operation guaranteed to 20 Gbps.

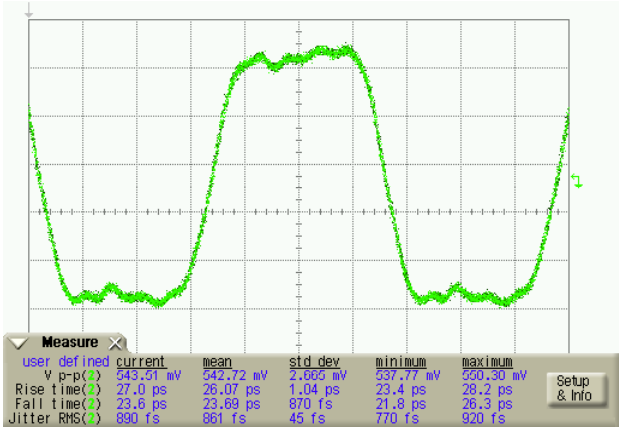


Figure 10. Typical CLKOUTp eye diagram at 25 Gbps, 27-1 PRBS, 100 mV/div, 50 ps/div. Operation guaranteed to 20 Gbps.

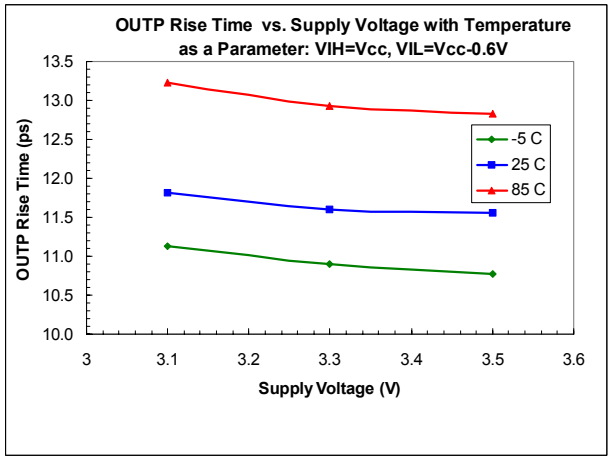


Figure 11. Typical data output rise time measured over power supply and temperature.

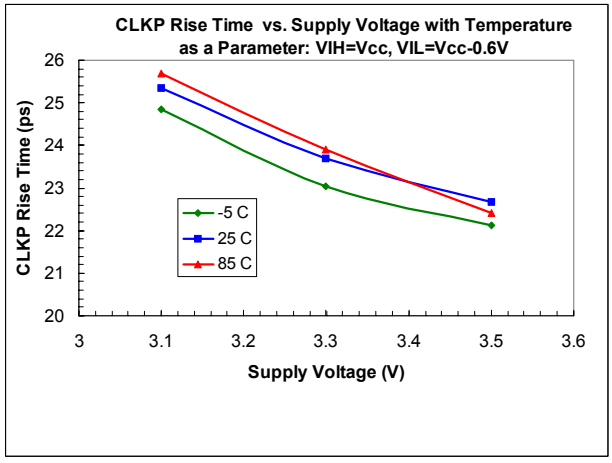


Figure 12. Typical clock output rise time measured over power supply and temperature.

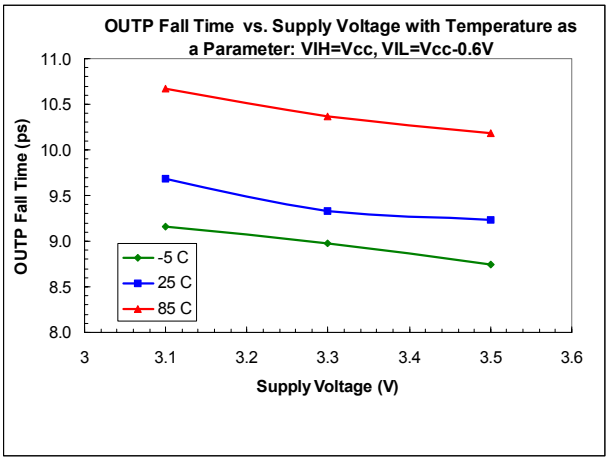


Figure 13. Typical data output fall time measured over power supply and temperature.

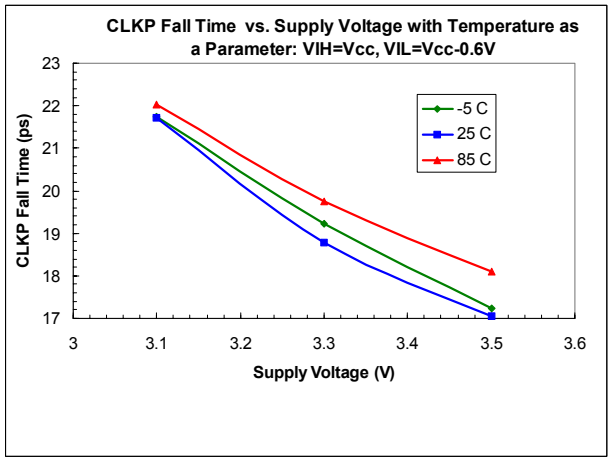


Figure 14. Typical clock output fall time measured over power supply and temperature.

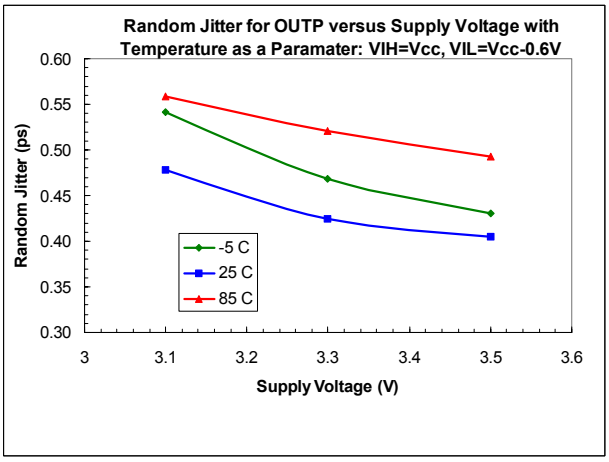


Figure 15. Data output RMS jitter measured using 25 Gbps 1010 pattern over supply and temperature. RMS jitter of scope and input were not removed.

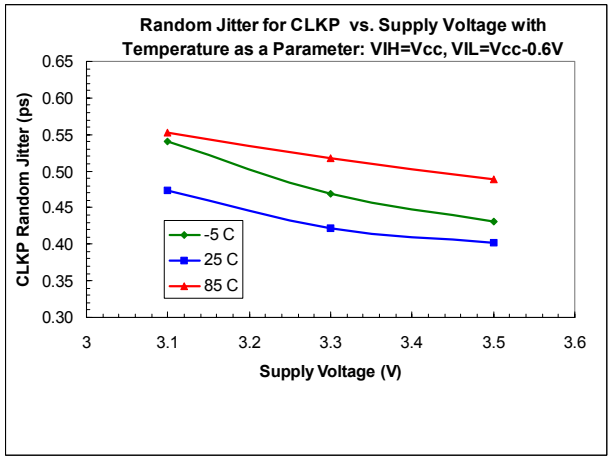


Figure 16. Clock output RMS jitter measured using 25 Gbps 1010 pattern over power supply and temperature. RMS jitter of scope and input were not removed.

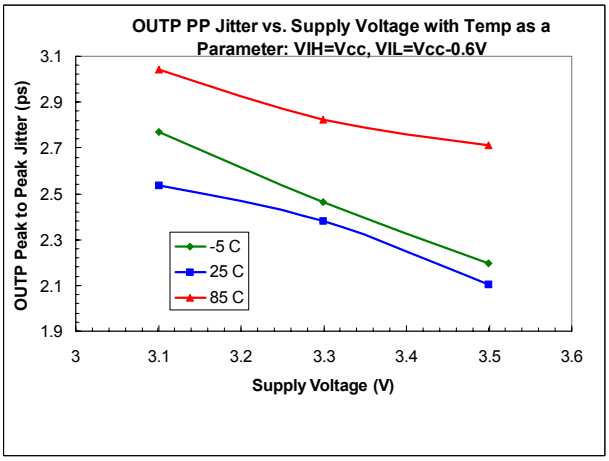


Figure 17. Data output Peak-to-peak jitter using 25 Gbps (2^7-1 PRBS) over power supply and temperature. The peak-to-peak jitter of the input was removed from the measurement.

Input and Output S-parameters

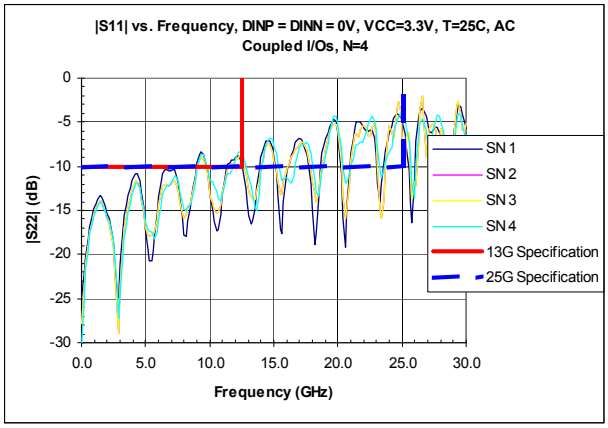


Figure 13. S11 magnitude measured on a data input from four packaged parts on evaluation boards with input common mode of V_{CC}.

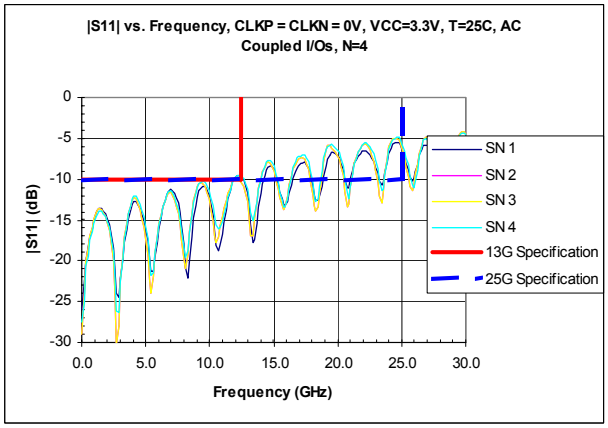


Figure 14. S11 magnitude measured on a clock input from four packaged parts on evaluation boards with input common mode of V_{CC}.

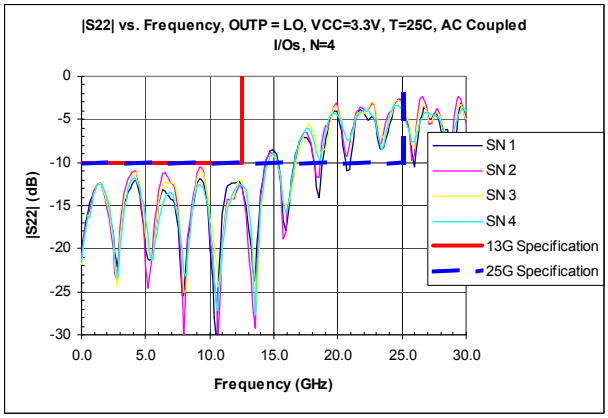


Figure 15. Data output logic low state S22 measured on four packaged parts on evaluation boards.

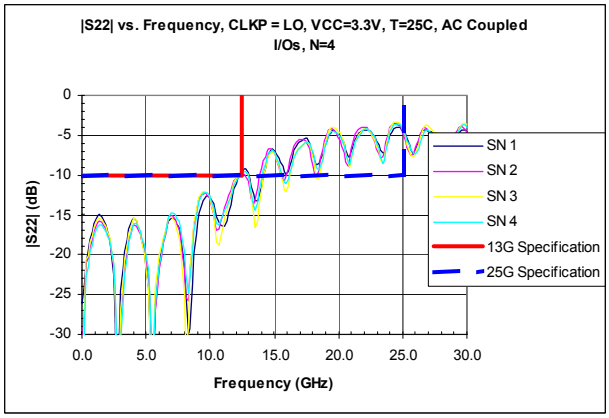


Figure 16. Clock output logic low state S22 measured on four packaged parts on evaluation boards.

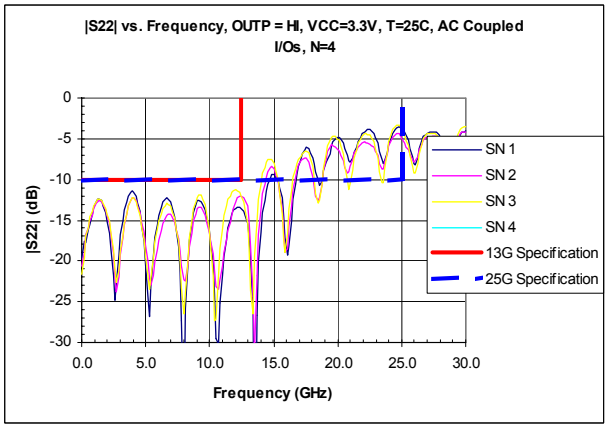


Figure 17. Data output logic high state S22 measured on four packaged parts on evaluation boards.

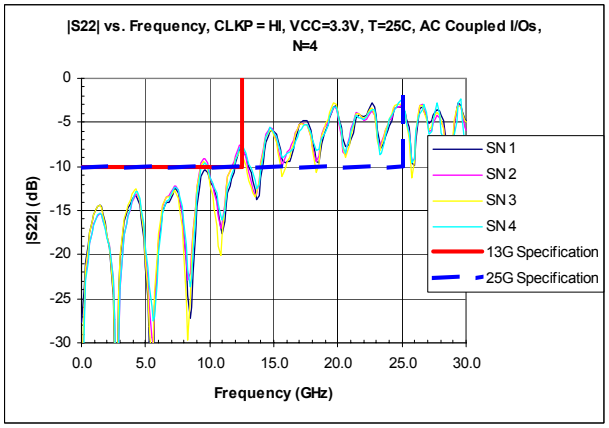
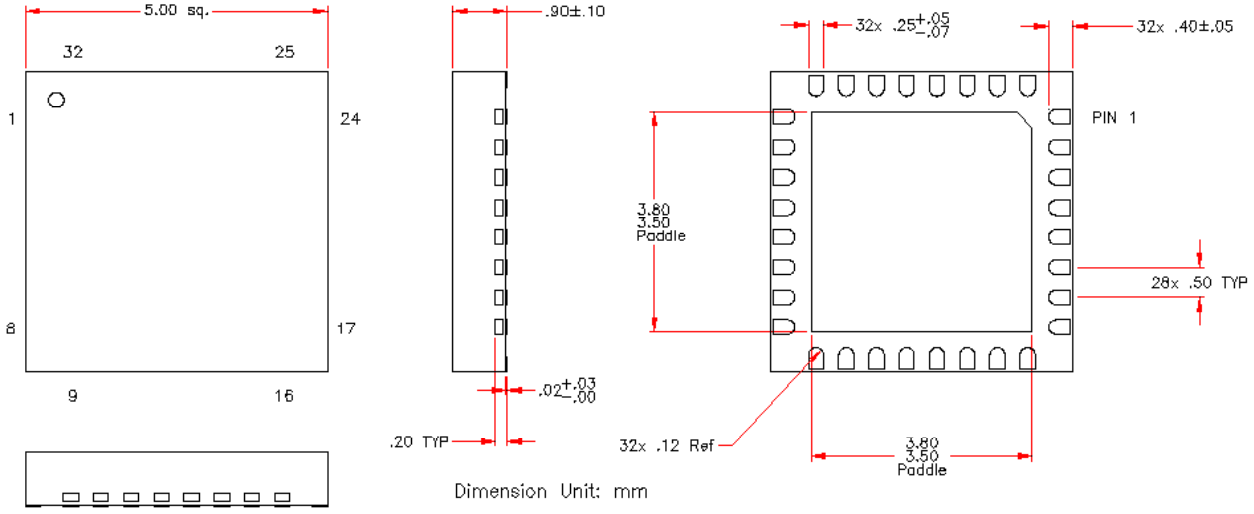


Figure 16. Clock output logic high state S22 measured on four packaged parts on evaluation boards.

QFN Pinout and Mechanical Drawing



Name	Pin	Description	Function
D_{IN0p}, D_{IN0n}, D_{IN1p}, D_{IN1n}, D_{IN2p}, D_{IN2n}, D_{IN3p}, D_{IN3n}	28, 29, 30, 31, 2, 3, 4, 5	Differential Data Inputs: On-chip 50 Ω termination to V_{CC} provided. Data inputs can be DC-coupled or AC-coupled. As well, they can be operated differentially or single-ended. When operated single-ended the unused input should be terminated with 50 Ω to V_{CC}. ***External AC coupling is required for ground-referenced signals***.	Input
CLK_{INp}, CLK_{INn}	20, 19	Clock Input: up to 20 GHz system clock input. On-chip 50 Ω termination to V_{CC} provided. Clock input can be DC-coupled or AC-coupled. As well, they can be operated differentially or single-ended. When operated single-ended the unused input should be terminated with 50 Ω to V_{CC}. ***External AC coupling is required for ground-referenced signals***.	Input
D_{OUTp}, D_{OUTn}	23, 22	High-Speed, Differential Data Output: up to 20 Gbps serial data. On-chip back-termination to V_{CC} provided to match to a 50 Ω characteristic impedance transmission line. ***External AC coupling is required for ground-referenced signals***.	Output
CLK_{OUTp}, CLK_{OUTn}	12, 11	Differential Clock Output: up to 5 GHz divide-by-4 clock output. On-chip back-termination to V_{CC} provided to match to a 50 Ω characteristic impedance transmission line. ***External AC coupling is required for ground-referenced signals***.	Output
V_{CC}	1, 7, 9, 14, 17, 26, 32	Power Supply: Connect to +3.3 V DC	Supply
GND	6, 10, 13, 15, 16, 18, 21, 24, 25, 27	Ground	Supply
DNU	8	Do not use. Not internally connected to the die	---

Notes:
1. The paddle must be electrically tied to ground.
2. All I/O pins must be AC coupled for ground reference use to prevent damage to the part.

Ordering Information

Part No.	Description
2080MX-S01QFN	20 Gbps 4:1 Mux (+3.3 Volt Supply) in QFN Package
2080MX-S01QFN-EVB	20 Gbps 4:1 Mux (+3.3 Volt Supply) in QFN Package on an Evaluation Board with SMA Connectors

Contact Information

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Limited Qualification Notification

NOTE: The 2080MX has undergone full design validation testing and meets the specifications outlined in this data sheet. However, it has not yet completed full qualification testing or absolute maximum characterization. Through extensive reliability testing, Inphi has demonstrated the reliability of other products fabricated in the semiconductor process used to fabricate the 2080MX. Contact Inphi for more details.

Inphi Corporation will honor the full warranty as outlined in Section 5 of Inphi's Standard Customer Purchase Order Terms and Conditions.

Updates From Previous Version

Initial Release.