DESCRIPTION

The sixteen megabit Synchronous Graphics RAM (SGRAM) is a single port, application specific memory device designed for graphics applications. It is organized as 256K words per bank x 32 bits per word x 2 banks. Internally, the SGRAM is organized as two separate banks, each comprising 1024 rows x 256 columns x 32 bits per data word. To refresh the SGRAM, the 1024 rows of each bank, 2048 rows in total, must be accessed within every 32 millisecond refresh interval. The synchronous interface of the SGRAM is similar to that of Synchronous DRAMs (SDRAMs) and is designed to achieve very high data rates. For a wide range of workstation and personal computer applications, the single 32 bit data port delivers sufficient bandwidth to refresh a video display while concurrently allowing rapid updates of the frame buffer by a graphics controller device.

FEATURES

- Fully synchronous; All signals referenced to a positive clock edge
- Single 3.3V±0.3V power supply
- Pipeline scheme
- Dual internal banks
- LVTTL compatible with multiplexed address
- MRS cycle with address key programs

- CAS Latency (2, 3)
- Burst Length (1, 2, 4, 8, Full Page)
- Burst Type (Sequential & Interleave)

- Byte control by DQMi
- Auto & self refresh
- 32ms refresh period (2K cycle)
- 100 Pin QFP
- SMRS cycle

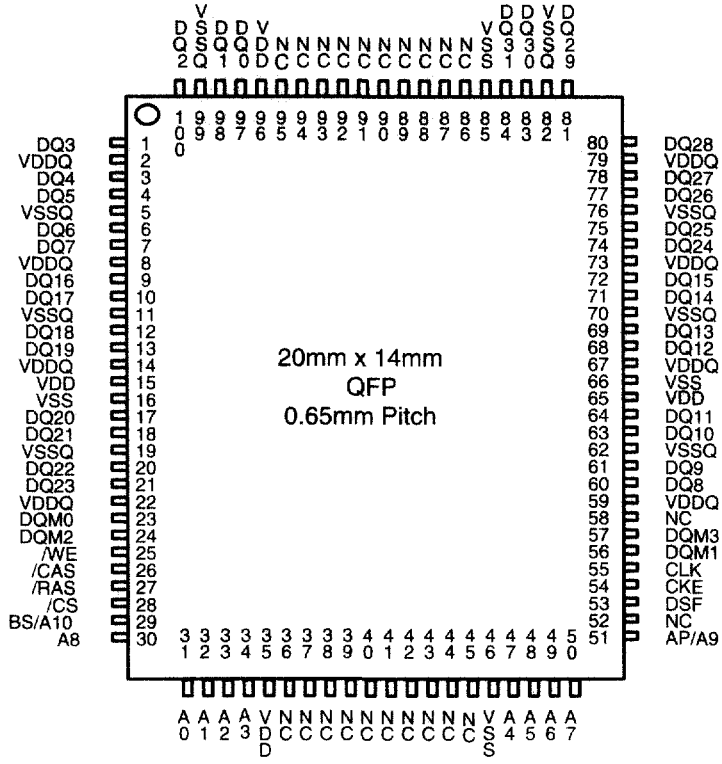
- Load mask register
- Load color register

- Persistent Write Per Bit (WPB)
- Block Write (8 Columns)

ORDERING INFORMATION

Part No.	Organization	I/O Interface	Package	Speed
HY58163210TQ-7F	256K x 32 x 2banks	LVTTL	TQFP	143MHz
HY58163210TQ-8F				125MHz
HY58163210TQ-10F				100MHz

PIN CONFIGURATION



(not drawn to scale)

Pin	Function
A0 - A10	Address Inputs
A0 - A9	Row Address Inputs
A0 - A7	Column Address Inputs
BS/A10	Bank Select
AP/A9	Auto Precharge
/CS	Chip Select
/CAS	Column Address Strobe
CKE	Clock Enable
CLK	System Clock Input
DQ0 - DQ31	Data Inputs/Outputs

Pin	Function
DQM0 - DQM3	DQ Mask Enable
DSF	Special Function Enable
NC	No Connection
/RAS	Row Address Strobe
VDD	Supply Voltage
VSS	Ground
VDDQ	Supply Voltage for DQs
VSSQ	Ground for DQs
/WE	Write Enable

Terms and Conventions

IOi, DQi, planei : The individual I/Os comprising the 32 bit DRAM port. DQi may also be used to refer to the specific package pin corresponding to I/Oi (planei).

byte 0 refers to data stored in or accessed from DQ7-DQ0 controlled by DQM0.
byte 1 refers to data stored in or accessed from DQ15-DQ8 controlled by DQM1.
byte 2 refers to data stored in or accessed from DQ23-DQ16 controlled by DQM2.
byte 3 refers to data stored in or accessed from DQ31-DQ24 controlled by DQM3.

write mask, or write mask register: A register comprising 32 bits, each bit controlling a write operation to one of the 32 planes. In write per bit mode, write mask bit i enables or disables a write operation to IOi (planei). The write mask is thus a write control register.

signal(CLK): The state of signal when CLK goes high.

address mask, column mask, or column address mask: The mask formed by DQ0-DQ7 for byte 0, DQ8-DQ15 for byte 1, DQ16-DQ23 for byte 2, and DQ24-DQ31 for byte 3 which replaces the column address bits A0-A3 during Block Write operations. The address mask contains only address information.

A signal is said to be asserted when it is in its active state, regardless if the signal is active high or active low. A signal is said to be negated if it is in its inactive state, regardless if the signal is active high or active low.

long word: the 32 bits of data, DQ0-DQ31 corresponding to a single memory address.

Don`t care state: designates that a signal can be in either the logic low state ($\leq$ a specified minimum voltage) or in the logic high state($\geq$ a specified maximum voltage).

PIN DESCRIPTION

PIN NAME	TYPE	FUNCTION
CLK	INPUT	CLK is driven by the system clock. All SGRAM inputs are sampled on the positive edge of CLK. CLK also controls the output registers.
CKE	INPUT	CKE determines validity of the next CLK. If CKE is high, the next CLK rising edge is valid, otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not asserted and the HY5816321 suspends operation. When the SGRAM is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low. In Self refresh mode, low level on this pins also used as part of the input command to specify Self refresh.
$\overline{CS}$	INPUT	$\overline{CS}$ low starts the command input cycle. When $\overline{CS}$ is high, commands are ignored but operation continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	INPUT	$\overline{CAS}$, $\overline{RAS}$ and $\overline{WE}$ define the command being entered.
DSF	INPUT	DSF is part of the graphic command of the SGRAM. If DSF is inactive, the SGRAM operates as same as SDRAM.
A0 - A9	INPUT	Row address is determined by A0 - A9 at the CLK rising edge in the activate command cycle. Column address is determined by A0 - A7 at the CLK rising edge at the read or write command cycle. A9 defines the precharge mode. When A9 is high in the precharge command cycle, both banks are precharged; when A9 is low, only the bank selected by A10 is precharged. When A9 high in read or write command cycle, the precharge start automatically after the burst access.
BS/A10	INPUT	A10 is the bank select signal(BS). In command cycle, A10 low selects bank 0 and A10 high selects bank1.
DQM0 - DQM3	INPUT	DQM controls I/O buffers. DQM0 controls DQ0 to DQ7, DQM1 controls DQ8 to DQ15, DQM2 controls DQ16 to DQ23, DQM3 controls DQ24 to DQ31. In read mode, DQM controls the output buffers like conventional $\overline{OE}$ pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.
DQ0 - DQ31	INPUT/ OUTPUT	Data I/O; Data bus. The I/Os are byte-maskable during read`s and write`s. The DQs also serve as column/byte mask inputs during block write`s.
V_{DDQ} V_{SSQ} V_{CC} V_{SS}	SUPPLY	DQ Power: Provide isolated power to DQs for improved noise immunity. DQ Ground: Provide isolated ground to DQs for improved noise immunity. Power Supply: 3.3V ± 0.3V Ground

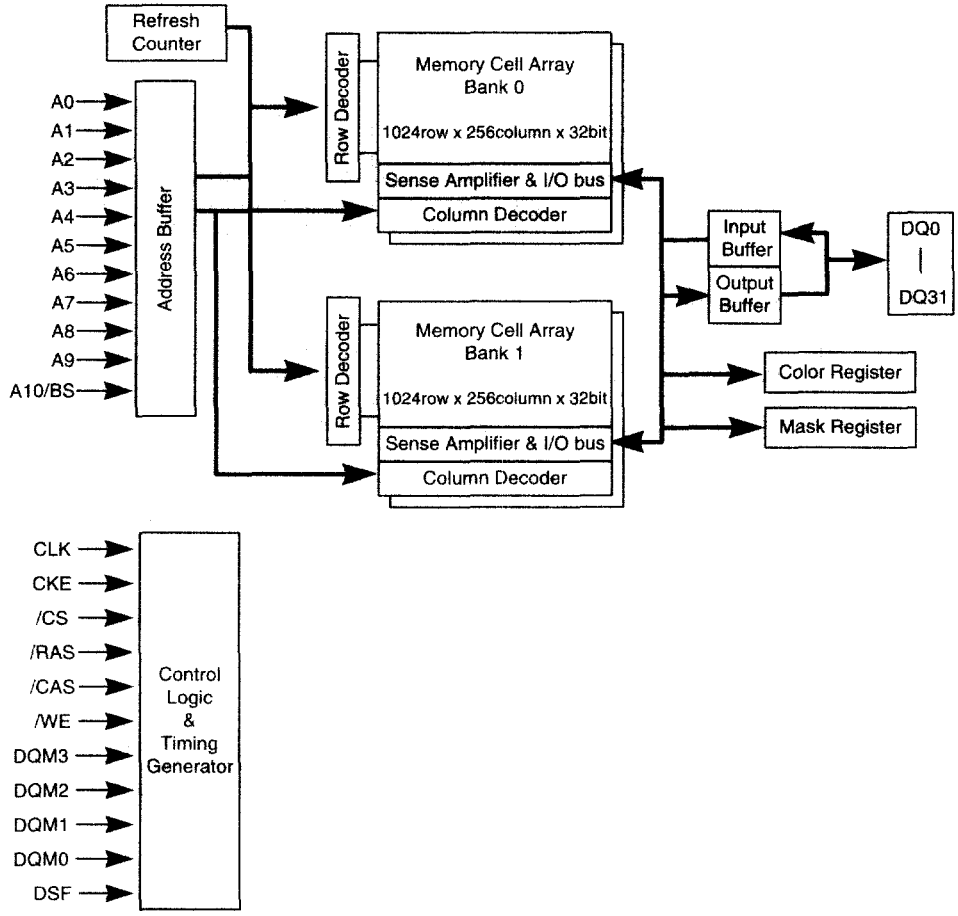


Figure 2. Simplified Block Diagram

Description of Functional Units

Input Block

All input to the SGRAM are registered at the positive edge of the system clock CLK. Two separate internal clock systems exist, one gated by the clock enable signal CKE and the other ungated. The gated clock system controls the various internal blocks, including RAM bank access, the state machine, and the read/write paths. The ungated clock is used to strobe the CKE input master slave DQ flip flop so that the gated internal clock can be internally disabled and re-enabled. The latched address, data, and control inputs are input to the state machine and command decode to select and control a cycle to be executed.

Command Decode and State Machine

The Command Decode consists of state registers and an instruction decoder. The Command Decode combines with the registered input block to form the state machine of the SGRAM. The state machine accepts new control inputs from the input block on each cycle to selectively change the state of the state machine and issue a new command to the SGRAM according to Tables 2 and 3.

Programmable Pipeline

To optimize performance for a wide variety of applications, the SGRAM has a programmable pipeline which adjusts the number of stages, and thus the access latency of data read from DRAM. The SGRAM can be programmed via a Mode Register Access to two, or three cycles of latency relative to CLK. Figure 8 shows how the two possible latencies for read and write operation are programmed via the mode register. Higher latency allows faster clock cycles to be used, which for relatively long data bursts results in substantial bandwidth improvements.

Mode Register

The mode register is a 11 bit register used to program the $\overline{CAS}$ latency for burst read operations and the burst length for read and write bursts. The mode register is loaded using the address pins, A9/AP-A0 plus the bank select input BS during Mode Register Access operations. See Table 2 for details on invoking a Mode Register access. The mode register is shown in Figure 8.

Write Mask Register

The write mask register is a 32 bit register used to control the internal write enables to each IO, or plane, in RAM. The write mask register is loaded during a Special Register ``Load write Mask Register`` (LMR). Once a Load Mask Register cycle is executed, the SGRAM goes into ``persistent`` write per bit mode, and will use the contents of the write mask on every write per bit write cycle thereafter until another LMR cycle is executed.

Color Register

The color register is a 32 bit register used as an alternate data source during block write operations. The register is loaded from the DQi inputs during Special Register ``Load Color Register``(LCR) cycles and is used as data during block write cycles. Once loaded, the color register cannot be altered except by another LCR cycle.

Refresh Counter

The Refresh Counter is a 11-bit counter used for auto refresh and self refresh operations. During refresh cycles, the refresh counter is input to the row decoder instead of the outputs of the row address buffers. The refresh counter increments after each refresh cycle, cycling through all 1204 rows of each bank, or 2048 rows in total. Refresh is performed in a ping pong manner between DRAM banks. That is, refresh cycle will alternate between bank 0 and bank 1 on successive refresh cycles.

Column Address Mask

During block write cycles, A7-A3 select a group of eight contiguous columns for write operation using the color register as the data source. The column mask is loaded from the DQ inputs at write time and is used to enable any arbitrary subset of these eight columns in RAM to be written using the contents of the color register. Separate 8-bit mask are loaded on DQ7-0, DQ15-8, DQ23-16, and DQ31-24, meaning that the subset of columns written to memory can be different for each byte. The column mask can be changed during each $\overline{CAS}$ cycle.

Timing

The timing block contains the various clock and control signals used to perform the various functions of the SGRAM. These signals are generally referenced to the input CLK signal and control addressing, sensing, and the read and write datapaths within the SGRAM.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	SYMBOL	RATING	UNIT
Voltage on VDD, VDDQ pins relative to ground	V_{DD}, V_{DDQ}	-0.5 to 4.6	V
Voltage on any pin relative to ground	Vin, Vout	-0.5 to 4.6	V
Short circuit output current	*Ios*	*50*	*mA*
Power Dissipation	P_D	1.3	W
Storage temperature (plastic package)	T_{STG}	-55 to 125	°C

Note:
1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}, V_{DDQ}	Supply voltage	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	2.0	3.0	V_{DD}+0.3	V
V_{IL}	Low-level input voltage	- 0.3	0	0.8	V
T_A	Operating free air ambient temperature	0		70	°C
C_L	External load capacitance on DQ			30	pF

Note:
1. Overshoot limit: V_{IH}(max)= VDD +1.5V with pulsewidth ≤ 5ns
2. Undershoot limit: V_{IL}(min)= -1.5V with pulsewidth ≤ 5ns

PIN CAPACITANCE VALUES

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IC}	Input capacitance: CLK, CKE, $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$, $\overline{WE}$,DSF, DQM	-	5	pF
C_{IA}	Input capacitance: BS/A10, AP/A9, A8 - A0	-	5	pF
$C_{I/O}$	Input/Output capacitance: DQ	-	7	pF

DECOUPLING CAPACITANCE GUIDE LINE
Recommended decoupling capacitance added to power line at board.

PARAMETER	SYMBOL	VALUE	UNIT
Decoupling Capacitance between V_{DD} and Vss	C_{DC1}	0.1+0.01	μF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1+0.01	μF

Notes:
1. V_{DD} an V_{DDQ} pins are separated each other.
   All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
2. Vss and V_{SSQ} pins are separated each other.
   All Vss pins are connected in chip. All V_{SSQ} pins are connected in chip.

OPERATING CURRENTS

(T_A=0 °C to 70 °C, V_{DD}=3.3V±10%, V_{SS}=0V, unless otherwise noted) Notes 1, 2

SYMBOL	PARAMETER/CONDITION	SPEED			UNIT	NOTE
		-7	-8	-10		
I_{DD1S}	Operating Current(Average Power Supply Current) Burst Length=4 t_{RC}=min., t_{CK}=min. at each operation One bank active 0V ≤ V_{IN} ≤ V_{DD} Outputs open addresses are changed up to 3 times during t_{RC}	250	230	190	mA	
I_{DD1D}	Operating Current(Average Power Supply Current) Burst Length=4 t_{RC}=min., t_{CK}=min. at each operation Two banks active 0V ≤ V_{IN} ≤ V_{DD} Outputs open addresses are changed up to 3 times during t_{RC}	380	340	280	mA	
I_{DD2P}	Precharge Stand-By Current(Power Supply Current) CKE=V_{IL} All banks idle t_{CK}=min. Power down mode 0V ≤ V_{IN} ≤ V_{DD}	4	4	4	mA	
I_{DD2PS}	Precharge Stand-By Current(Power Supply Current) CKE=V_{IL} All banks idle CLK=V_{IH} or V_{IL} Power down mode 0V ≤ V_{IN} ≤ V_{DD}	3	3	3	mA	
I_{DD2N}	Precharge Stand-By Current(Power Supply Current) CKE=V_{IH} Nop Commands only All banks idle t_{CK}=min. 0V ≤ V_{IN} ≤ V_{DD} Input signals are changed one time during 3 clock cycles	55	55	55	mA	
I_{DD2NS}	Precharge Stand-By Current(Power Supply Current) CKE=V_{IH} All banks idle CLK= V_{IH} or V_{IL} 0V ≤ V_{IN} ≤ V_{DD} Input signals are stable	20	20	20	mA	
I_{DD3P}	Active Stand-By Current(Power Supply Current) CKE=V_{IL} Any banks active t_{CK}=min. 0V ≤ V_{IN} ≤ V_{DD}	20	20	20	mA	
I_{DD3PS}	Active Stand-By Current(Power Supply Current) CKE=V_{IL} Any banks active CLK= V_{IH} or V_{IL} 0V ≤ V_{IN} ≤ V_{DD} Input signals are stable	20	20	20	mA	

OPERATING CURRENTS(Continued)
(T_A=0 °C to 70 °C, V_{DD}=3.3V±10%, V_{SS}=0V, unless otherwise noted) Notes 1, 2

SYMBOL	PARAMETER/CONDITION	SPEED			UNIT	NOTE
		-7	-8	-10		
I_{DD3N}	Active Stand-By Current(Power Supply Current) CKE=V_{IH} Nop Commands only Any banks active t_{CK}=min. 0V ≤ V_{IN} ≤ V_{DD} Input signals are changed one time during 3 clock cycles	90	90	90	mA	
I_{DD3NS}	Active Stand-By Current(Power Supply Current) CKE=V_{IH} Any banks active CLK= V_{IH} or V_{IL} 0V ≤ V_{IN} ≤ V_{DD} Input signals are stable	30	30	30	mA	
I_{DD4}	Burst mode Current(Average Power Supply Current) t_{CK}=min. Outputs open 0V ≤ V_{IN} ≤ V_{DD} Any banks active gapless data, burst length=4, Addresses are changed only one time during t_{CK}(min.)	290	260	220	mA	
I_{DD5}	Refresh Current #1(Average Power Supply Current) Auto-Refresh; t_{CK}=min., t_{RC}=min. 0V ≤ V_{IN} ≤ V_{DD}	240	210	180	mA	
I_{DD6}	Refresh Current #2(Average Power Supply Current) Self-Refresh; CKE=V_{IL} 0V ≤ V_{IN} ≤ V_{DD}	4	4	4	mA	
I_{DD7}	Block Write Current(Average Power Supply Current) Block Write; t_{CK}=min., t_{BWC}=min. 0V ≤ V_{IN} ≤ V_{DD}	270	240	210	mA	

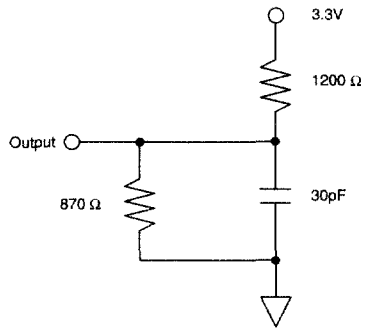
Notes:
1. I_{DD} depends on the outputs termination or load conditions, clock cycle rate and signal clocking rate; The specified values are obtained with the output open and no termination register.
2. An initial pause(DESL or NOP) of 200μs is required after power-up followed by a minimum of eight Auto-refresh cycles.

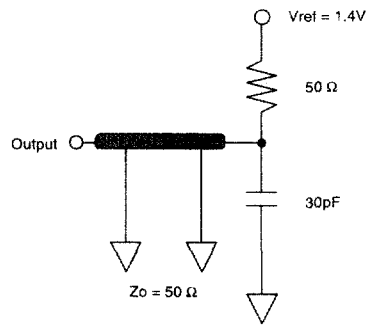
DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
V_{OH}	High - level output voltage	I_{OH} = -2 mA	2.4		V
V_{OL}	Low - level output voltage	I_{OL} = 2 mA		0.4	V
I_{LI}	Input leakage current	0 ≤ Vin ≤ 4.0V All other pins at ground	-10	+10	μA
I_{LO}	Output leakage current	0 ≤ Vout ≤ V_{DD}, DQ disabled Both banks in idle state	-10	+10	μA

AC OPERATING TEST CONDITIONS

PARAMETER	VALUE
AC input levels	V_{IH}/V_{IL}=2.4V/0.4V
Input timing measurement reference level	1.4V
Input rise and fall time	tr/tf=1ns/1ns
Output measurement reference level	1.4V
Output load condition	See figure (b)





V_{OH}(DC)=2.4V I_O= -2mA
V_{OL}(DC)=0.4V I_O= 2mA

(a) Output load circuit for DC measurements (b) Output load circuit for AC measurements

AC CHARACTERISTICS
TIMING PARAMETERS AND DIAGRAMS

SYNCHRONOUS TIMING PARAMETERS (C_{LOAD} = 30pF)											
PARAMETER		SYMBOL		-7		-8		-10		UNIT	NOTE
				Min.	Max.	Min.	Max.	Min.	Max.		
Clock cycle time	CL=3	t_{CK3}		7	-	8	-	10	-	ns	
	CL=2	t_{CK2}		10	-	12	-	15	-	ns	1
Access time from CLK	CL=3	t_{AC3}		-	6	-	7	-	7	ns	
	CL=2	t_{AC2}		-	9	-	10	-	12	ns	1,2
CLK pulsewidth high		t_{CHW}		2.5	-	3	-	3.5	-	ns	3
CLK pulsewidth low		t_{CLW}		2.5	-	3	-	3.5	-	ns	3
Data-out holdtime		t_{OH}		2	-	2	-	3	-	ns	2
Data-out low impedance time		t_{LZ}		0	-	0	-	0	-	ns	2
Data-out high impedance time	CL=3	t_{HZ}		2	7	2	7	2	7	ns	
	CL=2			2	10	2	10	2	10	ns	
Set-up time to CLK	Data	t_{SU}	t_{DS}	2	-	2.5	-	3	-	ns	3
	Address		t_{AS}								
	Command		t_{CS}								
Hold time to CLK	Data	t_H	t_{DH}	1	-	1	-	1	-	ns	3
	Address		t_{AH}								
	Command		t_{CH}								
Set-up time to CLK, CKE at Power Down Exit		t_{SUCKP}		3	-	3.5	-	4	-	ns	4

Notes:

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2 - 0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf)=1ns. If tr & tf is longer than 1ns, transient time compensation should be considered. I.e.,[(tr+tf)/2 - 1]ns should be added to the parameter.
4. A time of t_{SUCKP} has to elapse after asserting CKE to resume normal operation when exiting power down mode.

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

PARAMETER	SYMBOL	-7	-8	-10	UNIT	NOTE
Row active to Row active delay	t_{RRD}(min)	14	16	20	ns	1
/RAS to /CAS delay	t_{RCD}(min)	21	24	30	ns	1
Row precharge time	t_{RP}(min)	21	24	30	ns	1
Row active time	t_{RAS}(min)	42	48	60	ns	1
	t_{RAS}(max)	100			µs	-
Row cycle time	t_{RC}(min)	63	72	90	ns	1
Last data in new col. Address delay	t_{CDL}(min)	1			CLK	2
Last data in to Row precharge	t_{RWL}min)	1			CLK	2
Last data in to burst stop	t_{BDL}(min)	1			CLK	2
Col. Address to col. Address delay	t_{CCD}(min)	1			CLK	3
Block write cycle time	t_{BWC}(min)	14	16	20	ns	1,4
Number of valid output data	CAS latency=3	2			-	5
	CAS latency=2	1				

Notes:

1. The minimum number of clock is determined by dividing the minimum time required with clock cycle time, and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every column address change except block write cycle.
4. This parameter means minimum /CAS to /CAS delay at block write cycle only.
5. In case of Row precharge interrupt, Auto precharge and Read burst stop.

Table 1. Relationship Between Frequency and Minimum Latency

Parameter	Symbol	CL	-7		-8		-10		Note
		tCK	3 7	2 10	3 8	2 12	3 10	2 15	
Read command to output valid data	tCAS		3	2	3	2	3	2	
Active command to column command (same bank)	tRCD		3	2	3	2	3	2	
Active command to active command (same bank)	tRC		9	6	9	6	9	6	=(tRAS+tRP)
Active command to precharge command (same bank)	tRAS		6	4	6	4	6	4	
Precharge command to active command (same bank)	tRP		3	2	3	2	3	2	
Last data in to precharge command (same bank)	tRWL		1	1	1	1	1	1	
Block write to precharge command	tBWL		2	2	2	2	2	2	=(tRWL+1)
Active command to active command (different bank)	tRRD		2	2	2	2	2	2	
Last data in to active command (Auto precharge, same bank)	tAPW		4	3	4	3	4	3	=(tRWL+tRP)
Block write to active command (Auto precharge, same bank)	tAPBW		5	4	5	4	5	4	=(tBWL+tRP)
Self refresh exit to command input	tSREX		9	6	9	6	9	6	=tRC
Precharge command to high impedance	tHZP		3	2	3	2	3	2	
Last data out to active command	tAPR		1	1	1	1	1	1	=(tEP+tRP)
Last data out to precharge	tEP		-2	-1	-2	-1	-2	-1	
Column command to column command	tCCD		1	1	1	1	1	1	
Write command to data in latency	tWCD		0	0	0	0	0	0	
Block write cycle time	tBWC		2	2	2	2	2	2	
Special mode register set to block write	tSBW		2	2	2	2	2	2	
DQM to data in	tDID		0	0	0	0	0	0	
DQM to data out	tDOD		2	2	2	2	2	2	
CKE to CLK disable	tCLE		1	1	1	1	1	1	
Burst stop to output valid data hold	tBSR		2	1	2	1	2	1	
Burst stop to output high impedance	tBSH		3	2	3	2	3	2	
MRS to active command	tRSA		2	2	2	2	2	2	
SMRS to active command	tSSA		2	2	2	2	2	2	
Active command to SMRS	tASS		3	2	3	2	3	2	
Register set to register set	tRR		2	2	2	2	2	2	

Table 2. State and Function Truth Table for Selected Bank

Current state of Selected Bank	CLK↑										Action to selected bank (Unless otherwise noted)
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BS	A9	A8 ~ A0	DQMi	DQi	
Idle	L	L	L	L	L	opcode			X	X	Mode Register set
	L	L	L	L	H	X	X	op code	X	X	Special Register set
	L	H	H	H	X	X	X	X	X	X	NOP
	H	X	X	X	X	X	X	X	X	X	
	L	L	H	L	L	BA	RA	X	X		
	L	L	H	H	L	BA	RA	RA	X		Activate Row, Bank Deselect WPB Mask
	L	L	H	H	H	BA	RA	RA	X		Activate Row, Bank Select WPB Mask
Row Active	L	L	L	L	H	X	X	op code	X	X	Special Register Set
	L	H	H	H	X	X	X	X	X	X	NOP
	H	X	X	X	X	X	X	X	X	X	
	L	L	H	L	L	BA	L	X	X	X	Precharge selected Bank
	L	L	H	L	L	X	H	X	X	X	Precharge Both Banks
	L	H	L	L	L	BA	L	CA	byte enable	data in	Begin Write
	L	H	L	L	H	BA	L	CA	byte enable	addr mask	Begin Block Write
	L	H	L	L	L	BA	H	CA	byte enable	data in	Begin Write, Auto Precharge
	L	H	L	L	H	BA	H	CA	byte enable	data in	Begin Block Write, Auto Precharge
	L	H	L	H	L	BA	L	CA	byte enable	data out	Begin Read
	L	H	L	H	L	BA	H	CA	byte enable	data out	Begin Read, Auto Precharge
Read	L	H	H	H	X	X	X	X	X	data out	NOP, *continue burst to* end → Row Active
	H	X	X	X	X	X	X	X	X	data out	
	L	L	H	L	L	BA	L	X	X	data out	Term Burst, Precharge selected Bank
	L	H	L	L	L	X	H	X	X	data out	Term Burst, Precharge Both Banks
	L	H	L	L	L	BA	L	CA	X	data out	Term Burst, Begin Write[2]
	L	H	L	L	L	BA	H	CA	X	data out	Term Burst, Begin Write, Auto Precharge[2]
	L	H	L	L	H	BA	L	CA	X	data out	Term Burst, Begin Block Write[2]
	L	H	L	L	H	BA	H	CA	X	data out	Term Burst, Begin Block Write, Auto Precharge[2]
	L	H	L	H	L	BA	L	CA	X	data out	Term Burst, Begin New Read
	L	H	L	H	L	BA	H	CA	X	data out	Term Burst, Begin New Read. Auto Precharge
	L	H	H	L	L	X	X	X	X	data out	Term Burst → Row Active

Table 2. State and Function Truth Table for Selected Bank[1](Continued)

Current state of Selected Bank	CLK↑										Action to selected bank (Unless otherwise noted)
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BS	A9	A8 -A0	DQMi	DQi	
Write	L	H	H	H	X	X	X	X	X	data in	NOP, continue burst to end → Row Active
	H	X	X	X	X	X	X	X	X	data in	
	L	L	H	L	L	BA	L	X	X	X	Term Burst, Precharge Selected Bank
	L	L	H	L	L	X	H	X	X	X	Term Burst, Precharge Both Banks
	L	H	L	L	L	BA	L	CA	X	X	Term Burst, Begin New Write
	L	H	L	L	L	BA	H	CA	X	X	Term Burst, Begin New Write, Auto Precharge
	L	H	L	L	H	BA	L	CA	X	X	Term Burst, Begin New Block Write
	L	H	L	L	H	BA	H	CA	X	X	Term Burst, Begin New Block Write, Auto Precharge
	L	H	L	H	L	BA	L	CA	X	X	Term Burst, Begin New Read
	L	H	L	H	L	BA	H	CA	X	X	Term Burst, Begin New Read, Auto Precharge
	L	H	H	L	L	X	X	X	X	X	Term Burst → Row Active
Read, Auto - Prchg	L	H	H	H	X	X	X	X	X	data out	NOP, continue burst to end → Precharge[3]
	H	X	X	X	X	X	X	X	X	data out	
Write, Blk Write, Auto - Prchg	L	H	H	H	X	X	X	X	X	data in	NOP, continue burst to end → Precharge[3]
	H	X	X	X	X	X	X	X	X	data in	
Prchrging	L	L	H	L	X	BA	L	X	X	X	NOP → Idle after tRP
	L	H	H	H	X	X	X	X	X	X	NOP → Idle after tRP
	H	X	X	X	X	X	X	X	X	X	
Row Activating	H	X	X	X	X	X	X	X	X	X	NOP → Row Active after tRCD[4]
	L	H	H	H	X	X	X	X	X	X	
Mode Reg. Accessing	L	H	H	H	X	X	X	X	X	X	NOP
	H	X	X	X	X	X	X	X	X	X	
Special Mode Reg. Accessing	L	H	H	H	X	X	X	X	X	X	NOP
	H	X	X	X	X	X	X	X	X	X	

Notes:

1. Assumes CKE high on the previous clock cycles.
2. Read burst must terminate one cycle before the start of a write sequence. This can be accomplished in one of two ways. First, if the last bit of the burst is output two cycles before the start of the write sequence, the burst will terminate and the output will tristate during the cycle before the write command is issued. Second, the burst can be terminated by bringing DQMi high and issuing a terminate burst command two cycles before the write command. This will also guarantee that the output will tristate and the read pipeline will be flushed during the cycle before the write command is issued.
3. Within a Read or Write burst sequence with Auto Precharge selected, no Read or Write commands are allowed to the opposite bank. However, a read or write burst (with or without auto precharge selected) can be invoked in the opposite bank on the clock cycle corresponding to the last address of the burst in progress in the current bank.

4. tRCD specifies the minimum period beginning from the start of a row activate command and the start of a read burst, write burst, or block write command in the same bank. Only NOP commands are allowed during this period to the selected bank. After the tRCD minimum period has expired, but before the minimum row activation period tRAS has expired, no precharge or burst terminate commands can be invoked on that bank. This is analogous to the minimum tRAS period found in previous generation asynchronous DRAMs.

Table 3. State and Function Truth Table, Operation involving Both Banks

Current state	CLK↑												Action
	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DSF	BS	A9	A8-A0	DQMi	DQi	
	n-1	n											
Power Down	L	L	X	X	X	X	X	X	X	X	X	X	Maintain Power Down
	L	H	L	H	H	H	X	X	X	X	X	X	Exit Power Down → BBI
	L	H	H	X	X	X	X	X	X	X	X	X	
Self Refresh[1]	L	L	X	X	X	X	X	X	X	X	X	X	Maintain Self Refresh
	L	H	L	H	H	H	X	X	X	X	X	X	Exit Self Refresh → BBI
	L	H	H	X	X	X	X	X	X	X	X	X	
Both Banks Idle(BBI)	H	L	L	H	H	H	X	X	X	X	X	X	Enter Power Down
	H	L	H	X	X	X	X	X	X	X	X	X	Enter Power Down
	H	L	L	L	L	H	X	X	X	X	X	X	Enter Self Refresh
	H	H	L	H	H	H	X	X	X	X	X	X	NOP
	H	H	H	X	X	X	X	X	X	X	X	X	NOP
	H	H	L	L	L	L	L	op code			X	X	Mode Reg. Access
	H	H	L	L	L	L	H	X	X	op code	X	X	Special Register Access
	H	H	L	L	L	H	L	X	X	X	X	X	Auto Refresh
CLK Suspend	L	L	X	X	X	X	X	X	X	X	X	X	Maintain CLK Suspend
	L	H	X	X	X	X	X	X	X	X	X	X	Exit CLK Suspend
Auto refreshing	H	H	L	H	H	H	X	X	X	X	X	X	NOP → Both Banks
	H	H	H	X	X	X	X	X	X	X	X	X	Idle after tRC
Any state other than above	H	L	Any valid command for specified state										Enter CLK Suspend[2]
	H	H											See Table2

Notes:
1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high.
2. The valid command specified during the Enter CLK Suspend cycle will be executed, and the next clock cycle will be ignored as well all subsequent clock cycles until CLK Suspend is exited.

Summary of Functions and Function Invocation

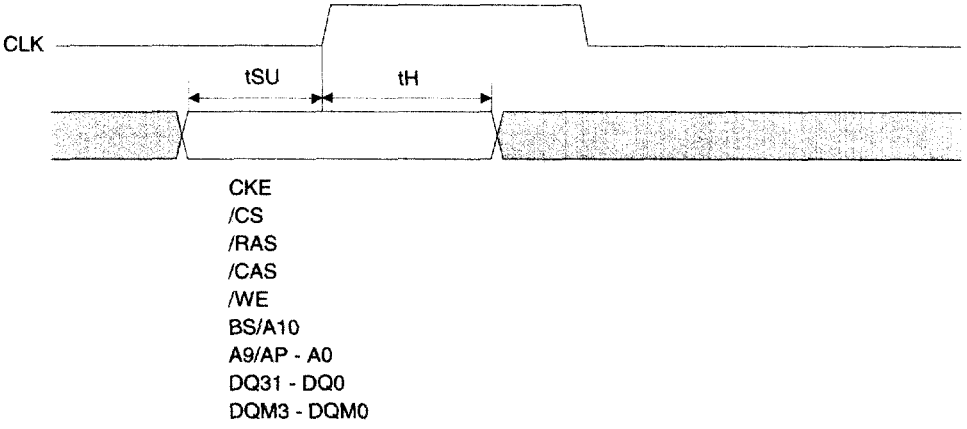


Figure 3. General Cycle Invocation Scheme for SGRAM

General Cycle Select

The available functions of the SGRAM are selected according to the values of the various control inputs at each rising edge of CLK and the internal state of the SGRAM at that time. Figure 3 shows how each control input must be valid with an adequate set up and hold time relative to the rising edge of CLK to perform the desired command. Tables 2 and 3 show the complete state table and command set for the SGRAM.

General State Transition and Command Sequence for One Bank

With few exceptions, the two banks of the SGRAM operate autonomously according to which bank is selected by the BS/A10 signal for any given cycle type. Figure 4 shows a simplified arrangement of the possible state transitions for each bank operating separately. Normally, a row of DRAM in one of the two banks is activated. While the bank is activating, only NOP cycles are allowed to that bank. After a certain time period, the bank enters its active state, designated by Row Active. Once in the Row Active state, commands for executing Read, Read with Auto Precharge, Write (including block write and write per bit), and Write with Auto Precharge can be executed, which transition the bank to the appropriate state and allow read or write bursting to occur. Reads and Writes can be intermixed along the same row, or page address, however certain timing parameters and clock cycle latencies must be observed when switching between the read and write states. Read and Write operation to the selected bank (without Auto Precharge selected) can be terminated in one of four ways:

1) By issuing a precharge command to the selected bank
   → Goes to Precharging state
2) By issuing a burst terminate command
   → Goes to Row Active state
3) By issuing a read or write command to the opposite bank
   → Current bank goes to Row Active state
4) By reaching the end of the burst (burst length=1, 2, 4, or 8 only).
   → Goes to Row Active state

NOTE:

If the burst length is set to full page, the burst will not terminate even after all addresses in the full page burst have been read or written. The burst can only be terminated by issuing one of commands 1-3 above.

Read and Write operation to the selected bank(with Auto Precharge selected) can be terminated only by reaching the end of the selected burst, after which that bank goes to the precharging state. Auto Precharge is not supported for burst length equal to full page.

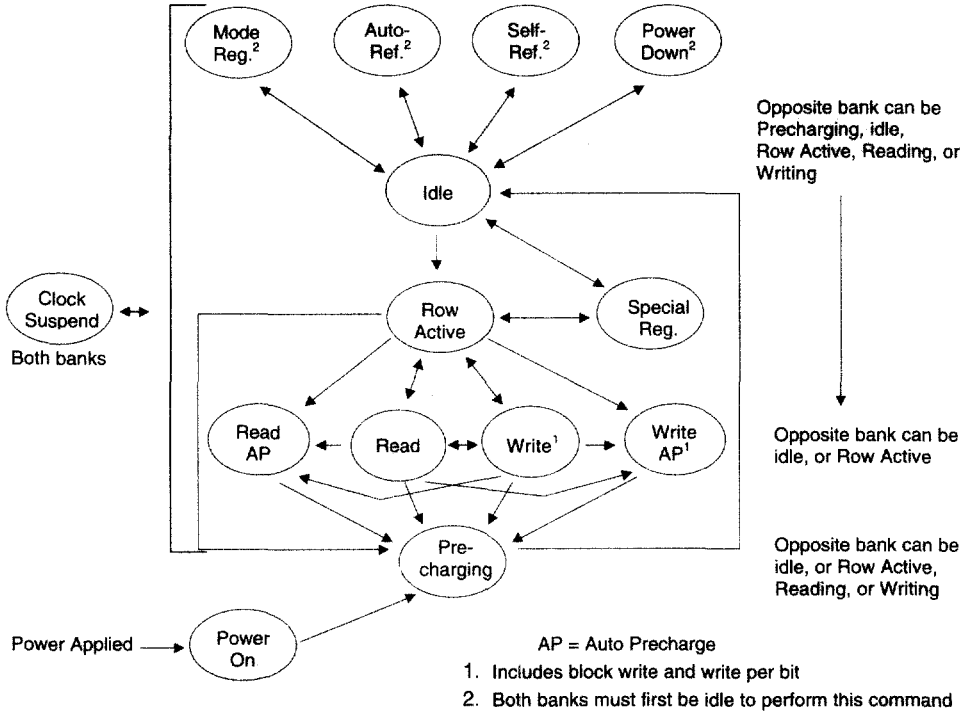


Figure 4. Simplified state transition diagram for each bank.

After precharge of the selected bank is invoked, that bank enters the "Precharging" state for some specified period of time during which only NOP cycles can be executed to that bank. After the specified precharge interval is expired, the bank re-enters the Idle state. It is important to note that while either bank is transiting from one state to another according to Figure 4, the opposite bank can be active. Due to the single read and write port of the SGRAM, the two banks cannot be reading or writing simultaneously. For example, if bank 0 is in the read state and bank 1 is in the row active state, a new read command given with bank 1 selected by BS/A10, will cause bank 1 to enter the read state and bank 0 to terminate its burst and enter the row active state. While a bank is in the row active, read, or write state, the clock signal can be suspended. This causes the external clock signal to be ignored and all cycles to be decoded as NOPs. Suspending the clock affects both banks, regardless of which ones are active.

Operation(cycle description, timing overview)

1.1 Mode Register Programming

Description of Register Functions

The SGRAM has an on chip mode register which is programmed by the user to select the read latency, burst length and burst type to be used during read / write operations to the DRAM.

To achieve very high data rates, the SGRAM is equipped with a read pipeline which can be programmed by the user to operate with one, two, or three cycles of clock latency. Read latency is defined as the number of the first positive clock edge following the initial read invocation cycle (which we arbitrarily define as clock 0) at which the first piece of data is guaranteed to be valid. Figure 5 illustrates read latencies of one, two, and three. The higher the latency, the higher the clock frequency the SGRAM can run at, and the higher the peak data rate.

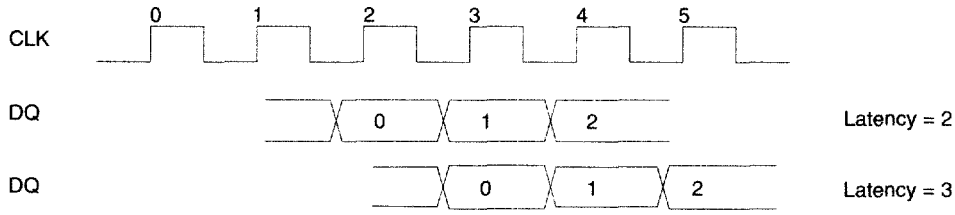


Figure 5. Definition of Read Latency with Examples

Whenever a read (or write) command is invoked, the SGRAM initiates a read (or write) to the appropriate column address selected by A7-A0. This is defined as the beginning of the read (or write) burst. Subsequent clock cycles can be used to perform high speed reads (or writes) to column addresses adjacent to the column address supplied on A7-A0 when the read or write was invoked. The number of column addresses which can be read or written, including the original address supplied on A7-A0 is defined as the burst length. The SGRAM supports burst lengths of one, two, four, eight, and a full page of column addresses.

The SGRAM supports both sequential and interleave mode address bursting. In burst mode, read or write is done to the address selected by A7-A0 at the beginning of the burst. On successive burst cycles, the column address is internally incremented and a read (or write) is performed to the incremented address. The process can continue until a read(or write) to the most significant address in the burst has been executed. On the next burst cycle, the internal address will wrap to the least significant address of the burst and a read (or write) to that address will be executed. Successive burst cycles will cause the column address to internally increment and a read (or write) to the incremented address will occur until reads (or writes) to all addresses in the burst have been executed.

For all burst lengths, except full page, the burst have been read (or written). For full page mode, the burst must be explicitly terminated by a separate command. Table 4 show the sequence of burst addressing for burst lengths of two, four, eight, and full page.

Table 4. Address sequence for different burst lengths

Burst Length = 2

Starting column address A0(decimal)	Sequential	Interleave
0	0,1	0,1
1	1,0	1,0

Burst Length = 4

Starting column address $A_1 - A_0$(decimal)	Sequential	Interleave
0	0,1,2,3	0,1,2,3
1	1,2,3,0	1,0,3,2
2	2,3,0,1	2,3,0,1
3	3,0,1,2	3,2,1,0

Burst Length = 8

Starting column address $A_2 - A_0$(decimal)	Sequential	Interleave
0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
1	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
2	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
3	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
4	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
5	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
6	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
7	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

Burst Length = full page

Starting column address $A_7 - A_0$(decimal)	Sequential
0	0,1,2,···,255
1	1,2,3,···,255,0
2	2,3,4,···,255,0,1
3	3,4,5,···,255,0,1,2
.	.
.	.
.	.
255	255,0,1,···,254

Loading the Mode Register

Figure 6 shows the general timing and control for loading the mode register per Table 2. Figure 8 shows the assignment of the op code bits to the mode register and how the mode register bits control latency and burst operation.

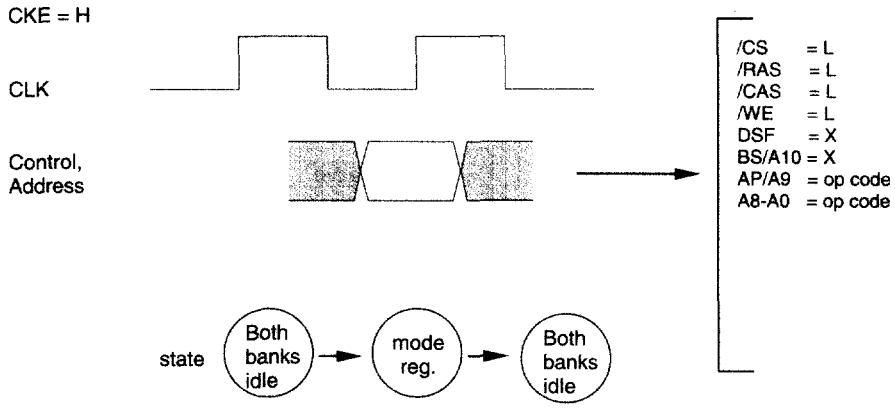
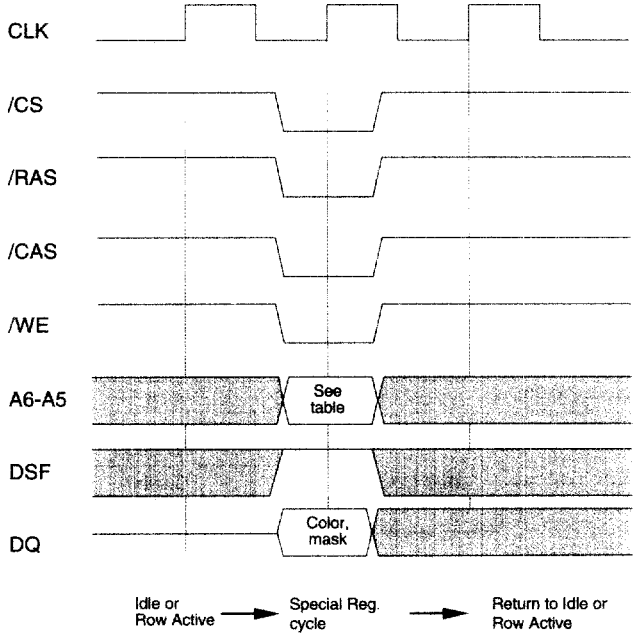


Figure 6. Timing of mode register access (Program latency and burst length)

1.2 Special Mode Operations (loading the color register, WPB mask)

To support write per bit and block write operations, the SGRAM has a write per bit mask register and a color register. Every Special Register Access allows one of these registers to be written with the contents of the DQ pins. The write per bit register and the color register are not byte writable. The DQM pins have no impact during Special Register Access operations. Write per bit operation is not available when loading the write per bit mask register or the color register. Special Register Access cycles are invoked as described in Table 2 and can only be invoked when both banks are in either the idle or row active state. Figure 7 shows the general timing and control for the Special Register Access cycle and illustrates how the opcode supplied on address bits A6 and A5 determine which of the two registers, the write mask register or the color register, gets loaded from the DQ pins. A6 and A5 are used to determined whether loading color data or mask data, other pins should be low, color data and mask data are loaded through DQ pins into the color register and the mask register respectively.



A6	A5	Action
0	0	NOP
0	1	Load Write Mask Reg.
1	0	Load Color Reg.
1	1	Illegal

Figure 7. Timing and control for special register access cycle

Mode Register Configuration

A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	Write Mode	0	0	CAS Latency			BT	BL		

Write Mode		CAS Latency				Burst Type		Burst Length				
A9	Length	A6	A5	A4	Latency	A3	Type	A2	A1	A0	BT=0	BT=1
0	Burst	0	0	0	R	0	Sequential	0	0	0	1	R
1	Single Bit Note1	0	0	1	R	1	Interleave	0	0	1	2	2
		0	1	0	2			0	1	0	4	4
		0	1	1	3			0	1	1	8	8
		1	0	0	R			1	0	0	R	R
		1	0	1	R			1	0	1	R	R
		1	1	0	R			1	1	0	R	R
		1	1	1	R			1	1	1	F. P. Note2	R

Special Mode Register Set

A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	LC	LM	0	0	0	0	0

Load Mask	A5	Function
	0	Disable
	1	Enable Note3

Load Color	A6	Function
	0	Disable
	1	Enable Note3

Notes:
1. When A9=1, burst length at Write is always one regardless of BL value.
2. Sequential Burst Type Only.
3. If both LC and LM are high, data of mask and color register will be unknown.

Figure 8. Loading of the mode register and special mode register

2. Row activate

A single row in either bank of DRAM can be activated using a row activate command. A bank can be activated even when the opposite bank is active. A row activate command cannot be given to a bank if that bank is already active. Also, a row activate command cannot be given to either bank if the SGRAM is currently in the power down, self refresh, auto refresh(for the period specified by tRC), or clock suspend states. Once a row activate command has been issued to the bank selected by the bank address (supplied by BS/A10), the selected bank leaves its idle state and goes into its row activating state. Accordingly, the row address is latched and the appropriate row in the bank is selected. Data from that row of memory is sensed and latched by the bank's sense amplifiers, to be used for later read (or write) operations. Figure 9 shows a row activation cycle per Table 2 with and without write per bit selected. tRCD specifies the minimum period beginning from the start of a row activate command and the start of a read burst, write burst, or block write command in the same bank. Only NOP commands are allowed during this period to the selected bank. After the tRCD minimum period has expired, but before the minimum row activation period tRAS has expired, no precharge or burst terminate commands can be invoked on that bank. This is analogous to the minimum tRAS period found in previous generation asynchronous DRAMs.

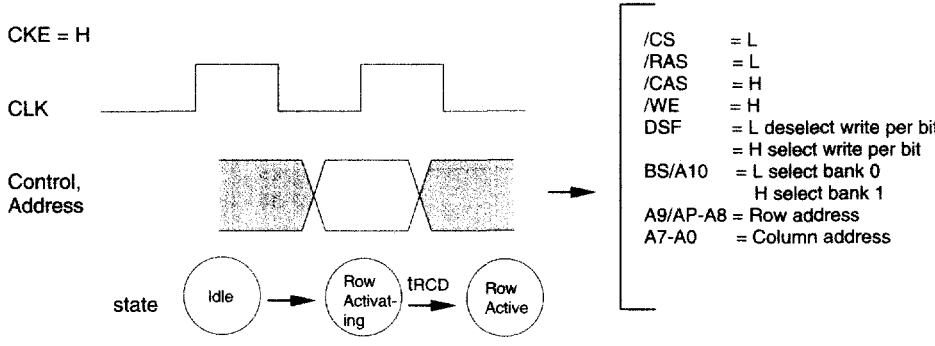


Figure 9. Row activate command to idle bank

3. Read Operation with Programmable Pipeline

3.1 Normal Read Bursts (Auto Precharge deselected)

Figure 10 shows the basic timing and control for initiating a burst read operation without Auto Precharge selected. Output of data depends on the read latency and burst length selected (See Mode Register Access, for details.). The higher the latency, the higher the operating frequency the SGRAM can run at, and the higher the peak data rate. See Figures 26 through 27 for details. Figures 26 through 27 illustrate burst writes following burst reads on the same page. The examples assume a burst length of four but burst lengths of 1, 2, 4, 8, or full page can also be used. By issuing NOPs after the initial read command, the SGRAM will continue reading data starting from the starting column address to the end of the read burst. Data will be read to the DQ outputs(assuming the corresponding DQM signals remains enabled low) until the last address in the burst has been read out. On the next clock cycle (burst length=1, 2, 4, or 8), the DQ outputs will go to hi-z and the bank will re-enter the row active state. If burst length is set to full page, the active bank does not automatically return to the row active state, even after all addresses within the burst have been read or written. The internal column address will continue to increment modulo 256 and read operation will continue.

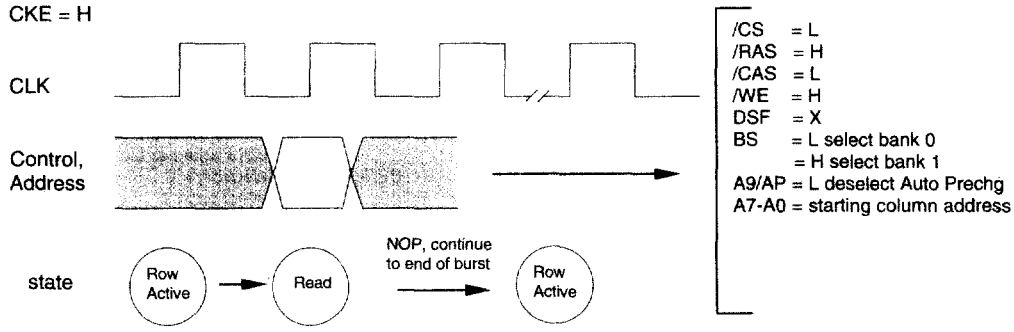


Figure 10. Burst read sequence, Auto Precharge Deselected

While in a read burst with Auto Precharge deselected, the user can issue the following command sequences.

1. Issue NOPs, continue reading data starting from the starting column address to the end of the read burst. Data will be read to the DQ outputs (assuming the corresponding DQM signals remains enabled low) until the last address in the burst, defined by the burst length and type, has been read out. On the next clock cycle, the DQ outputs will go to hi-z and the bank will re-enter the row active state.

2. Initiate another read command (with or without Auto Precharge selected) before the end of the burst and begin a new read burst starting from any column address. The burst in progress is terminated and the first address of the new burst is read to the output after a number of clock cycles defined by the $\overline{CAS}$ latency. See Figure 11 for details.

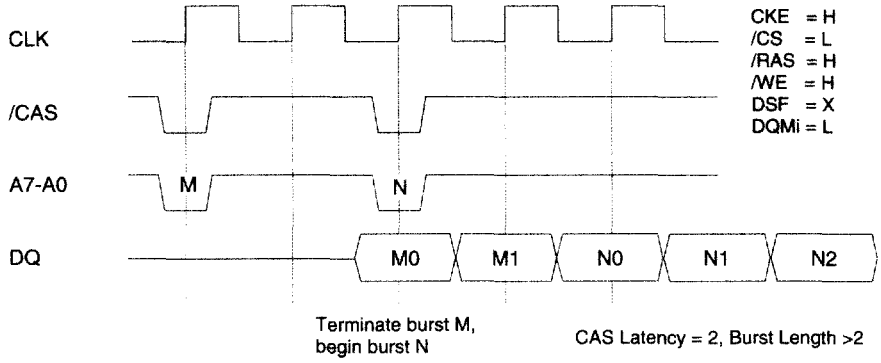


Figure 11. Timing of read initiation with read burst in progress

3. Initiate a new write burst or block write command before the end of the burst and begin a new write burst or block write starting from any column address. The burst in progress is terminated and the first address of the new write burst or block write is written. Figure 12 illustrates the timing and control for this sequence. The appropriate DQMi read/write byte enable signals must be asserted two clock cycles before the write command is issued (JEDEC specifies DQM latency is always two, regardless of the $\overline{CAS}$ latency). The DQ outputs are guaranteed to be in hi-z after a period t_{HZ} from the beginning of the clock cycle following the clock cycle in which DQMi is asserted.

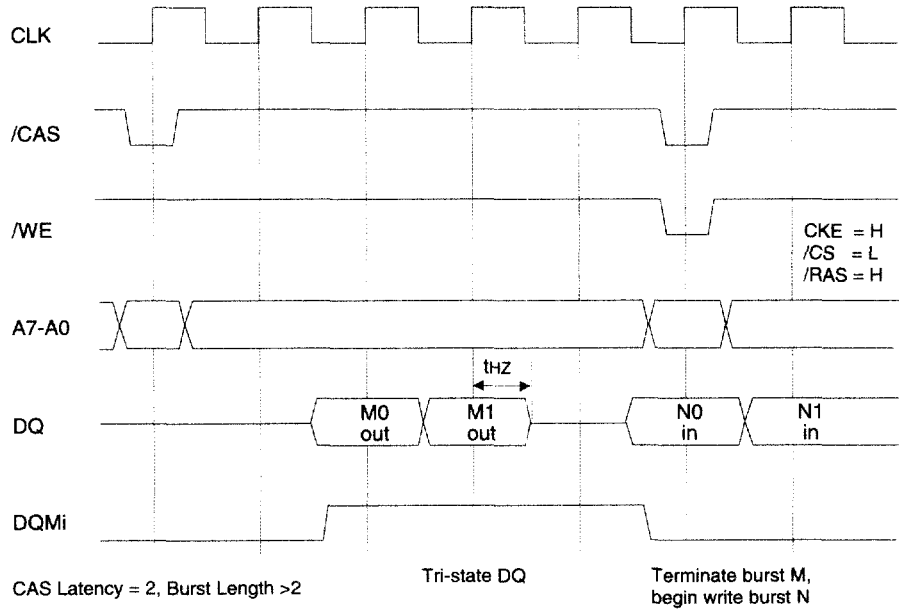


Figure 12. Timing of write initiation with read burst in progress

4. Issue a terminate burst command and return to the row active state. The timing and control for this sequence is shown in Figure 13 for the case where $\overline{CAS}$ latency is three and burst length is greater than two. Note that in this example the terminate burst command occurs on the third clock cycle after the initial read command. The terminate burst command causes the data associated with the burst counter address at the beginning of the burst terminate cycle (M2 in Figure 13) to be output to DQ after the number of clock cycles defined by the clock latency. On the next clock cycle, DQ goes to hi-z and the bank goes to the row active state.

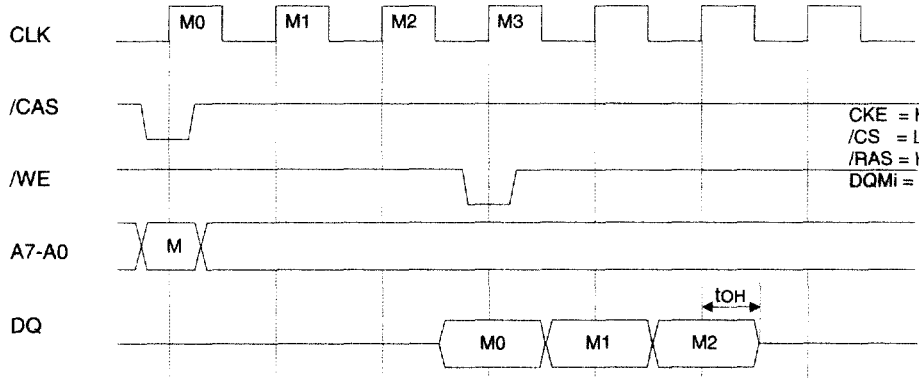


Figure 13. Timing of burst terminate command with read burst in progress

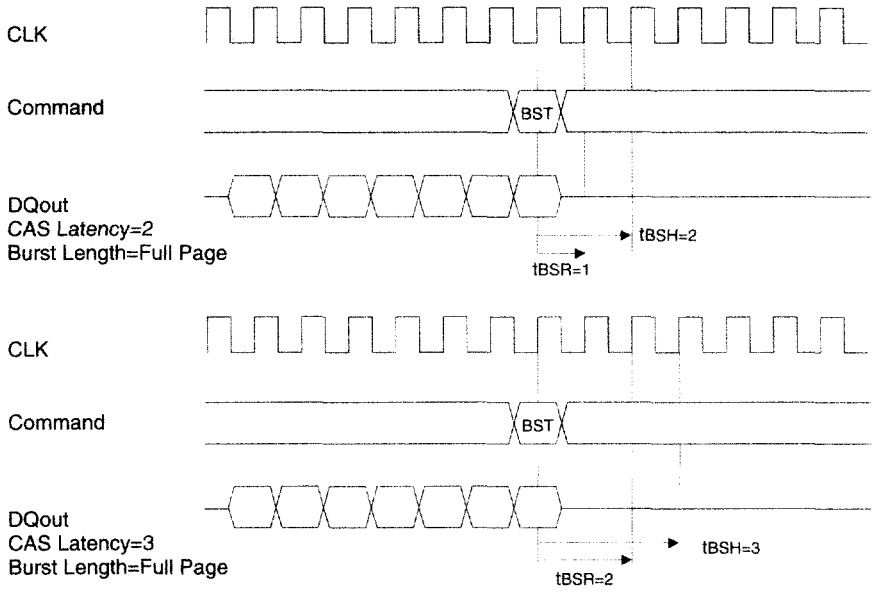


Figure 13-1. Full page burst stop

Burst stop(BST) command is used to stop data output during a full-page burst read. This command sets the output buffer to high-Z and stops the full-page burst read. The timing, from command input to the last data, depends on $\overline{CAS}$ latency. BST command is legitimate only in case full page burst mode, and is illegal in case burst length 1,2,4 and 8.

$\overline{CAS}$ Latency	BST to valid data	BST to high impedance
2	1	2
3	2	3

5. Issue a precharge command (for the selected bank or for both banks), depending on the logic level of AP/A9 terminate the burst, and return to the idle state after the precharge interval tRP. Like the terminate burst command, the last data read out is that associated with burst address during the precharge command cycle. The major difference between a precharge command and a burst terminate command is that the burst terminate command returns the bank to its row active state while the precharge command returns the bank to its idle state after the designated precharge interval. The timing and control for the precharge cycle is shown in Figure 14 for the case where $\overline{CAS}$ latency is two and burst length is greater than two.

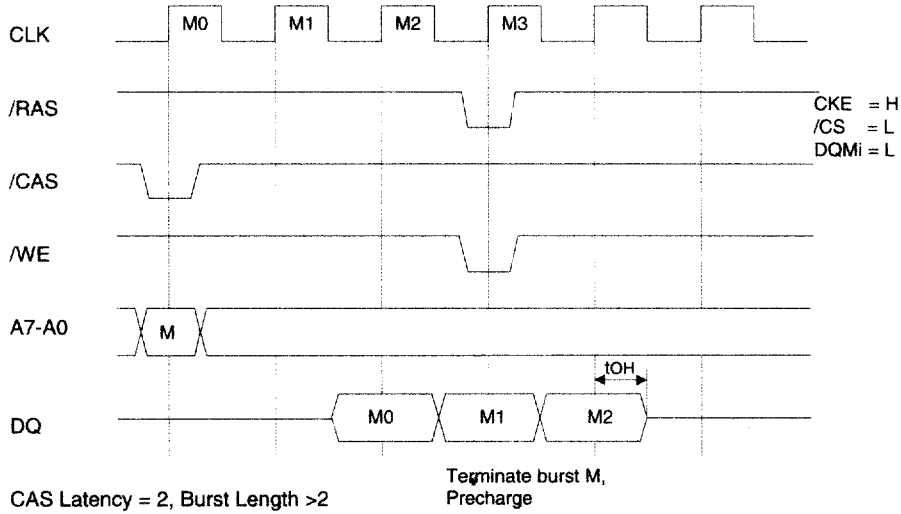


Figure 14. Timing of precharge command with read burst in progress

6. Suspend the clock. Suspending the clock can be done in accordance with the Table 3. While in the clock suspended state, the state of both banks will remain unchanged.

3.2 Read Burst with Auto Precharge Selected

Read with Auto Precharge can be selected with burst length set to 1, 2, 4, or 8 and is similar to normal read (Auto Precharge deselected) operation except that the read burst cannot be terminated by issuing another command. Once the read with Auto Precharge command is invoked within a bank, only NOP commands can be issued to that bank. At the clock cycle corresponding to the last column address in the burst the bank will enter precharge and return to the idle state after the tRP period has expired. Data will appear at the output according to the setting of the read $\overline{CAS}$ latency. Note that while a burst read with Auto Precharge selected cannot be terminated, data can be prevented from appearing at the DQ outputs by masking it off with the DQM control inputs. Figure 15 illustrates a burst read sequence with Auto Precharge selected for the case where $\overline{CAS}$ latency is two and burst length is two.

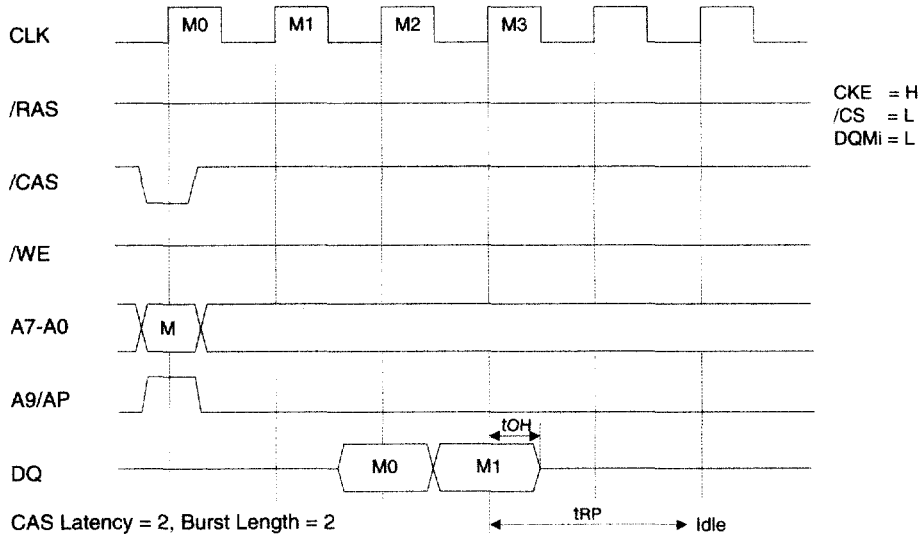
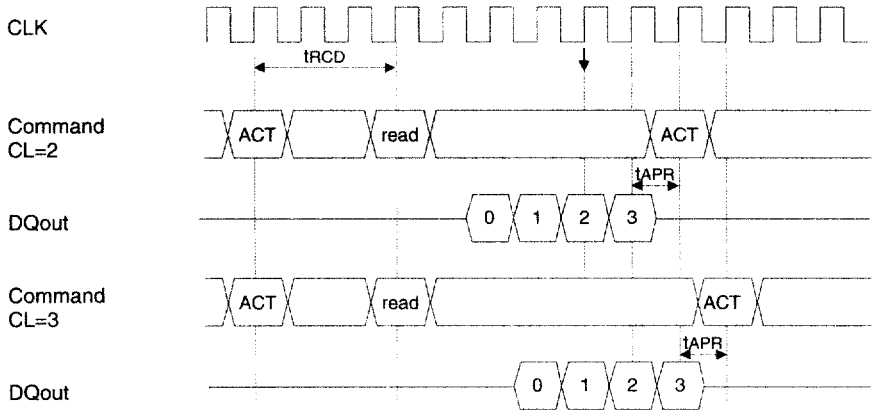


Figure 15. Read burst with Auto Precharge selected



Note. Internal Auto-precharge starts at the timing indicated by `` ↓ ``

Figure 15-1. Burst read with auto precharge followed by an active command

In this operation, since precharge is automatically performed after completion a read operation, so no precharge commands are necessary after each read operation. The command next to this command must be a bank active(ACTV, ACTVM) command. In addition, see Figure 15-1, an interval defined by t_{APR} is required before execution of the next command.

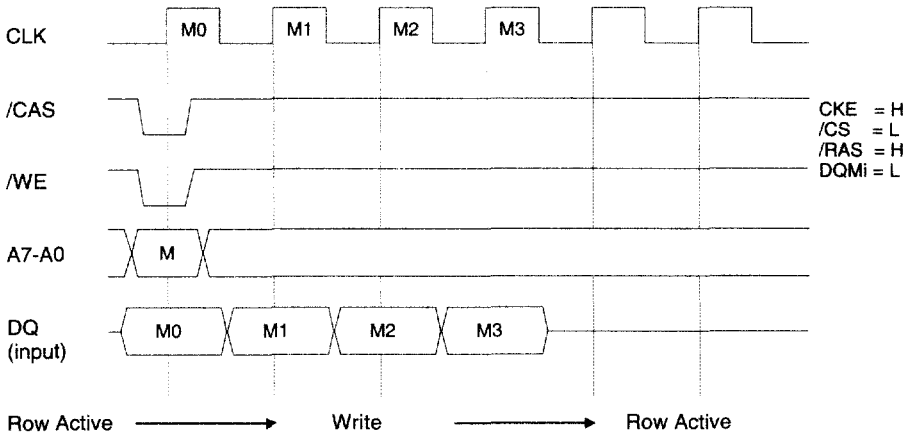
$\overline{CAS}$ latency	Precharge start cycle
3	2 cycle before the last data out
2	1 cycle before the last data out

4. Write Operation

There are several variations of write operation to the two banks of DRAM. Write bursts can be initiated to either bank with and without Auto Precharge selected. Also, write per bit and block write operations can be invoked. The basic write operation showing the relationship to the programmed $\overline{CAS}$ latency and burst length will be described first, and the variations for Auto Precharge, write per bit. and block write will be described subsequently. It is important to note that Auto Precharge, write per bit, and block write are orthogonal variations to the basic write operation. That is, each of them can be invoked independently of the others.

4.1 Write Operation with Auto precharge Deselected

The latency for write operation is defined as the clock cycle difference between the clock where write command and column address are asserted and the clock cycle where the first data to be written is presented and is always equal to zero. That is the data for a write operation is presented on the same clock cycle as the corresponding address, regardless of what value of $\overline{CAS}$ latency is programmed into the mode register. Figure 16 shows this relationship.

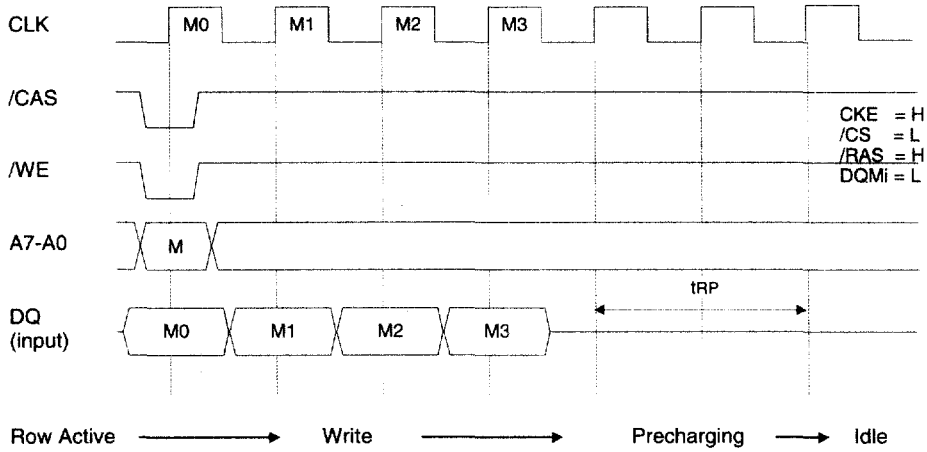


CAS Latency = 2, 3; Burst Length = 4

Figure 16. Write burst with Auto Precharge deselected.

4.2 Write Operation with Auto Precharge

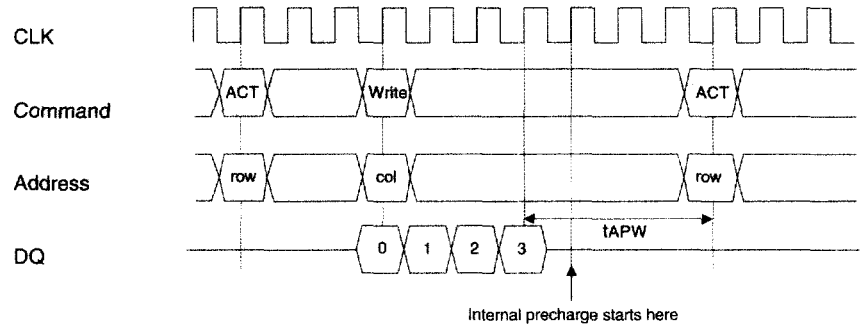
Write operation with Auto Precharge can be selected with burst length set to 1, 2, 4, or 8 and is similar to write operation without Auto Precharge except that once initiated the write burst cannot be terminated by another command. To complete the burst, NOPs must be executed and data input supplied for each address in the burst until the end of the burst has been reached. Alternatively, the DQM control inputs can be asserted to prevent writes from occurring during the burst sequence. On the clock cycle following the last address in the burst, the bank will begin precharging and will re-enter the idle state after the precharge period, tRP. Figure 17 illustrates the sequence.



CAS Latency = 2, 3; Burst Length = 4

Figure 17. Write burst Auto Precharge selected

Burst Write (Burst Length=4)



Single Write

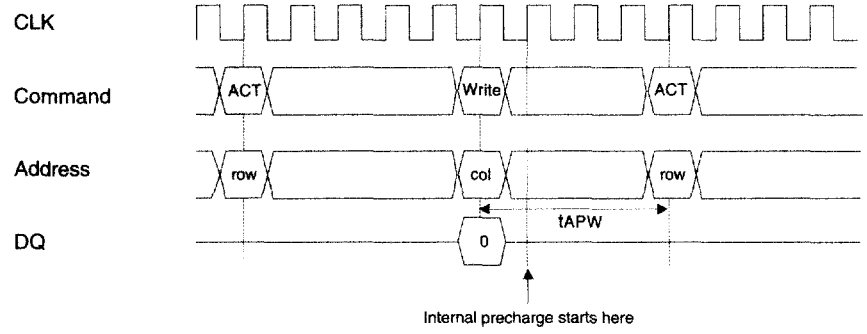


Figure 17-1. Write burst with Auto Precharge followed by an active command

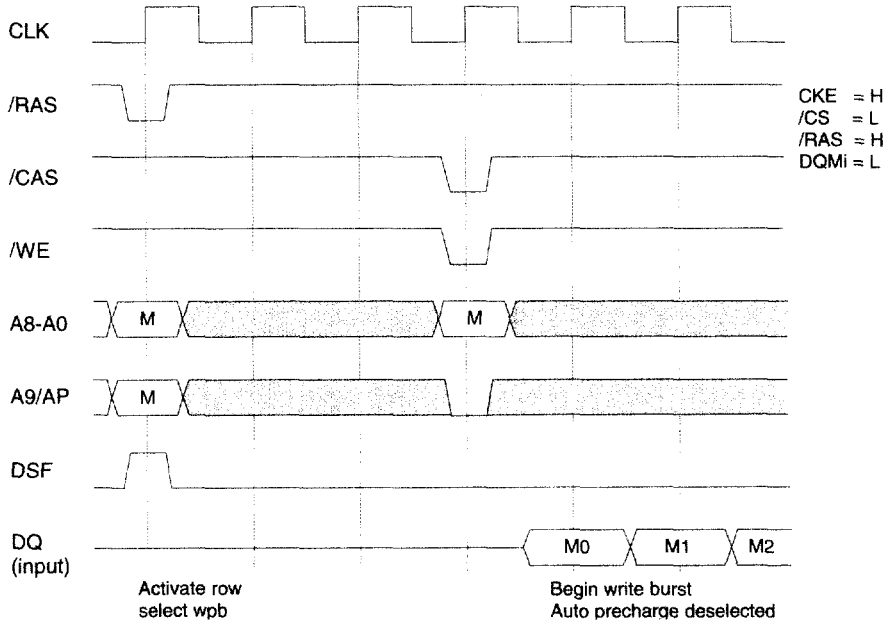
Write with Auto Precharge

In this operation, since precharge is automatically performed after completion of a burst write or a single write operation, so no precharge commands are necessary after the write operation. The command next to this command must be a bank active command(ACTV, ACTVM). In addition, an interval of tAPW is required between the last valid data input and the next command.

4.3 Write Operation with Write Per Bit

The SGRAM features a write per bit capability similar in functions to previous generation Video RAMs. Write per bit allows the write to each of the 32 DQs to be controlled individually by employing a 32 bit write per bit mask(or write mask) register which can be dynamically loaded via a Special Register Access cycle. The 32 bits in the write mask register have a one to one correspondence with the 32 DQs. A logic level 1 in bit position i in the mask register enables a write to DQi during write per bit write cycles. A logic level 0 in bit position i masks off, or disables, the write to DQi during write per bit write cycles.

To invoke write per bit write cycles, the write per bit function must be selected when activating a row / bank. So long as that bank remains active, all subsequent write cycles to that row / bank will use the write mask to control which DQs get written with the input data present on the DQ pins during the write cycles. Figure 18 illustrates write per bit operation. The figure shows that Auto Precharge is deselected although Auto Precharge can be selected in exactly the same way as in other write operations previously discussed.



CAS Latency = 2, 3; Burst Length >2

Figure 18. Write burst with Write Per Bit, Auto Precharge deselected

5. Block Write Operation

5.1 Block Write with auto precharge deselected

The SGRAM features a block write function similar to that of previous generation Video RAMs. Block write allows as many as eight times the number of bits to be written in a single cycle compared to standard write operations previously described. A 32 bit on chip color register can be loaded via a special register cycle. Once loaded, the color register acts as a data source for subsequent block write operations. The DQ pins then act as address pointers and are collectively known as an ``address mask``, replacing the three least significant column address bits, A2-A0. Each byte has its own independent address mask. DQ31-DQ24, DQ23-DQ16, DQ15-DQ8, and DQ7-DQ0 serve as address masks for bytes 3, 2, 1, and 0 respectively.
Considering byte 0, for example, DQ7-DQ0 act as individual address pointers to the eight column addresses represented by the eight binary combinations of A2-A0. Rather than using A2-A0 to select one address out of the possible eight to be written with the contents of the color register, the eight DQ7-DQ0 lines allow write selectability to each of the eight addresses represented by the eight combinations of A2-A0. A logic high level on DQi causes the appropriate address in memory to be written with the contents of the color register while a logic low level on DQi inhibits the appropriate address from being written. In essence, any subset of the eight column addresses(for each byte) can be written in a single block write cycle. Considering all four bytes represented by DQ31-DQ0, as many as 256 bits(8 bits x 8 column addresses x 4 bytes) can be written with the contents of the color register in every block write cycle. Figure 19 shows the write data and control for block write operation to all four bytes of the SGRAM.

Block write can be combined with write per bit and byte write (via the DQM pins) control to achieve full byte and bit mask-ability for the 256 bits selected during block write cycles. In other words, any subset of 256 bits can be written during every block write cycle. Furthermore, block write cycles can be intermixed with read cycles and non block write cycles while a bank / row is selected, however the block write command period t_{BWC} must be observed. For high frequency operation, this could result in one additional clock cycle at the end of a sequence of block write cycles. Since block write can conditionally write to eight adjacent column address locations at once, there is no provision for performing burst block writes by invoking a block write cycle followed by NOPs. In other words, each time a block write operation is desired, a block write command including the block address A7-A3 must be invoked. Figure 20 shows the timing and control for block write. In this example, write per bit operations is selected during the row activation cycle. During the subsequent block write and write cycles, the write per bit mask register will serve as a plane mask to the 32 planes, or I/Os of the SGRAM. During the block write cycles, the DQ pins serve as address mask bits while the color register serves as the input data source. Block write commands are not burstable. For each block write operation, a new block write command must be issued.

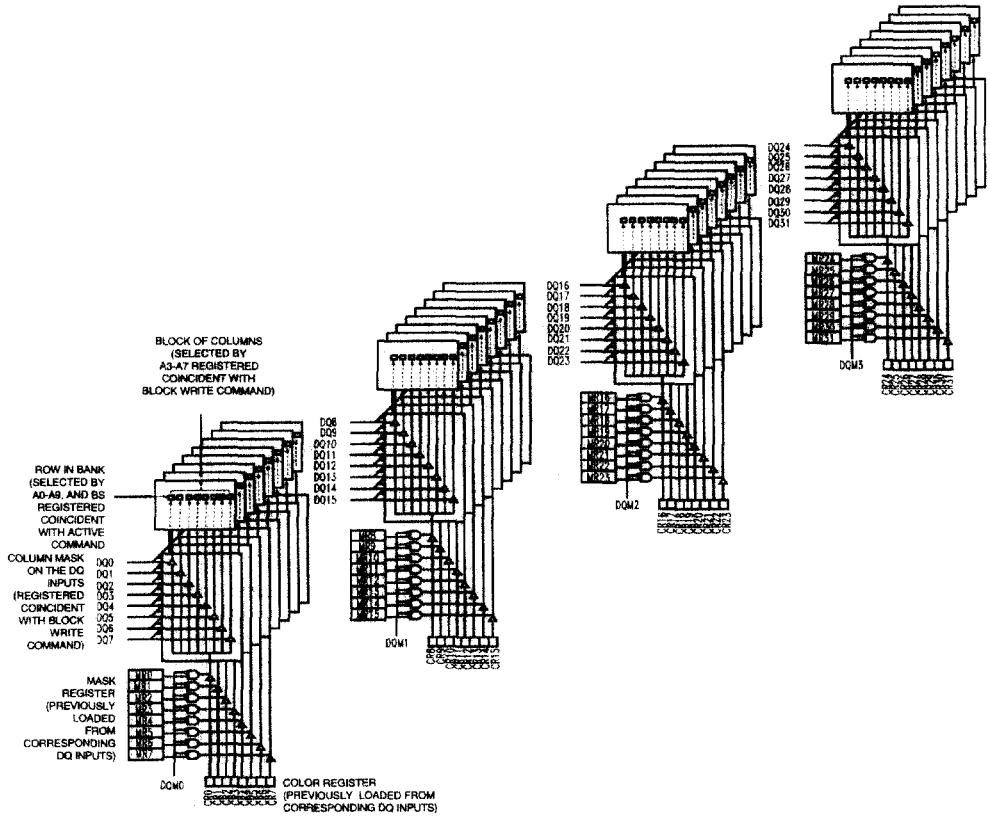
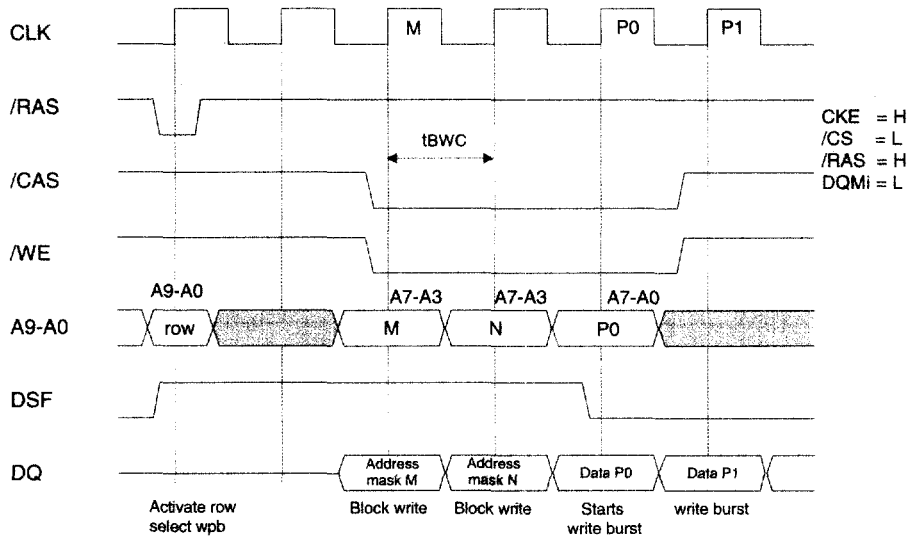


Figure 19. Diagram of block write operation



Burst Length >2

Note : At high speed CLK rate additional CLK is required to satisfy tBWC timing

Figure 20. Timing and control for block write cycles

Special mode register set in active state and block write

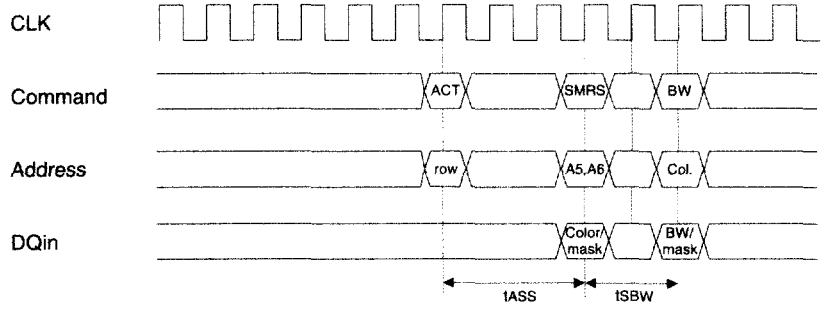


Figure 20-1. Special mode register set in active state and block write

Special mode register are set through address pins during IDLE, ACTV or ACTVM state. A5 and A6 pins are used to determine whether loading color data or mask data. Other pins should be low. Color data and mask data are loaded through DQ pins into the color register respectively. When special mode register set command is issued, if both A5 and A6 are equal to 1, then neither color nor mask data is assured. See ``1.2 Special Mode Operations``.

5.2 Block write with auto-precharge

In this operation, since precharge is automatically performed after completion of a block write operation, so no need to execute precharge command. The command next to this command must be a bank active command(ACTV, ACTVM). In addition, an interval of tAPBW is required between the last valid and the next command.
See ``special mode register operation (1. 2) ``

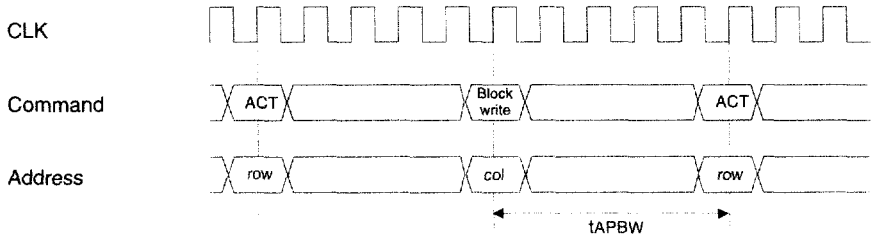


Figure 21. Timing of Block Write with auto precharge selected

6. Refresh Operation

Since the SGRAM is a dynamic memory device, the stored data must be refreshed periodically or it will be lost. To avoid data loss, all rows in both banks must be accessed during the maximum refresh interval specified by tREF. A row of data in either bank of RAM is refreshed whenever that row is activated. For example, activating a row for the purpose of reading or writing addresses along that row causes the data in that row to be refreshed. In addition to normal read and write operation, the SGRAM has two modes of refreshing the banks of memory: Auto Refresh and Self Refresh.

6.1 Auto Refresh

Auto Refresh is similar to $\overline{CAS}$ before $\overline{RAS}$ refresh found on previous generation asynchronous DRAMs. One Auto Refresh cycle refreshes one row of memory using a 11 bit, on chip refresh counter as the row address and bank select. The refresh counter is incremented during each Auto Refresh cycle. The upper 10 bits of the counter supply the address of one of the 1024 rows in each bank to be refreshed and the least significant bit selects the bank in which the refresh will occur. Thus, successive Auto Refresh cycles alternate between the two banks. Because Auto Refresh operation alternates between banks, both banks must be idle when Auto Refresh commands are invoked. Figure 22 shows two successive Auto Refresh cycles. Once an Auto Refresh cycle has been invoked, it is controlled internally until its duration. NOP cycles must be inserted during the entire Auto Refresh cycle time defined by tRC.

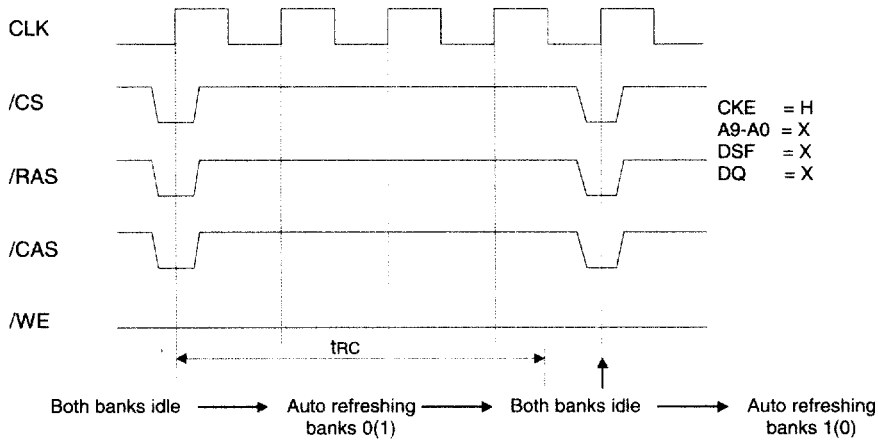


Figure 22. Timing and control for Auto Refresh Operation

6.2 Self Refresh

The SGRAM features an on chip refresh cycle timing generator which can be used in conjunction with the row refresh counter to refresh the two banks of DRAM entirely under internal control. Self Refresh can be invoked only when both banks are idle. While the device is in Self Refresh mode, CKE is the only enabled input to the device. All other inputs, including the clock are disabled and any input is ignored. Self Refresh mode is entered by invoking an Auto Refresh command with CKE low. Once this command is invoked, the cycle timing generator performs a burst refresh, sequencing through all 2048 rows(1024 rows in each bank, alternating each refresh cycle between banks) with a per row refresh cycle time of approximately 1 microsecond. To conserve power, once the burst refresh has been completed to all 2048 rows the cycle timing generator automatically slows down to a per row refresh period of approximately 32 microseconds and refresh operation continues until Self Refresh mode is exited.

Important: Upon exiting Self Refresh mode, the time elapsed since the least recently refreshed row was refreshed can vary from a few milliseconds to 32 milliseconds. It is thus imperative that the least recently refreshed row be refreshed immediately and that the most recently refreshed row be refreshed within the specified maximum refresh period. One way for the user to ensure this is to perform a burst of 2048 Auto Refresh commands immediately after exiting Self Refresh mode. This is especially critical for those systems employing burst refresh. For systems employing distributed refresh, a single Auto Refresh operation should be performed immediately. Since Self Refresh and Auto Refresh operations use the same internal row address counter, the first row to be refreshed by the Auto Refresh cycle will be the row least recently refreshed when Self Refresh was exited. From then on, distributed refresh should guarantee that the row most recently refreshed when Self Refresh was exited is refreshed within the specified maximum refresh interval. Self refresh mode is exited by starting the clock(if the clock had been stopped) and then asserting CKE after the clock waveform has stabilized. The low-to-high transition of CKE will re-enable the clock and other inputs asynchronously. A minimum time, specified by tSREX, must be satisfied before any command other than Exit Self Refresh is invoked. Figure 23 shows how Self Refresh mode is entered and exited. See Table 3 for more information.

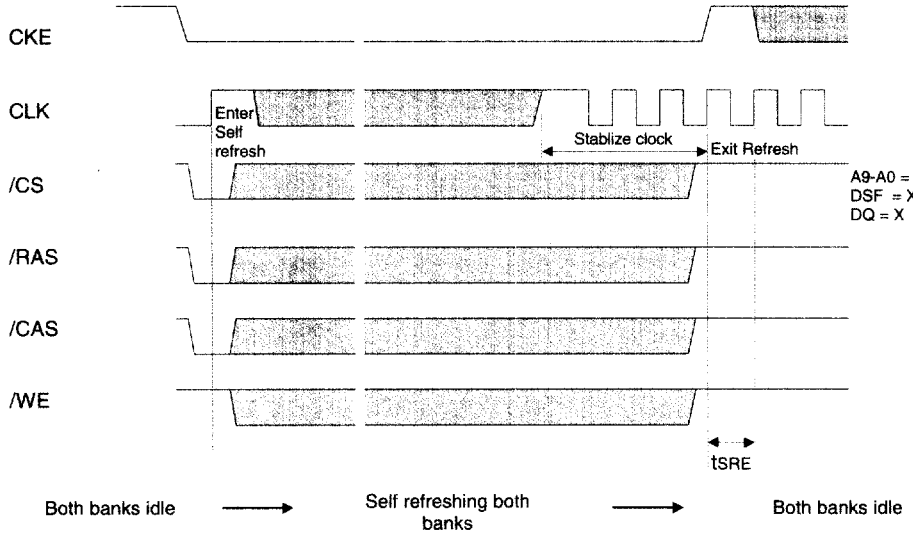


Figure 23. Timing and control for Self Refresh Operation

7. Power Down

The SGRAM has two internal clock buffers. A low current capacity clock buffer feeds the CKE input buffer while a high current clock buffer feeds the state machine and all DRAM circuits. During the Power Down state, the large clock buffer is disabled but the small clock buffer is not. In contrast to the Self Refresh state, entering and exiting Power Down is completely synchronous with respect to CKE. That is, CKE is sampled on every clock cycle, rather than asynchronously changing the state of the SGRAM. Power Down is the lowest power state available. During Power Down, the SGRAM is not refreshed. Therefore, the minimum refresh interval specification must be observed during power down or else data will be lost. Figure 24 shows an example of the timing and control for entering and exiting Power Down. Exiting Power Down requires one clock cycle, as shown in the figure, other commands can be issued on the clock cycle following the Exit Power Down command cycle.

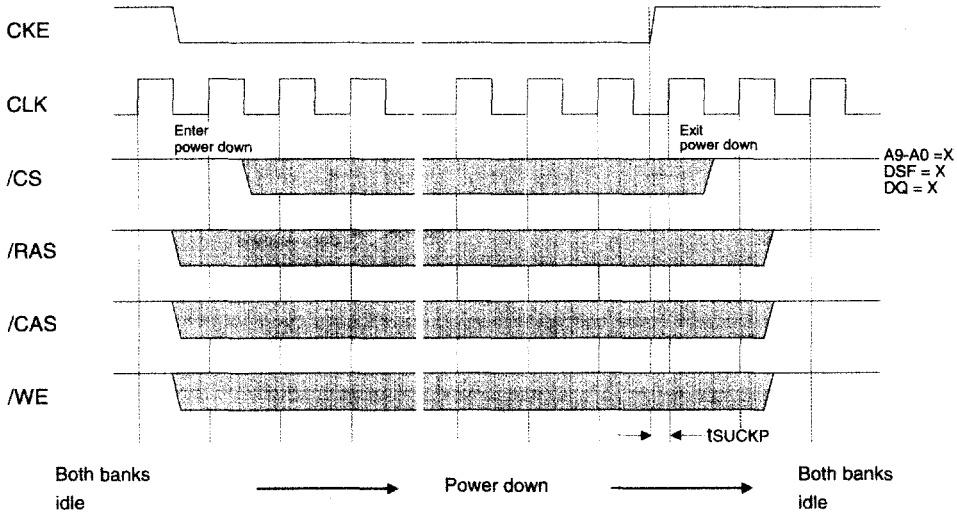


Figure 24. Example timing and control for Power down operation

8. Clock Suspend

Clock Suspend is very similar to Power Down, except that the Clock Suspend command is invoked by sampling the CKE signal low while one or both banks are not idle. While the clock is suspended, only the CLK input to the small CLK buffer and the CKE input are enabled, and the state of CKE is sampled on every clock cycle. Internally, the banks remain in the state they were in when the clock was suspended. For example, if bank 0 was in the middle of a read burst when the clock suspend command was invoked, the read state will be maintained while the clock is suspended and the internal burst address counter will not increased. The final read before clock suspension will be initiated at the clock cycle in which the clock suspend command was invoked. All subsequent clock cycles leading up to the exit clock suspension command will be ignored. On the clock cycle following the cycle in which the exit clock suspend command is invoked, the burst can be resumed from the next memory location designated by the burst length programmed in the Mode Register, or other legal commands can be issued to the active or both banks. While the clock is suspended, the SGRAM is not refreshed. Therefore, the minimum refresh interval specification must be observed to prevent loss of data. Figure 25 illustrates how Clock Suspend is entered and exited. See Table 3 for more information.

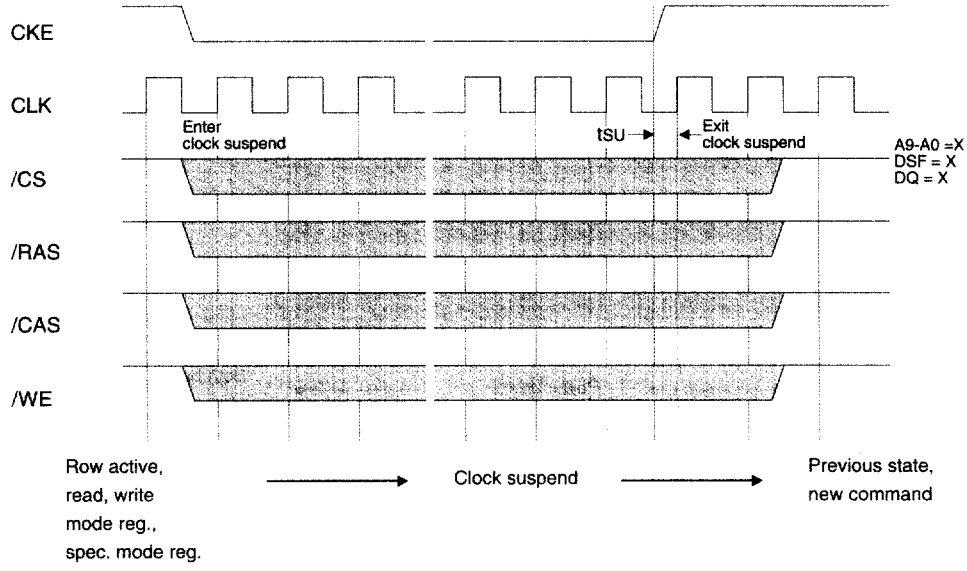


Figure 25. Example timing and control for Clock suspend operation

9. DQM control

The DQMi (i=0,1,2,3) controls the ith byte of DQ data. DQM control operation for read and for write are different in terms of operation timing.

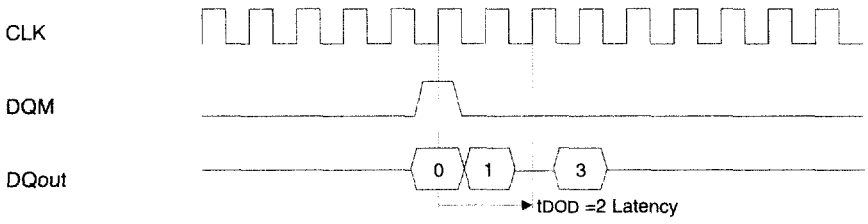
Reading

When data is read, output buffer can be controlled by DQMi.
By setting DQMi to low, the corresponding DQ output buffers become active.
By setting DQMi to high, the corresponding DQ output buffers are made floated so that the ith byte of data are driven out. The latency of DQM operation for read operation is 2.

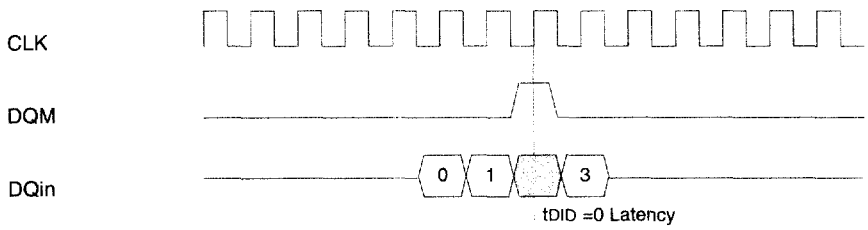
Writing

Input data can be controlled by DQMi.
While DQMi is low, data is driven into the HY5816321.
By setting DQMi to low, the corresponding ith byte of DQ input data are kept from being written to the HY5816321 and previous data are protected. The latency of DQM for write operation is 0.

Reading



Writing



10. Power - on sequence

During power - on sequence, DQM0, DQM1, DQM2, DQM3 and CKE must be set to high. When 200μs has past after power-on, all banks must be precharged using precharge command. After t_{RP} delay, set the mode register. And after t_{RSA} delay, execute two auto - refresh commands as dummy, an interval of t_{RC} is necessary between two auto - refresh commands.

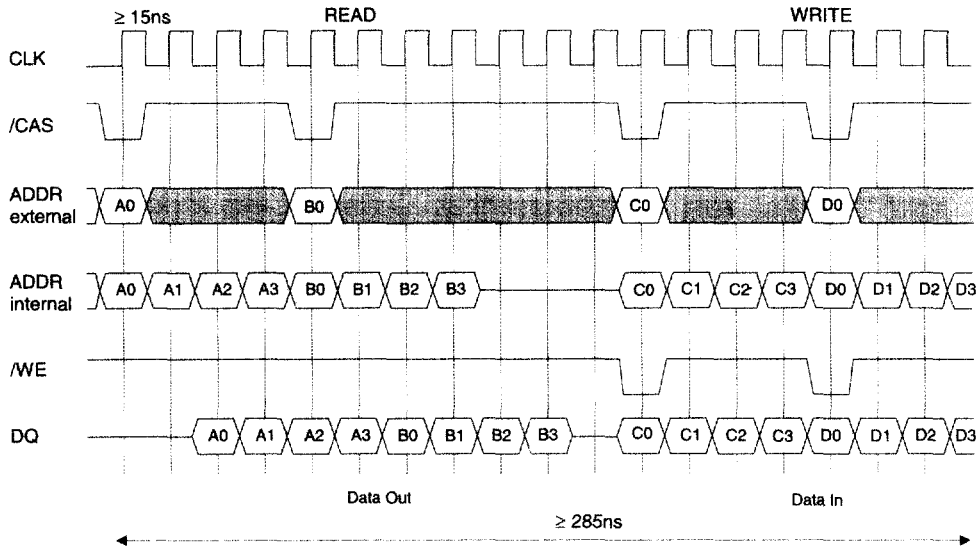


Figure 26. Timing of pipeline operation, latency = 2, burst length = 4

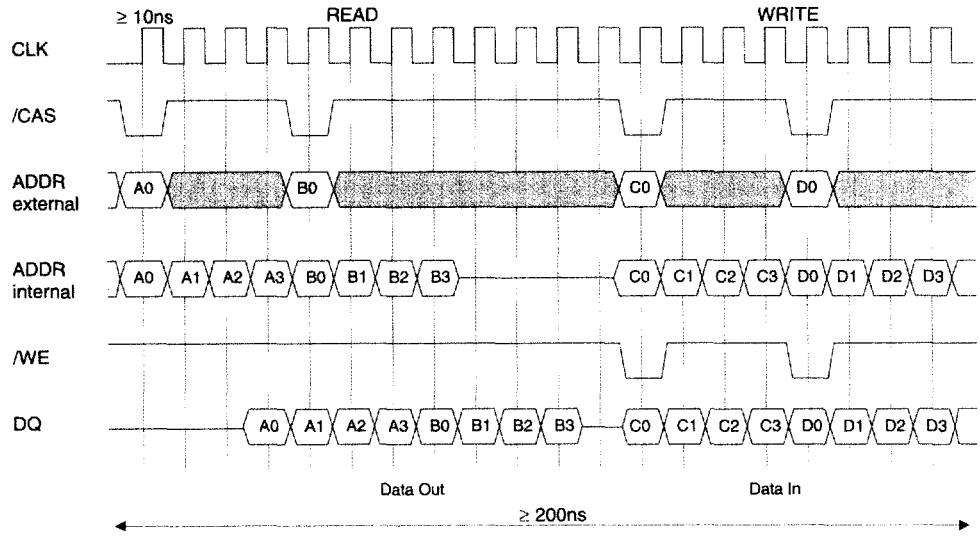


Figure 27. Timing of pipeline operation, latency = 3, burst length = 4

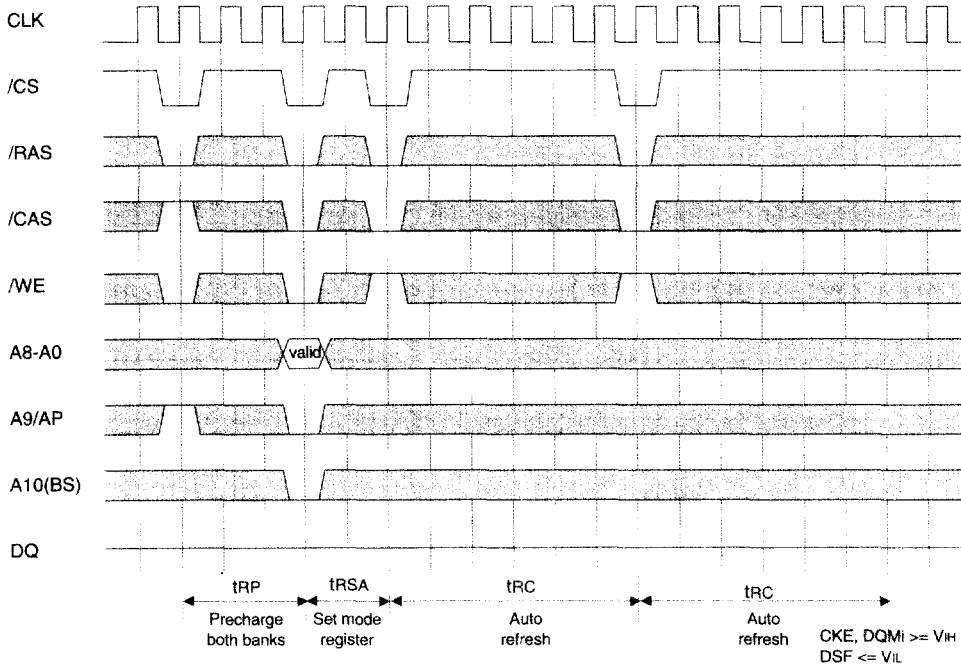
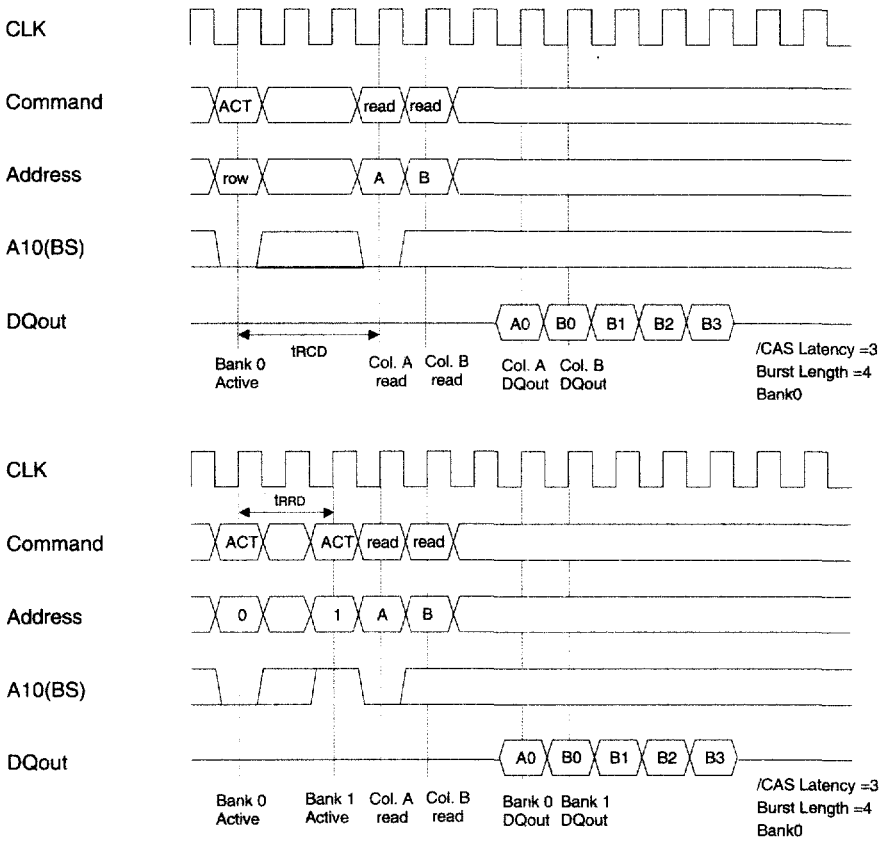


Figure 28. Power - On Sequence (using $\overline{CS}$ = Has chip deselect)

Command Intervals



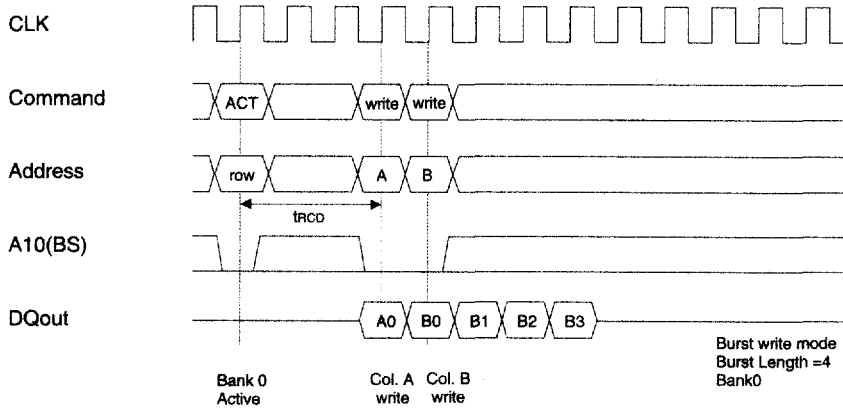
- Read command to read command interval

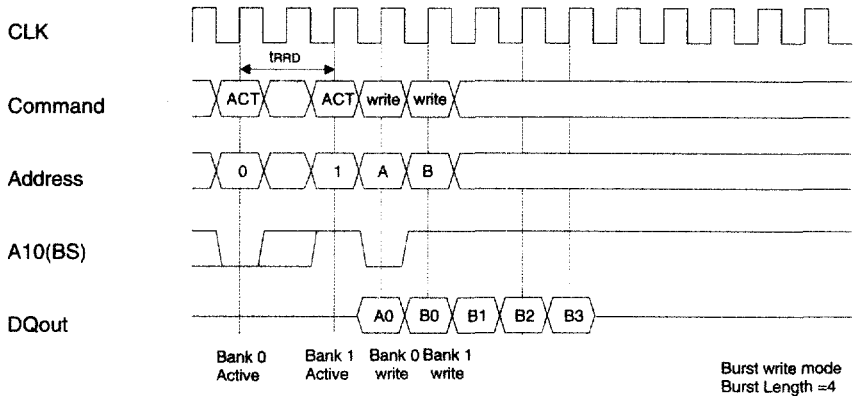
1. Operation for column in the same row (page): Within the same row (page), read command can be issued every cycle.
   Note that the last read command has the priority to the preceding read command, that is, any read command can interrupt the preceding burst read operation to get valid data aimed by this interruption.

2. Operation for column in other row of the same bank: To read data of other row of the same bank, it is necessary to execute a precharge command and a bank active command before executing the next read command.

3. Operation for another bank: For another bank in active state, burst read command can be executed in the next cycle after the preceding read command is issued. If another bank is in idle state, a bank active command should be executed before executing a read command.

Command Intervals(cont.)





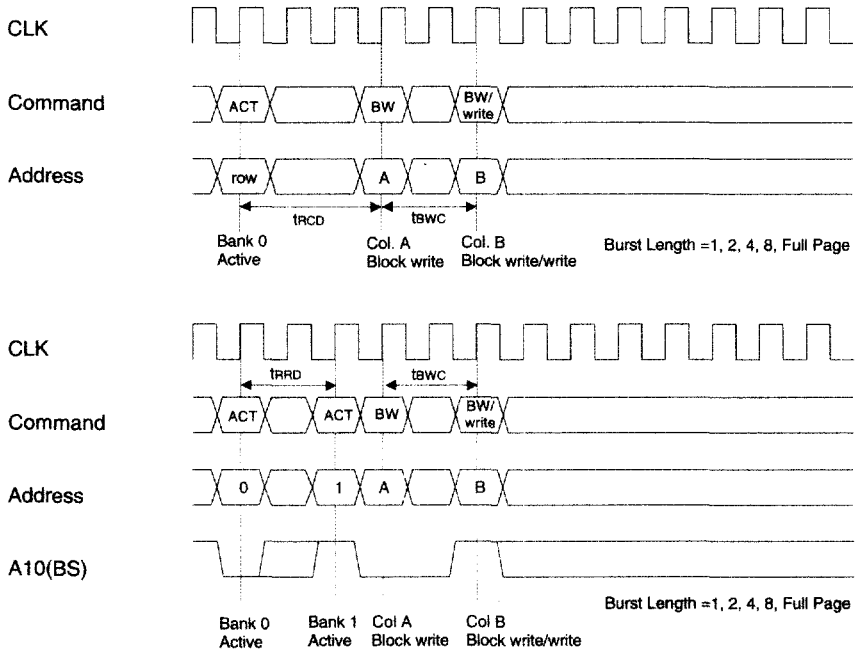
- Write command to write command interval

1. Operation for column in the same row (page): Within the same row (page), write command can be issued every cycle.
   Note that the last write command has the priority to the preceding write command, that is, any write command can interrupt the preceding burst write operation to get valid data.

2. Operation for column in other row of the same bank: To write data of other row of the same bank, it is necessary to execute a precharge command and a bank active command before executing the next write command.

3. Operation for another bank: For another bank in active state, burst write command can be executed in the next cycle after the preceding write command is issued. If another bank is in idle state, a bank active command should be executed.

Command Intervals(cont.)



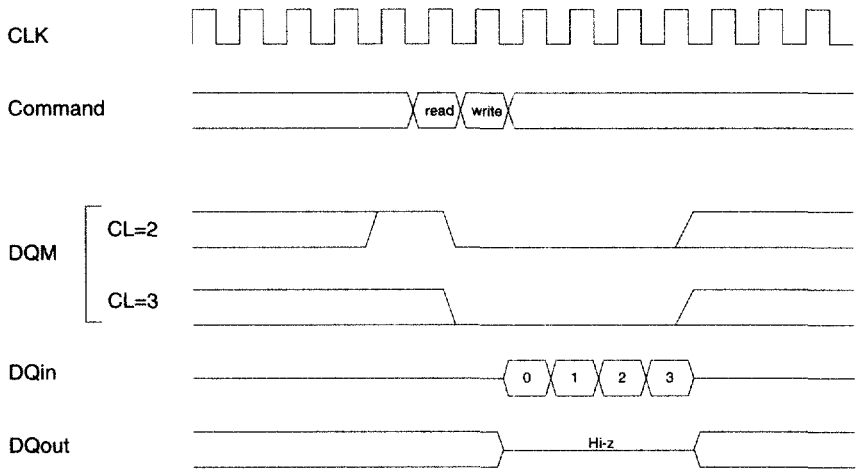
- Block Write command to write or block write command interval

1. Operation for column in the same row (page): Within the same row (page). It is necessary to take no less than tBWC between a block write and another block write/normal write. If tCK is less than tBWC, NOP command should be issued for the cycle between block write command and the following write or block write command.

2. Operation for column in other row of the same bank: To execute write command or another block write command for other row of the same bank, it is necessary to execute a precharge command and a bank active command before write or block write operation.

3. Operation for another bank: To execute write command or another block write command for another bank in active state, tBWC interval to the next command is necessary. If another bank is in idle state, a bank active command should be executed. If tCK is less than tBWC, NOP command should be issued for the cycle between a block write command and the following write or block write command.

Command Intervals(cont.)



- Read command to write or block write command interval

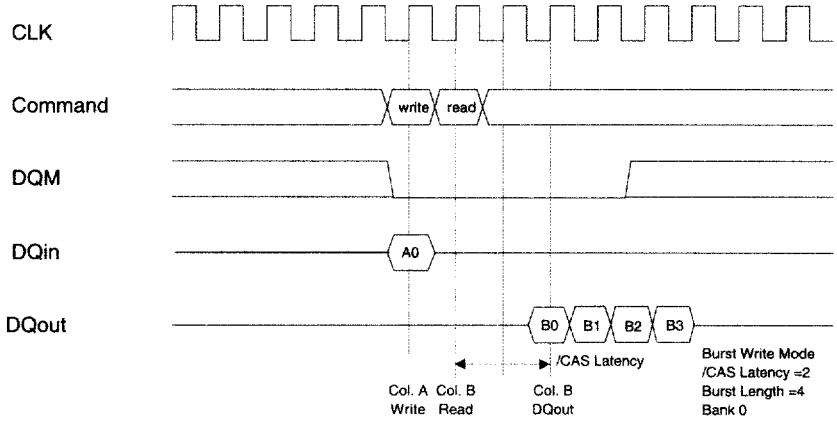
1. Operation for column in the same row : Write or block write command following the preceding read command can be performed after an interval of no less than 1 cycle. To set DQ output High - z when data are driven in, DQM must be used depending on /CAS latency as the timing shown above. Note that the last write or block write command has the priority to the preceding read command, that is, any write or block write command can interrupt the preceding burst read operation to get valid data.

2. Operation for column in other row of the same bank: To execute write or block write command for other row of the same bank, it is necessary to execute a precharge command and a bank active command before executing these commands.

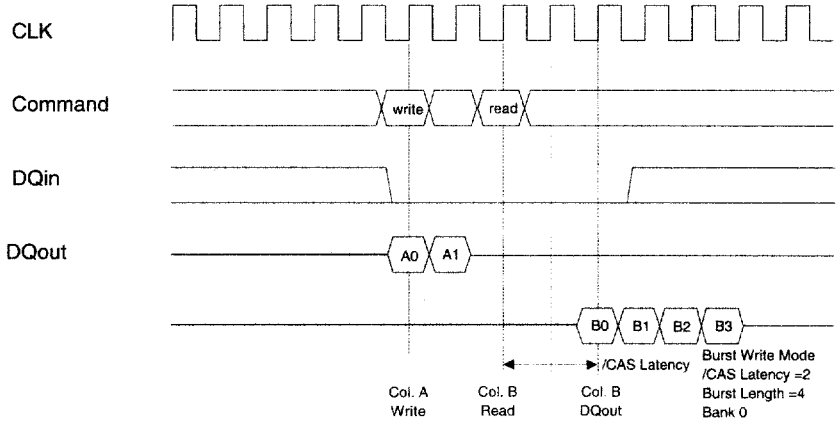
3. Operation for another bank: For another bank in active state, burst write command can be executed from the next cycle after the preceding write command is issued. If another bank is in the idle state, a bank active command should be executed.

Command Intervals(cont.)

Write to READ Command Intervals(1)



Write to READ Command Intervals(2)



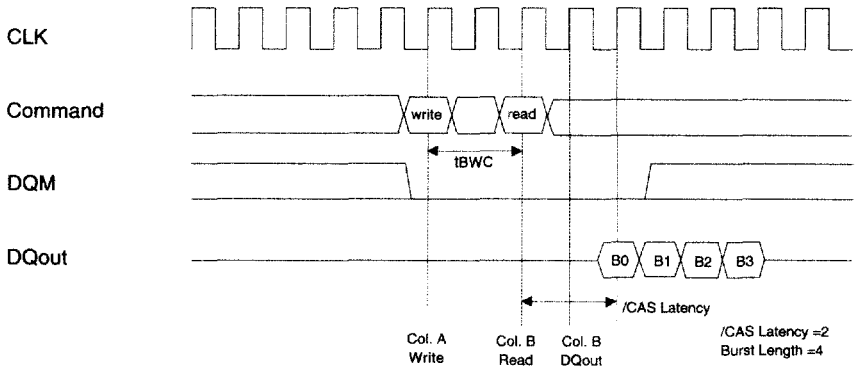
- Write command to read command interval

1. Operation for column in the same row : Read command following the preceding write command can be performed after an interval of no less than 1 cycle.
   Note that the last read command has the priority to the preceding write command, that is, any read command can interrupt the preceding burst write operation to get valid data.

2. Operation for column in other row of the same bank: To execute read command for other row of the same bank, it is necessary to execute a precharge command and a bank active command .

3. Operation for another bank: For another bank in active state, burst read command can be executed from the next cycle after the preceding write command is issued. If another bank is in the idle state, a bank active command should be executed prior to execute the following read command.

Command Intervals(cont.)



- Block Write command to read command interval

1. Operation for column in the same row (page): Within the same row (page). It is necessary to take no less than t_{BWC} between a block write and the following read command. If t_{CK} is less than t_{BWC}, NOP command should be issued for the cycle between block write command and the following read command.

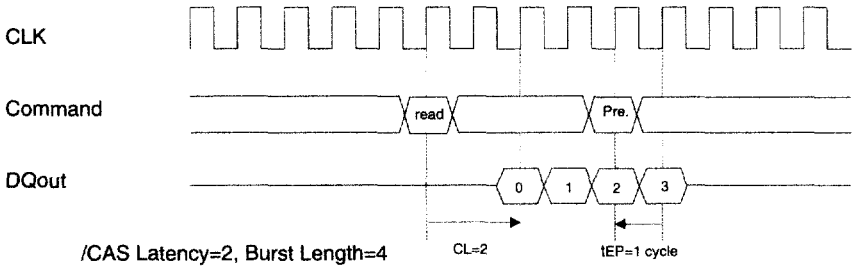
2. Operation for column in other row of the same bank: To execute red command for other row of the same bank, it is necessary to execute a precharge command and a bank active command before write or block write operation.

3. Operation for another bank: To execute read command for another bank in active state, t_{BWC} interval to the next command is necessary. If another bank is in idle state, a bank active command should be executed. If t_{CK} is less than t_{BWC}, NOP command should be issued for the cycle between a block write command and the following read command.

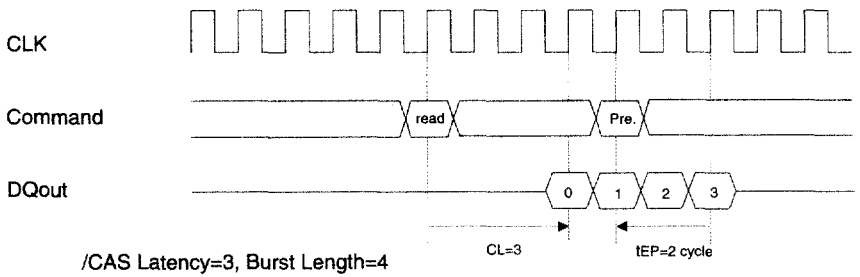
Command Intervals(cont.)

- Read command to precharge command interval

  The minimum interval between read command and precharge command is 1 cycle. However, since the output buffer then becomes High - Z after the cycles defined by tHZP, there is a possibility that burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the cycles defined by tEP must be assured as an interval from the final data output to precharge command execution.



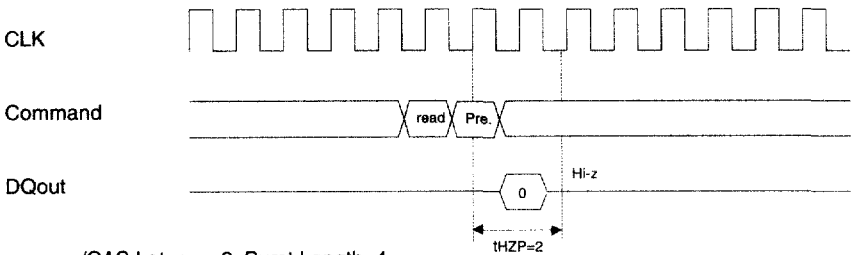
/CAS Latency=2, Burst Length=4



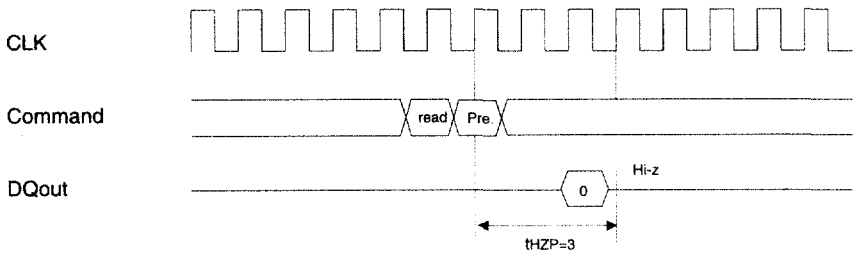
/CAS Latency=3, Burst Length=4

- Read command to precharge command interval(same bank): Output all data.

Command Intervals(cont.)



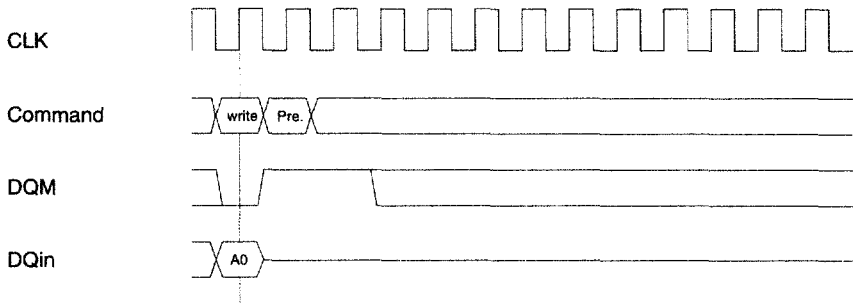
/CAS Latency=2, Burst Length=4

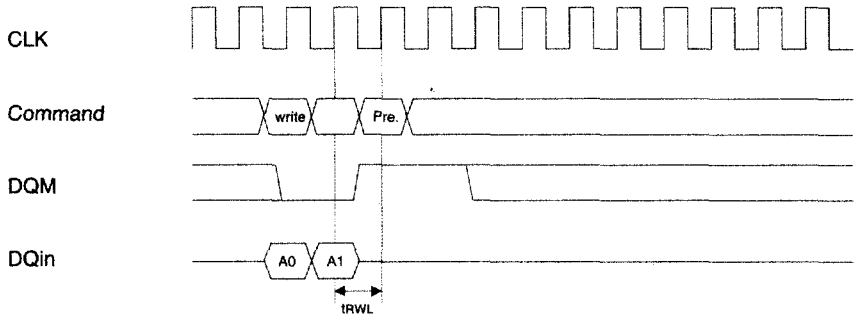


/CAS Latency=3, Burst Length=4

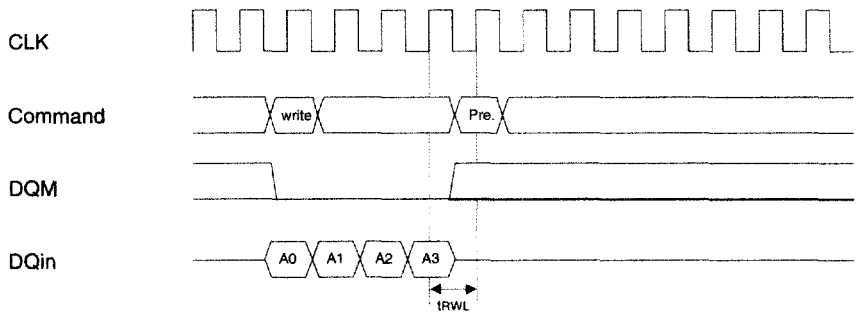
- Read to precharge command interval(same bank): To stop output data.

Command Intervals(cont.)





Burst Length =4(To stop write operation)



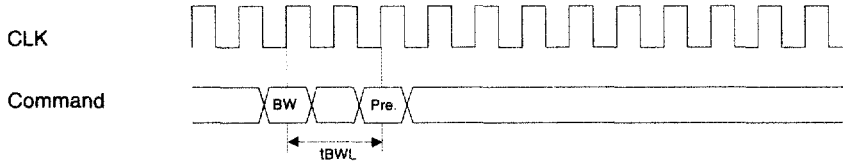
Burst Length =4(To write all data)

- Write command to precharge command
  The minimum interval between write command and the following precharge command. However, if the burst write operation is not finished, input must be masked by means of DQM for assurance of the cycle defined by tRWL.

Command Intervals(cont.)

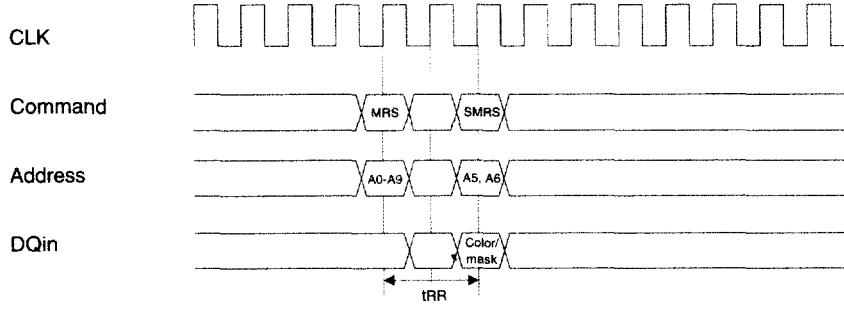
- Block Write command to precharge command interval

  The minimum interval between block write command and the following precharge command is tBWL.



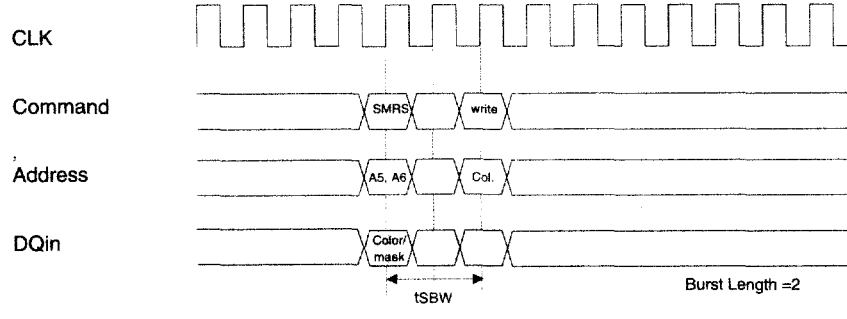
- Block Write to precharge command interval (same bank)
- Register set to register set interval

The minimum interval between two register sets(mode/special mode) is tRR.



- Mode register set to special mode register interval
- Special mode register set to block write /write interval

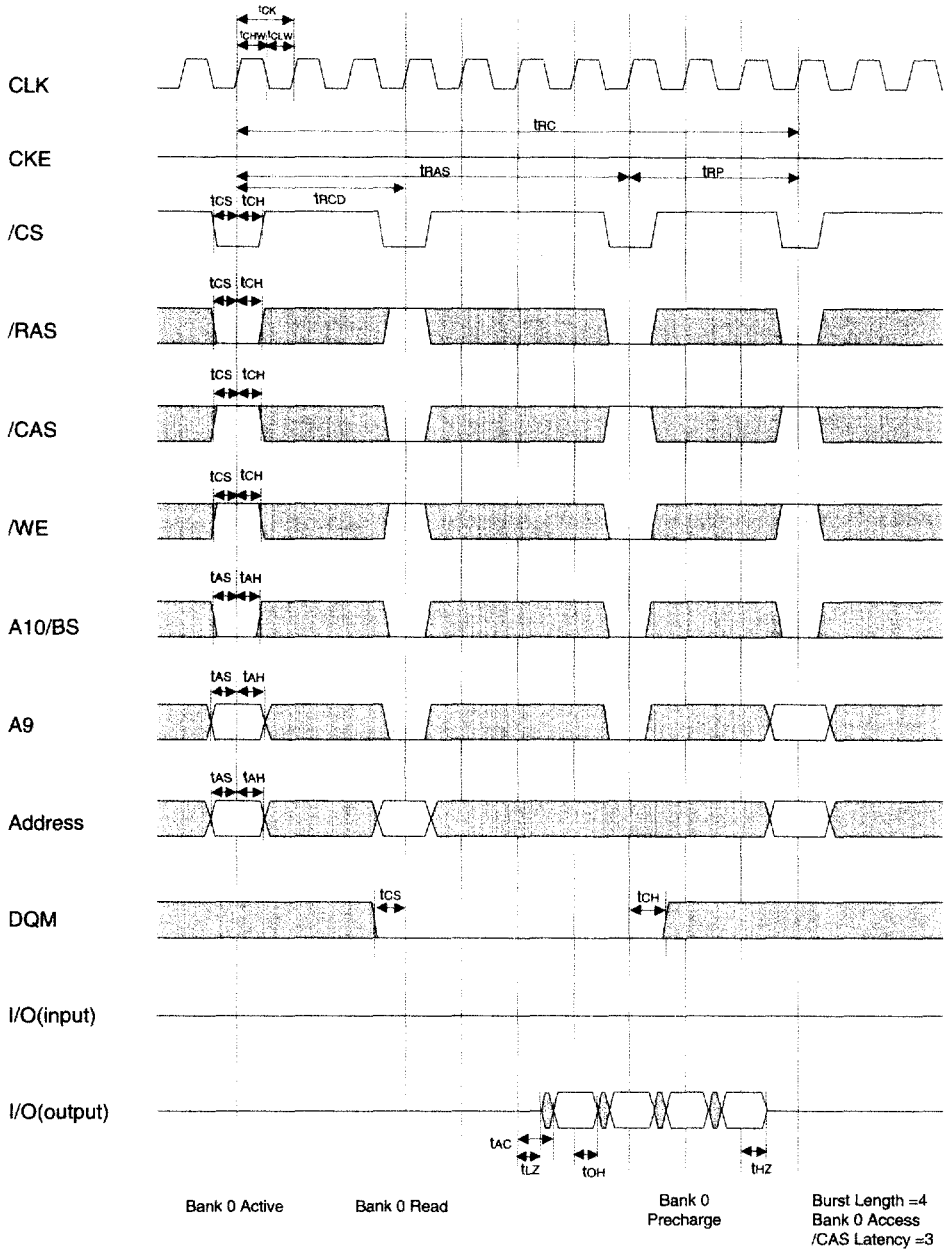
The minimum interval between special mode register set and block write/write is tSBW.



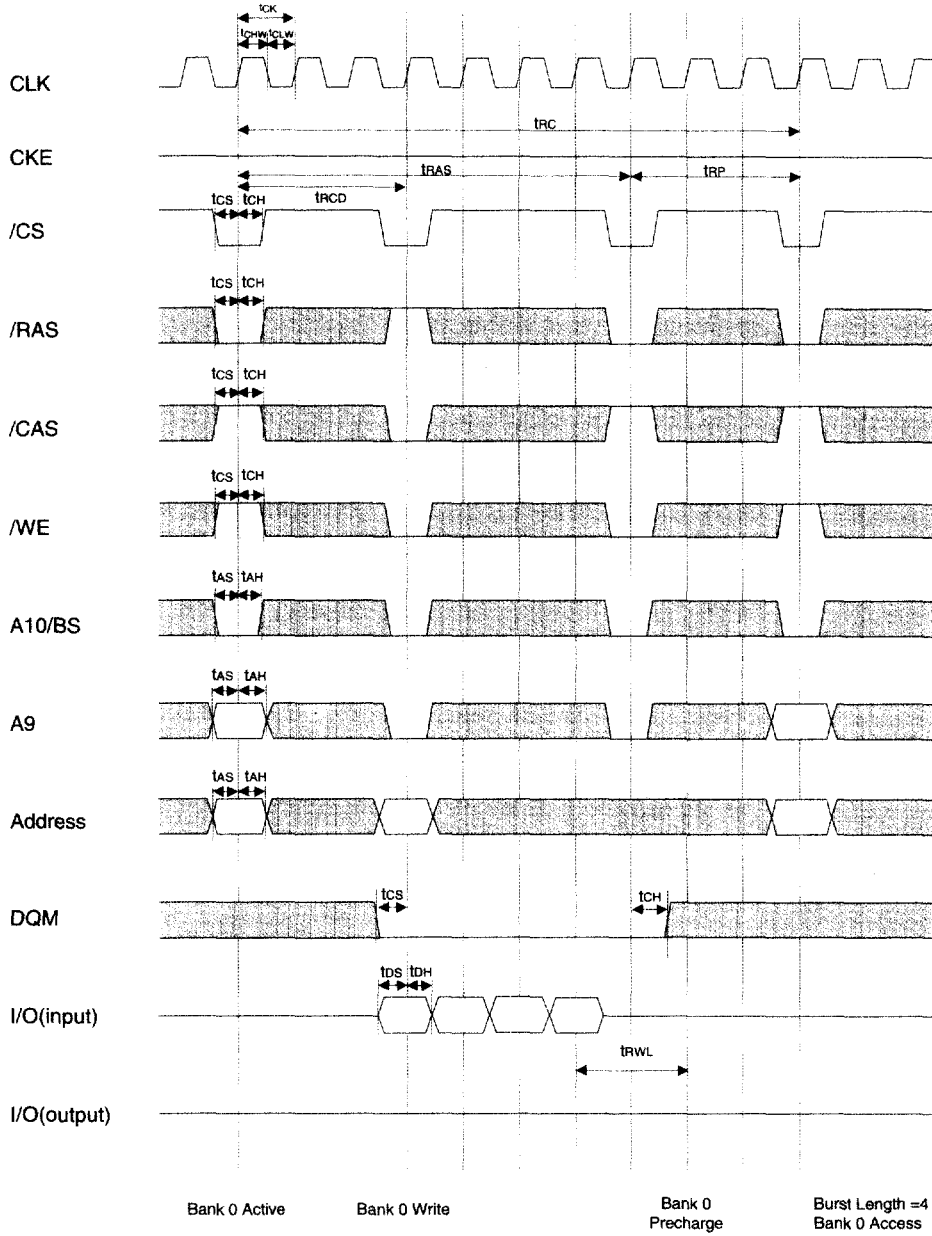
- Special mode register set to burst write interval

Timing Waveforms

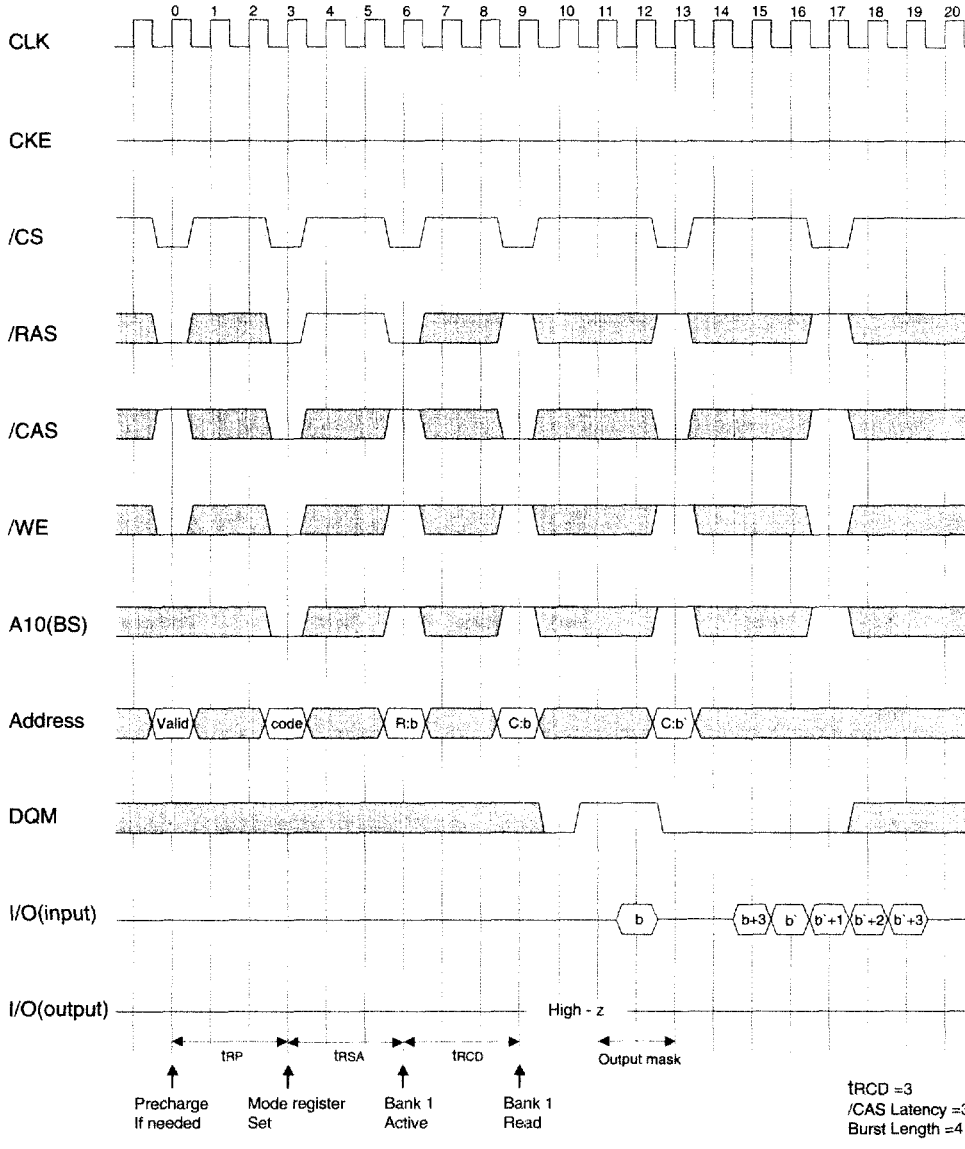
Read Cycle



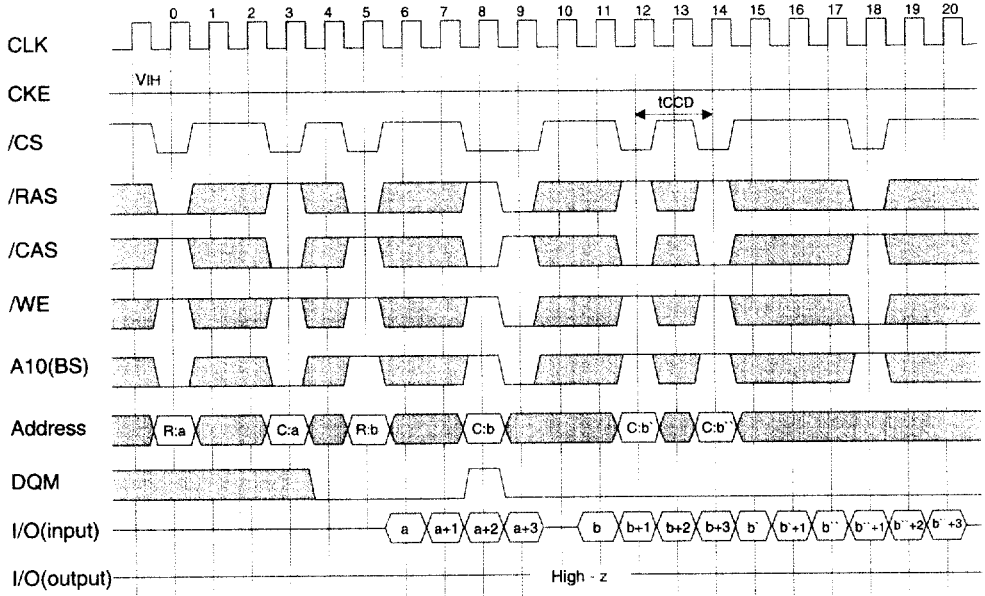
Write Cycle

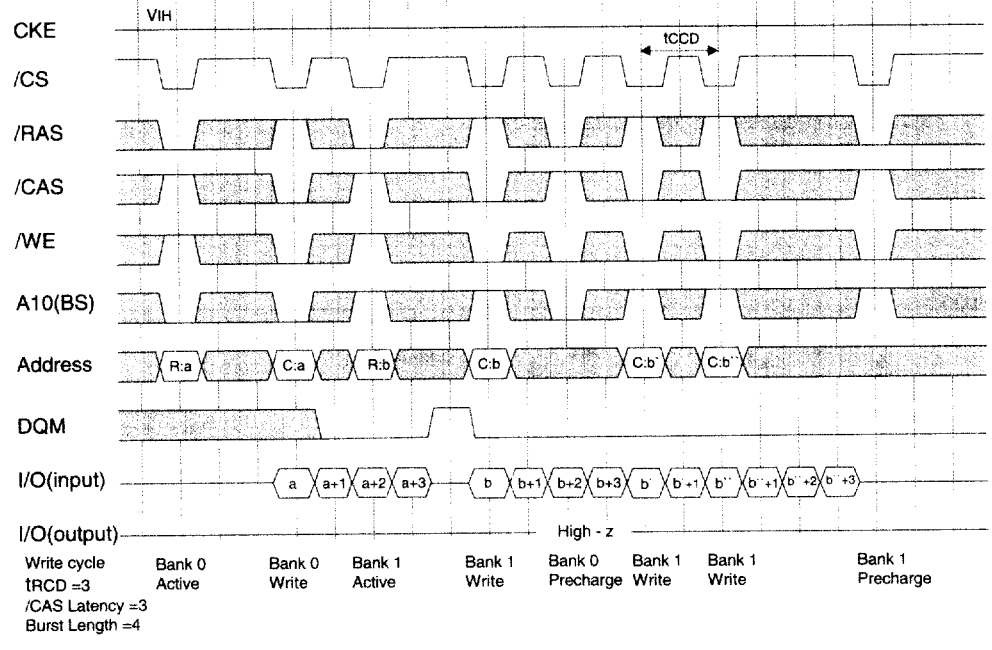

tCK
tCHW tCLW
CLK
tRC
CKE
tRAS
tRP
tCS tCH
tRCD
/CS
tCS tCH
/RAS
tCS tCH
/CAS
tCS tCH
/WE
tAS tAH
A10/BS
tAS tAH
A9
tAS tAH
Address
tCS
tCH
DQM
tDS tDH
I/O(input)
tRWL
I/O(output)
Bank 0 Active
Bank 0 Write
Bank 0
Precharge
Burst Length =4
Bank 0 Access

Mode Register Set Cycle

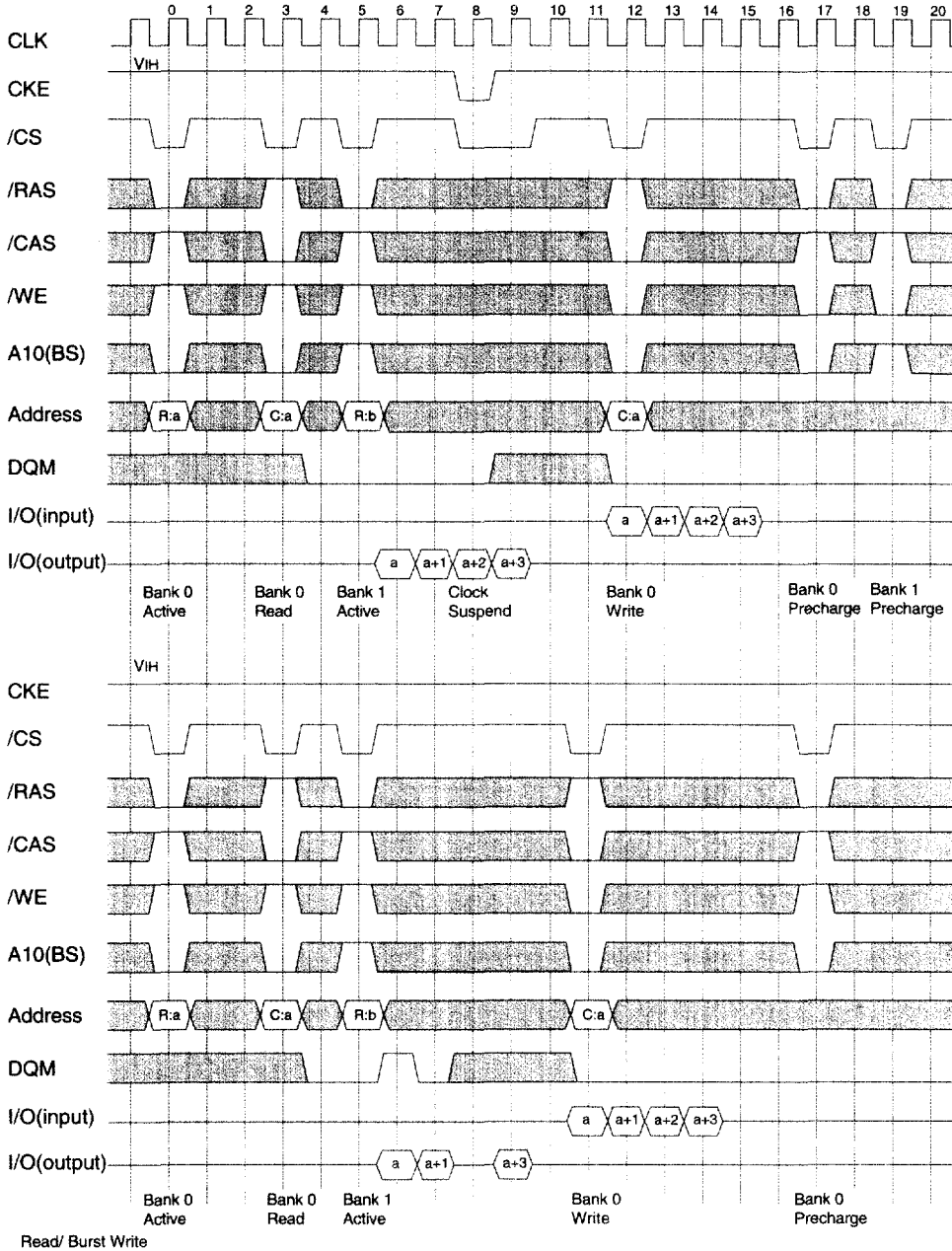


Read Cycle/Write cycle



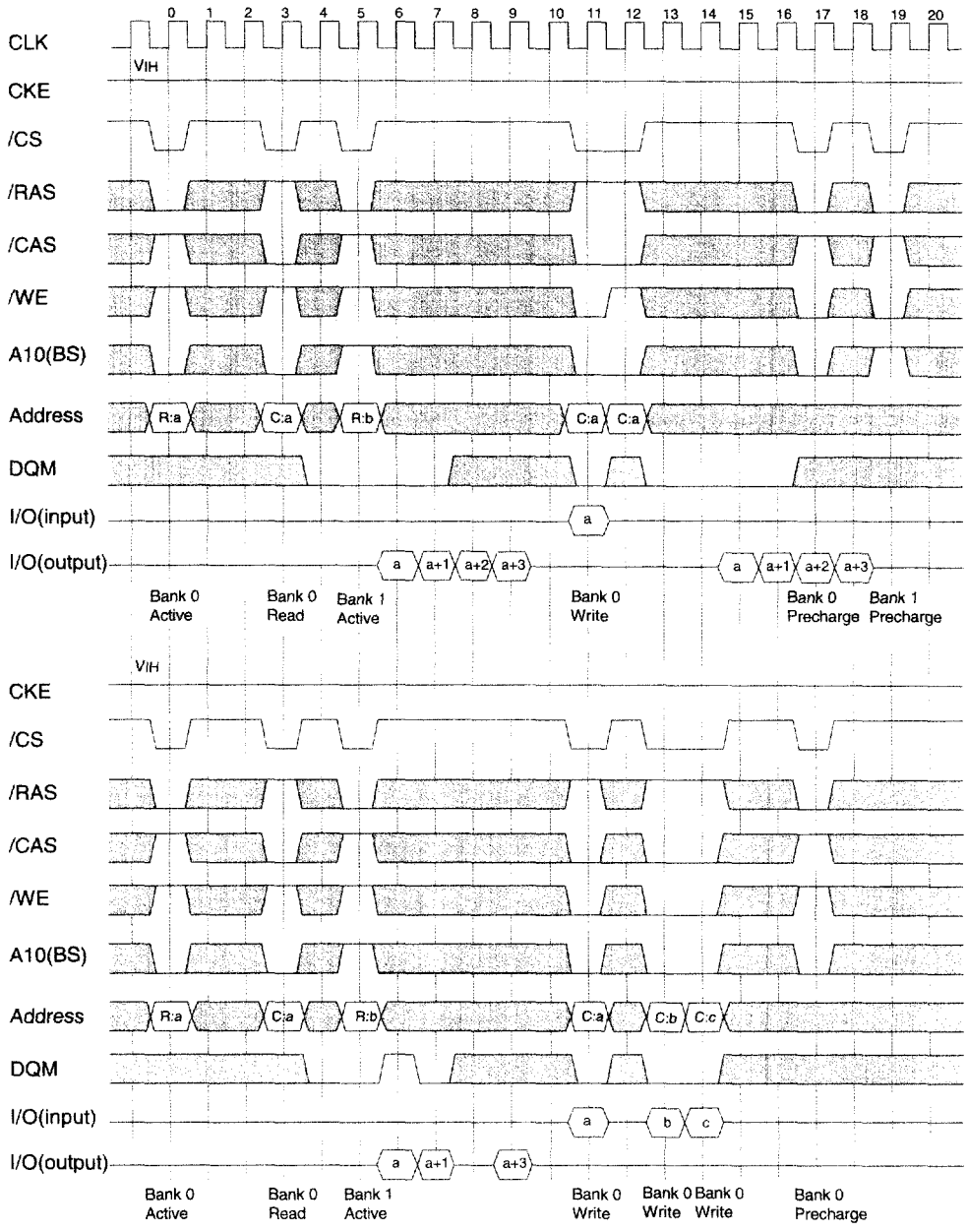


Read / Burst Write Cycle



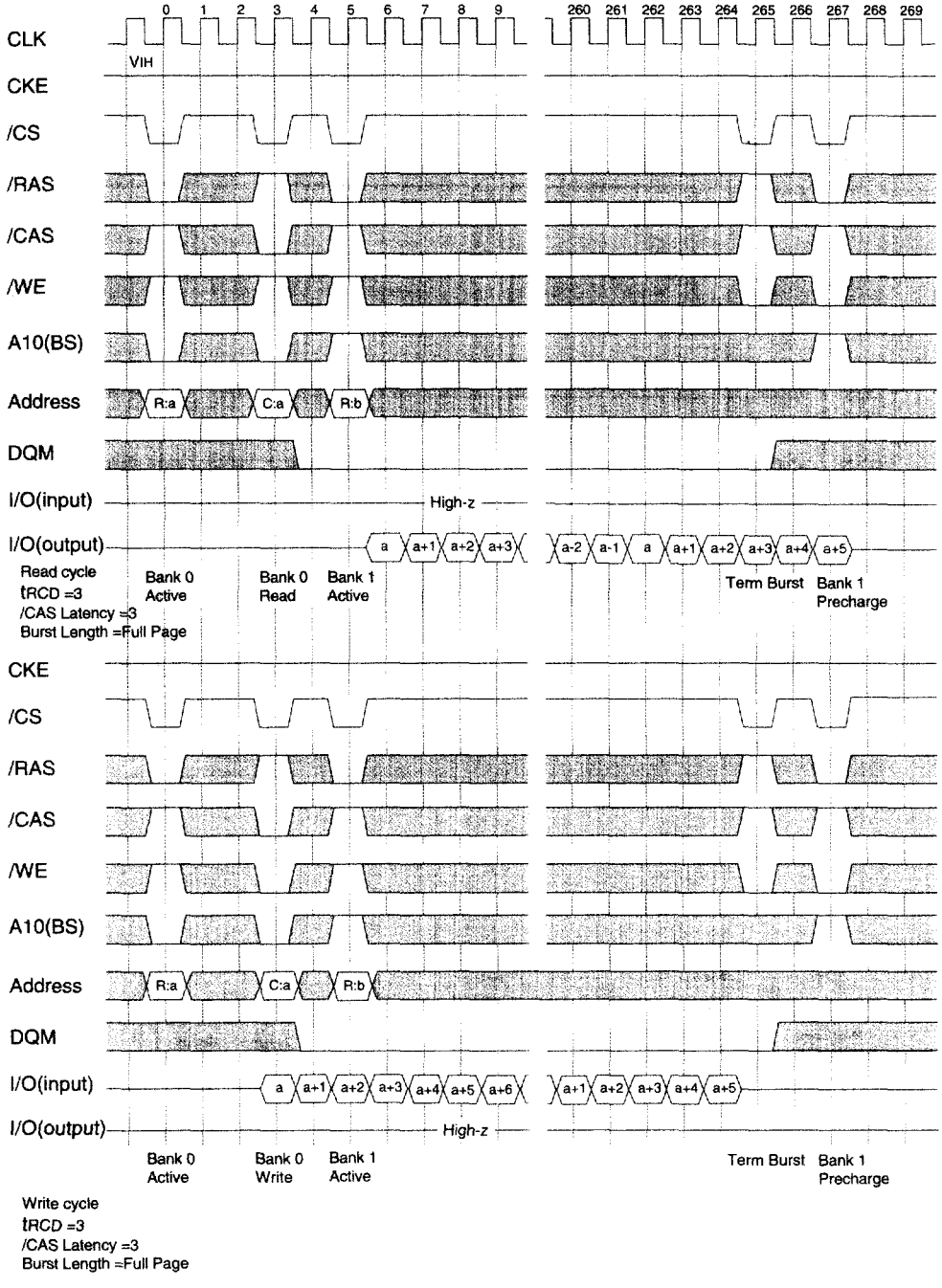
Read/ Burst Write
tRCD =3
/CAS Latency =3
Burst Length =4

Read / Single Write Cycle

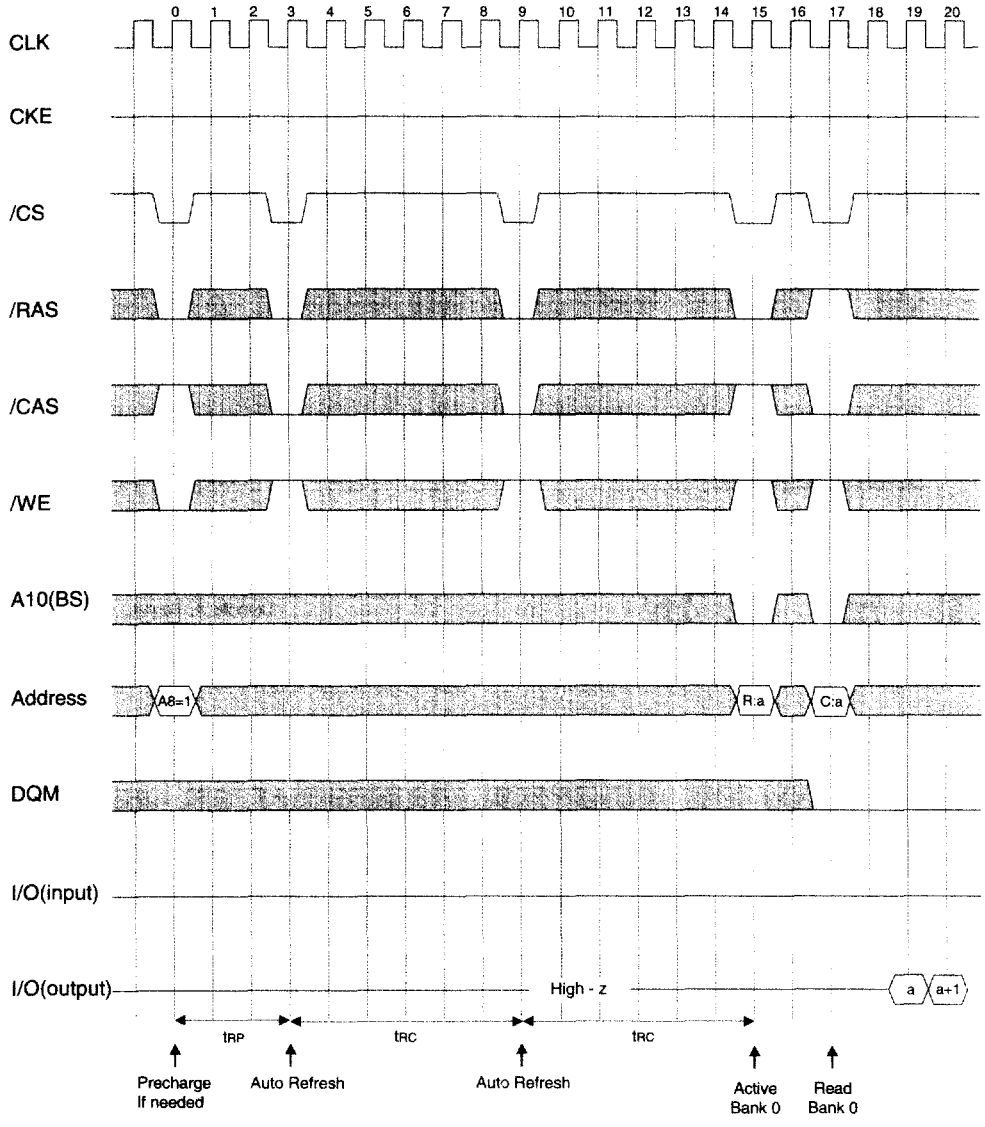


Read/ Single Write
tRCD =3
/CAS Latency =3
Burst Length =4

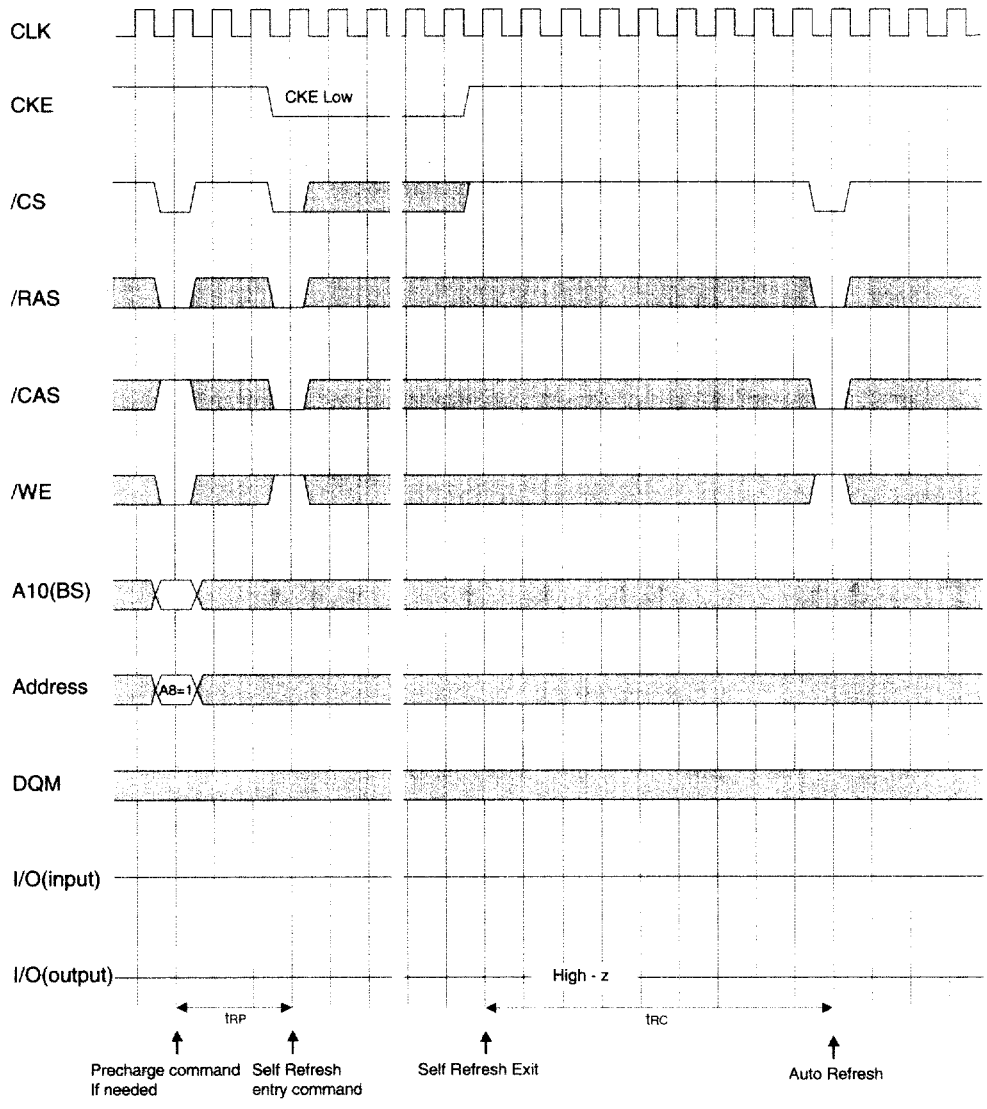
Full Page Read / Write Cycle



Auto Refresh Cycle

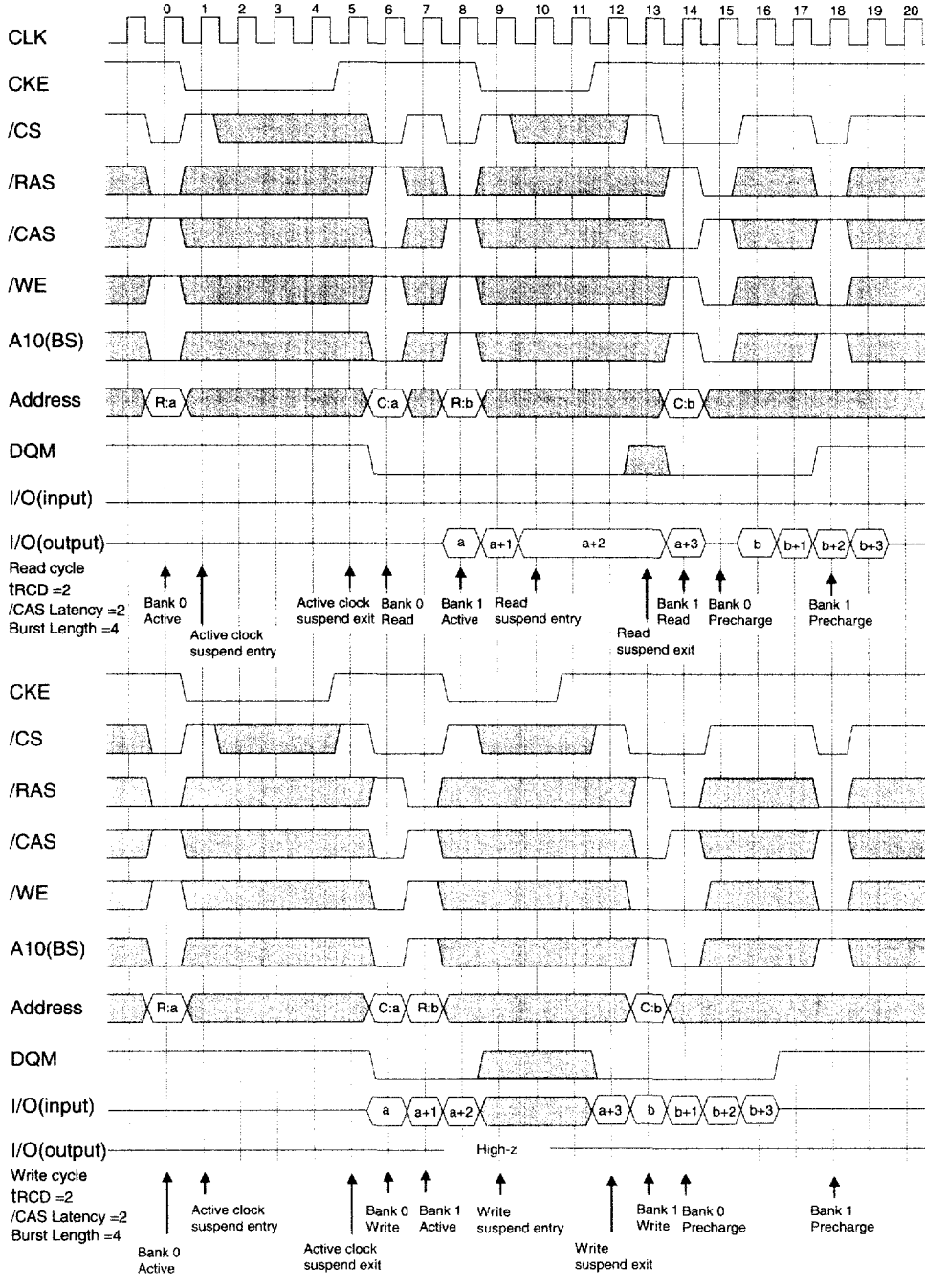


Self Refresh Cycle

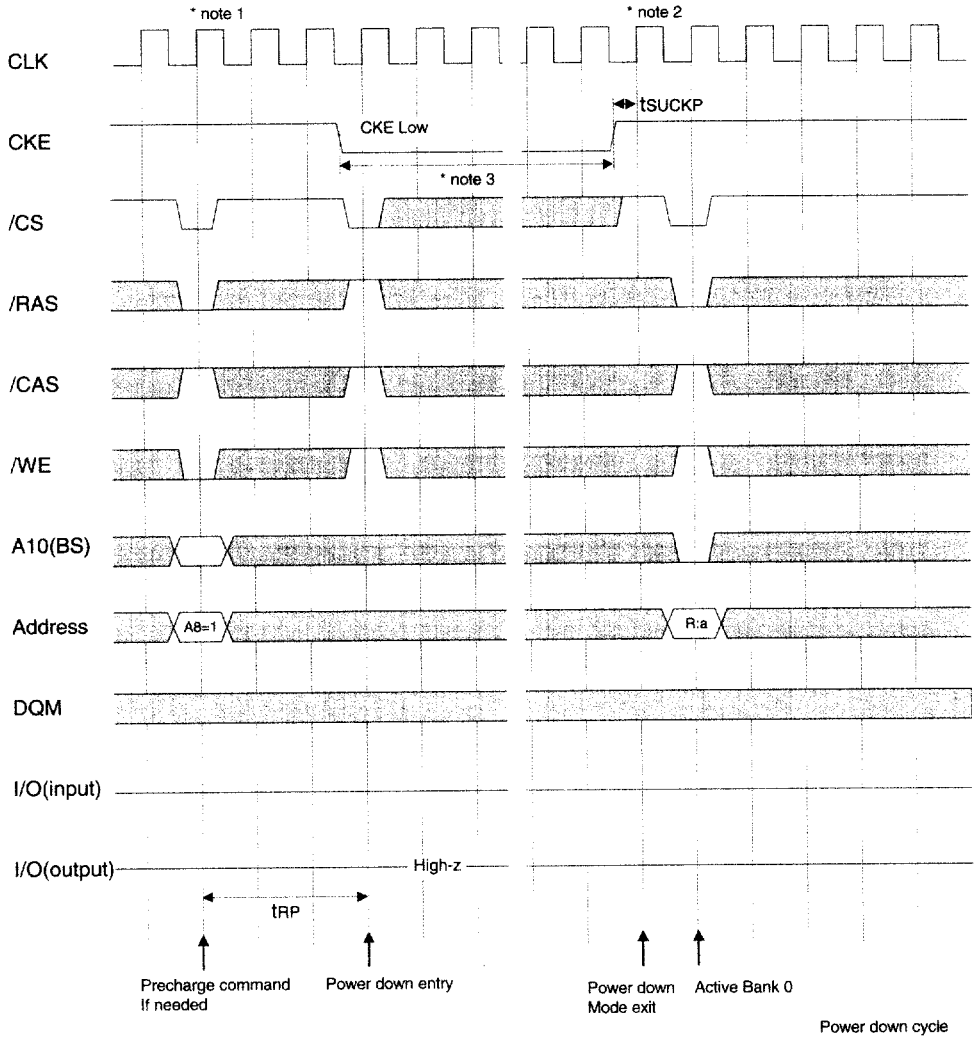


Self Refresh cycle
tRCD =3
/CAS Latency =3
Burst Length =4

Clock Suspend Mode



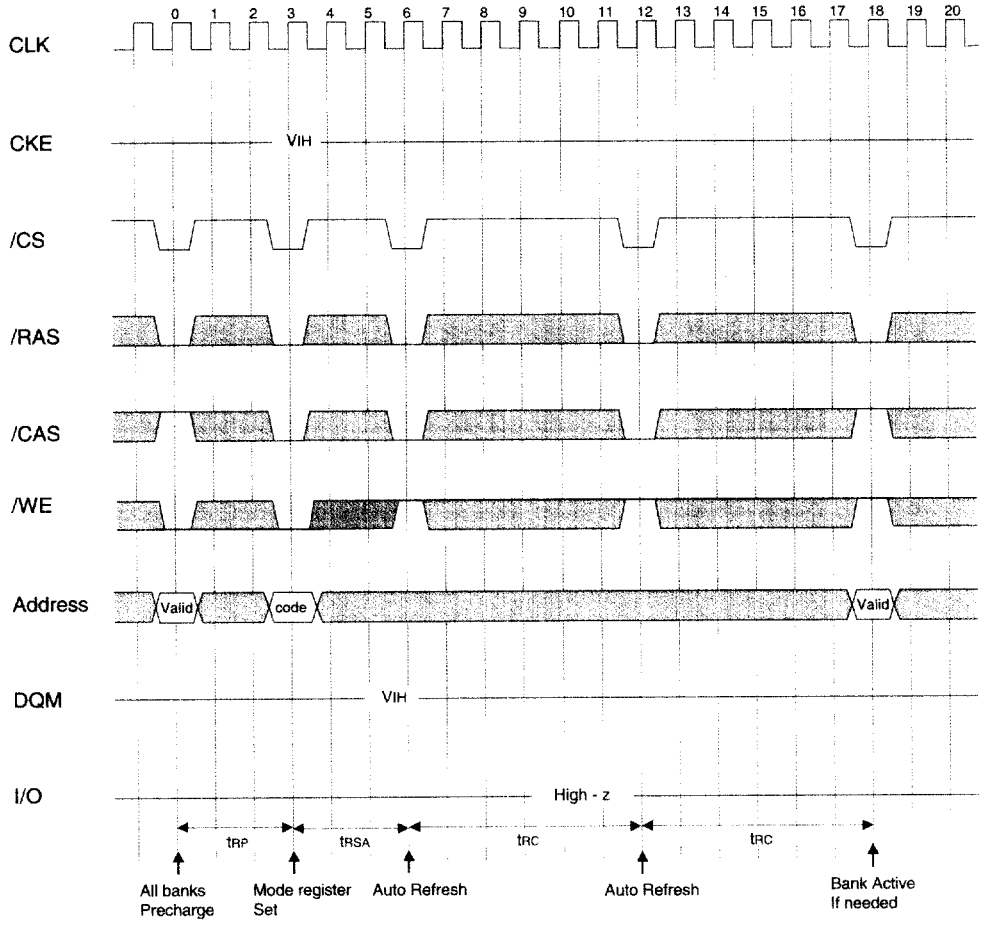
Power Down Mode



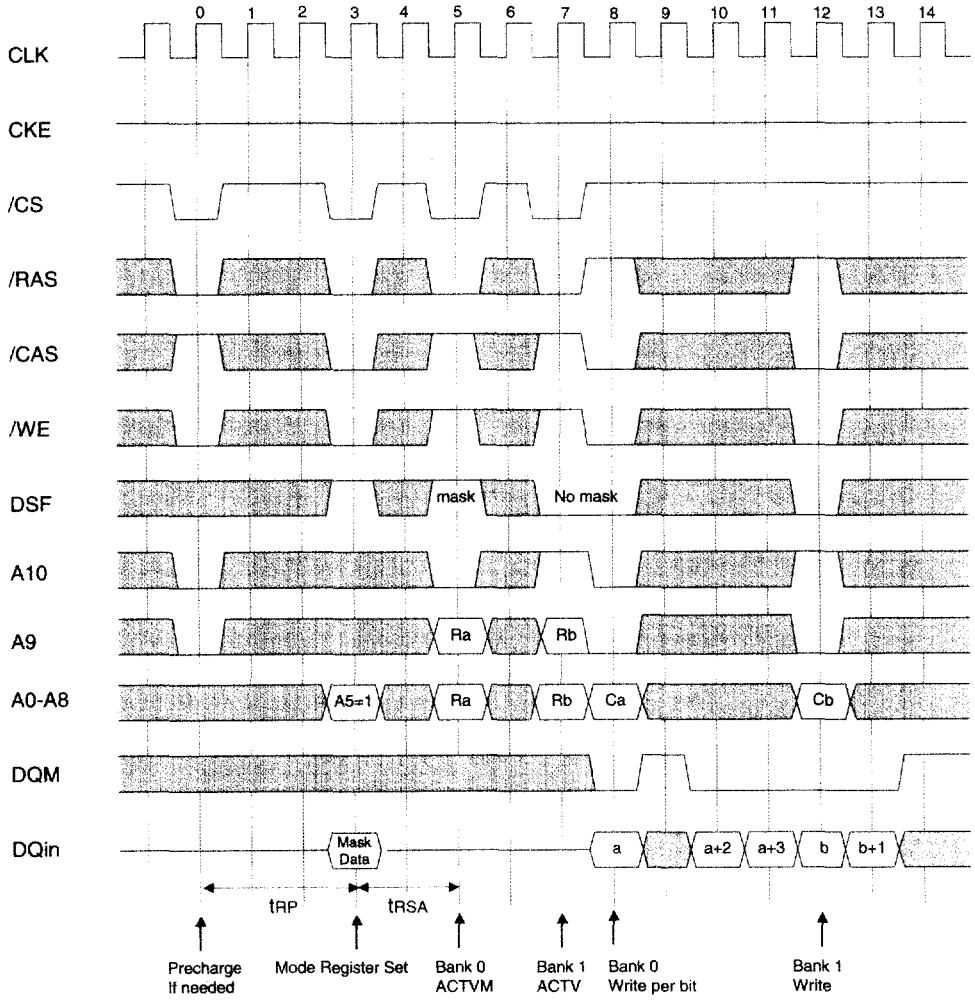
Power down cycle
tRCD =3
/CAS Latency =3
Burst Length =4

1. If needed all banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least tPDE prior to entering command.
3. Can not violate minimum refresh spec. (32ms).

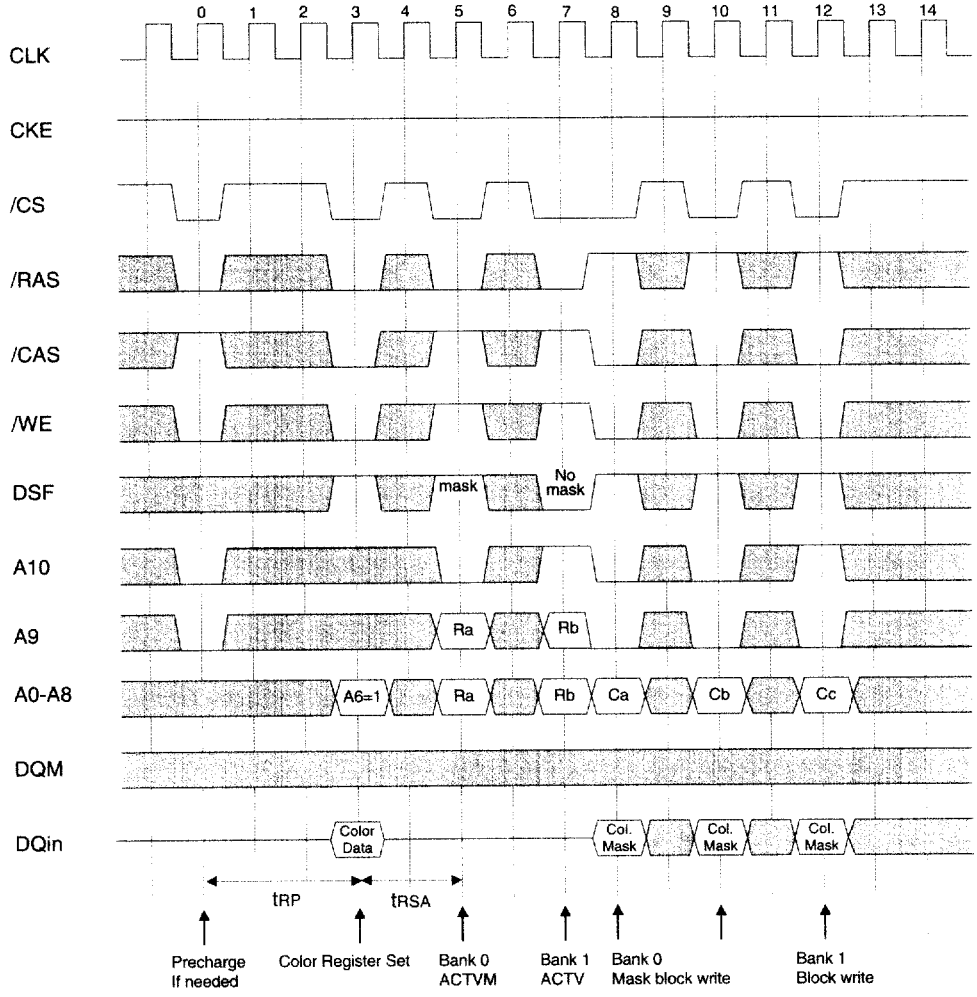
Power On Sequence



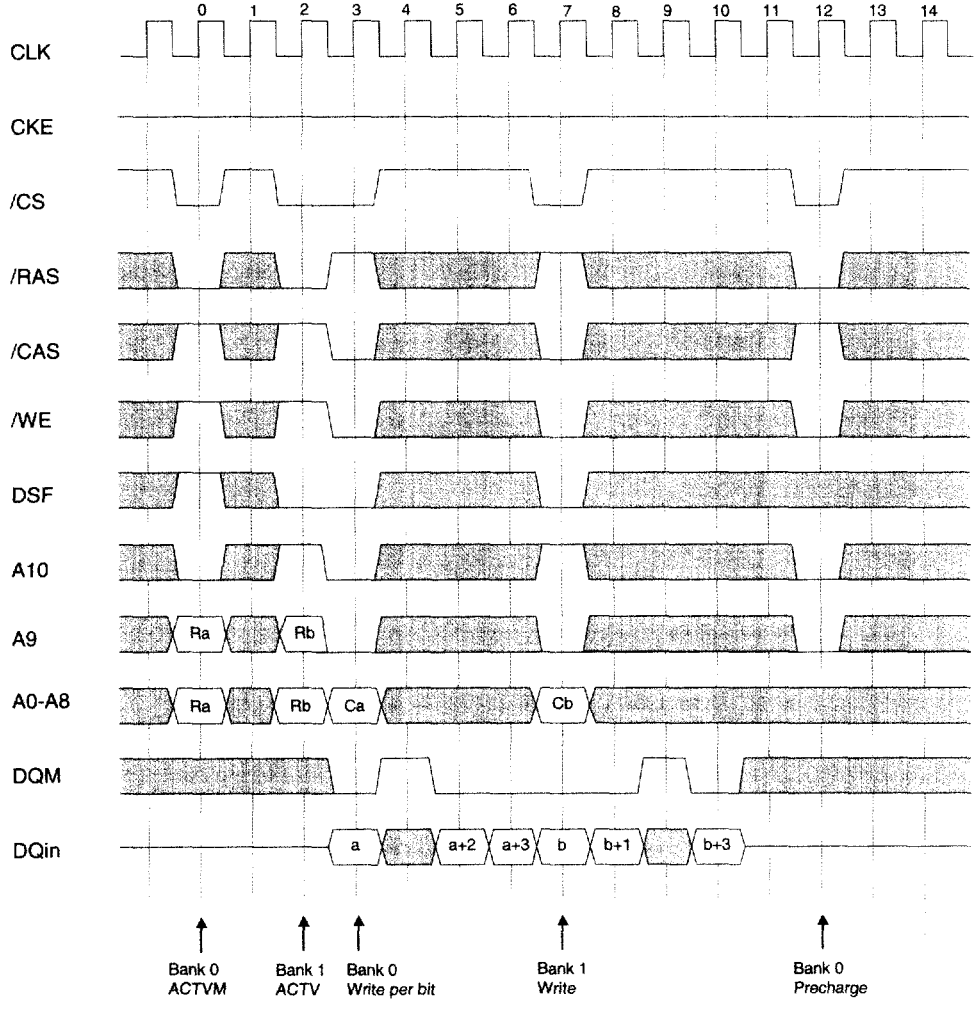
Mask Register Set Cycle



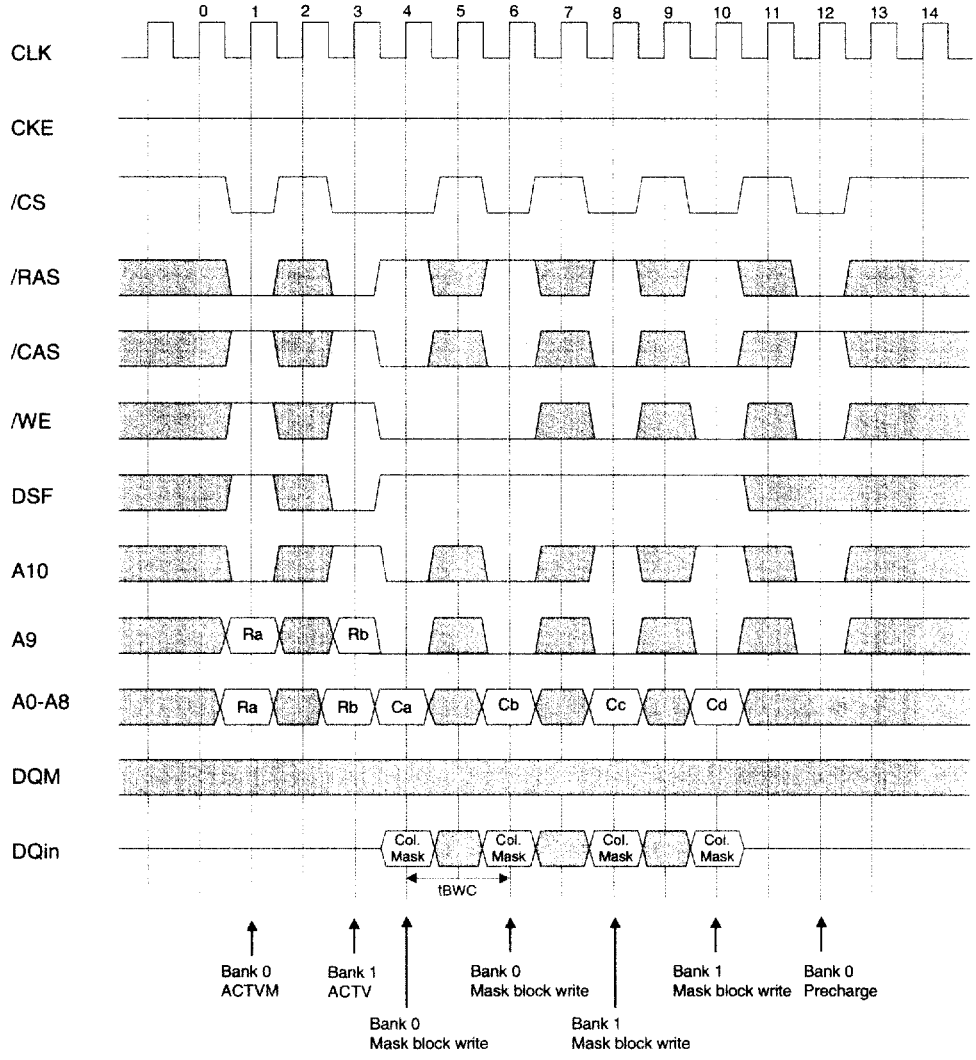
Color Register Set Cycle



Write Cycle (with I/O Mask)



Block Write Cycle



PACKAGE INFORMATION

20 x 14 mm^2 Thin Quad Flat Package (TQFP)