Digital video decoder and scaler circuit (DESC) SAA7194

SAA7194 NOT RECOMMENDED FOR NEW DESIGNS; USE SAA7196.

FEATURES

- Digital 8-bit luminance input (video (Y) or CVBS)
- Digital 8-chrominance input (CVBS or C from CVBS, Y/C, S-Video (S-VHS or Hi8))
- Luminance and chrominance signal processing for main standards PAL, NTSC and SECAM
- Horizontal and vertical sync detection for all standards
- User programmable luminance peaking for aperture correction
- Compatible with memory-based features (line-locked clock, square pixel)
- Cross colour reduction by chrominance comb filtering for NTSC or special cross-colour cancellation for SECAM
- UV signal delay lines for PAL to correct chrominance phase errors
- Square -pixel format with 768/640 active samples per line
- The bidirectional Expansion Port (YUV-bus) supports data rates of 780 x f_H (NTSC) and 944 x f_H (PAL, SECAM) in 4:2:2 format
- Brightness, contrast, hue and saturation controls for scaled outputs
- Down-scaling of video windows with 1023 active samples per line and 1023 active lines per frame to randomly sized windows
- 2D data processing for improved signal quality of scaled luminance data, especially for compression applications
- Chroma key (α-generation)
- YUV to RGB conversation including Anti-gamma ROM tables for RGB
- 16-word FIFO register for 32-bit output data
- Output configurable for 32/24/16-bit video data bus
- Scaled 16-bit 4:2:2 YUV output
- Scaled 15-bit RGB (5-5-5+α) and 24-bit (8-8-8+α) output
- Scaled 8-bit monochrome output
- Line increment, field sequence (off/even, interlace/non-interlace) and vertical reset control for easy memory interfacing
- Output of discontinuous data bursts of scaled video data or continuous data output with corresponding qualifier signals
- Real-time status information
- I^2C-bus control
- Only one crystal of 26.8MHz

DESCRIPTION

The CMOS circuit SAA7194, digital video decoder and scaler (DESC), is a highly integrated circuit for Desktop Video applications. It combines the functions of a digital video scaler (SAA7186).

The decoder is based on the principle of line-locked clock decoding. It runs at square-pixel frequencies to achieve correct aspect ratio.

Monitor controls are provided to ensure best display. Four data ports are supported:

Ports CVBS(7–0) and CHR(7–0) of the input interface are used in Y/C mode (Fig.1(a)) to decode digitized luminance and chrominance signals (digitized in two external ADCs).

In normal mode, the CVBS(7–0) input is only used, and only one ADC is necessary. The 32-bit VRAM output port is interface to the video memory; it outputs the down-scaled video data. Different formats and operation modes are supported by this circuit.

The 16-bit wide Expansion Port is a bidirectional port. In general, it establishes the digital YUV as known from the SAA71x1 family of digital decoders. In addition, the Expansion port is configurable to send data from the decoder unit or to accept external data fro input into the scaler. In input mode the clock rate and/or the sync signals may be delivered by the external data source.

Decoder and scaler units can run at different clock rates. The decoder processing always operates with a line locked clock (LLC). This clock is derived from the CVBS signal and is suited best for memory based video processing; the LLC clock is always present the scaler clock may be driven by the LLC clock or by an external clock depending on the configuration of the Expansion port.

The circuit is I^2C-bus-controlled. The I^2C-bus interface is clocked by LLC to ensure proper control.

The I^2C-bus control is divided into two sections:
- subaddress 00h to 1F for the decoder part
- subaddress 20h to 3F for the scaler part

The programming of the subaddresses for the scaler part becomes effective at the first vertical sync pulse VS after a transmission.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
SAA7194	120	QFP	plastic	SOT349 AA1

SAA7194 is a subset of SAA7196. In SAA7194, the internal CGC function is not available. Therefore, the pins 36, 37, 38 40 and 42 are defined differently, as shown in the following table:

SIGNAL NAME	PIN NUMBER	SAA7194	SAA7196	
RESN	36	I	O	
CGCE	37	I I = LOW needs to be grounded	I	
			if grounded (LOW) ⇒ internal CGC is disabled IC functions like SAA7194	if pulled up (HIGH) ⇒ internal CGC is enabled full-function SAA7196
CREF	38	I	I	O
LLC	40	I	I	O
LLC2	42	O (reserved)	O	

For further specification on SAA7194, please refer to datasheet SAA7196. Figure 1(a) and Figure 34 are slightly different for SAA7194, and are shown as follows:

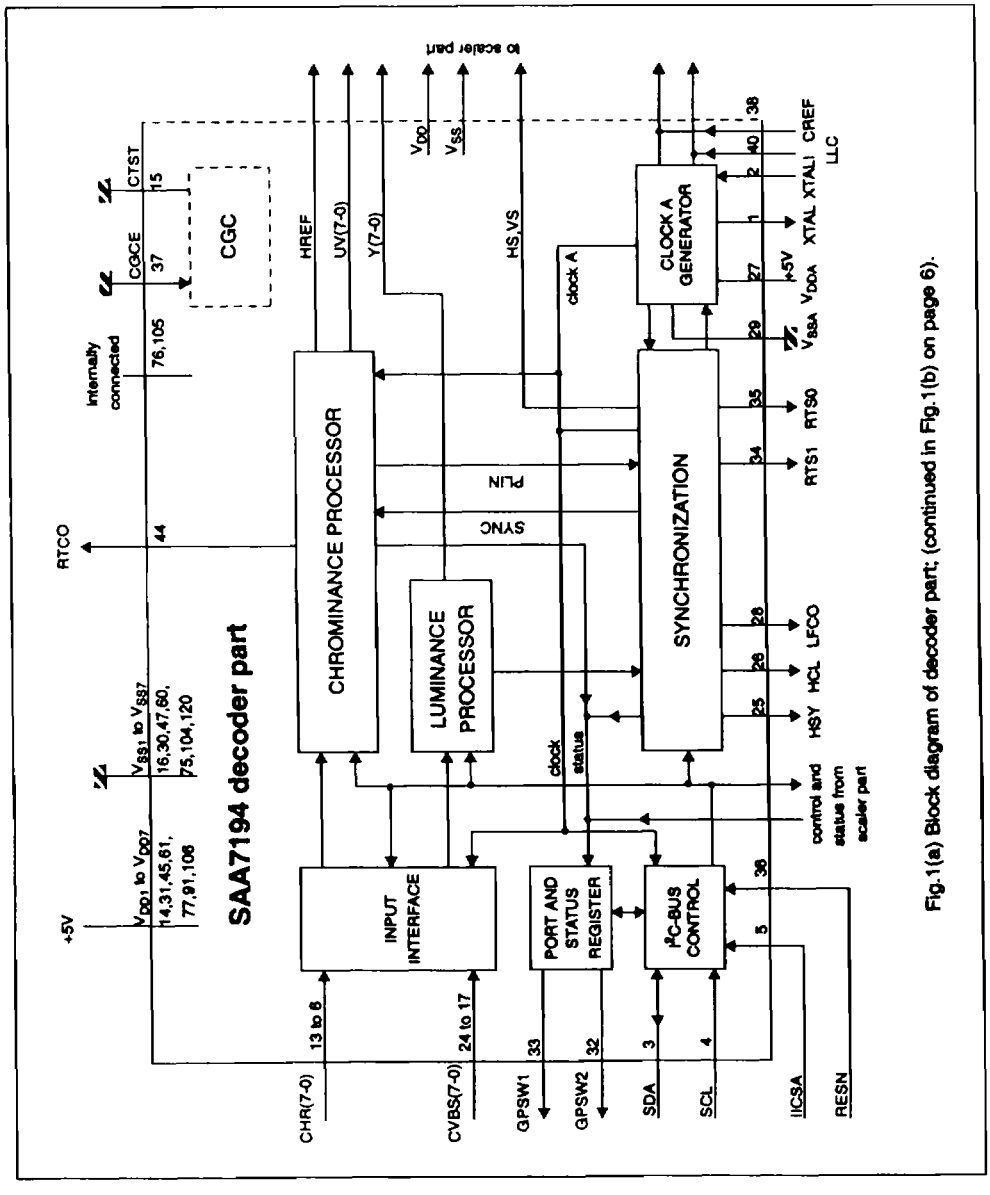

Fig.1(a) Block diagram of decoder part; (continued in Fig.1(b) on page 6).

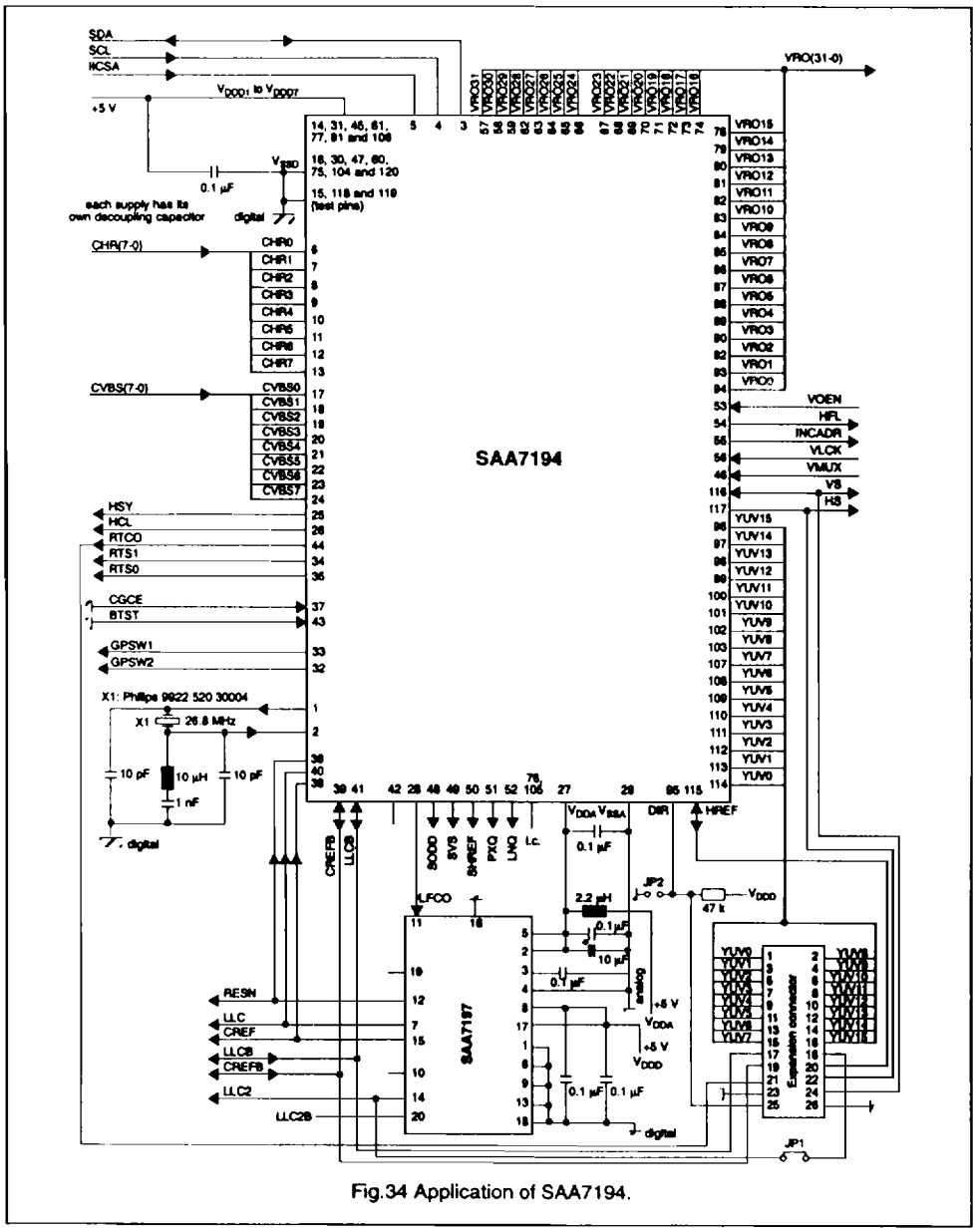

Fig.34 Application of SAA7194.