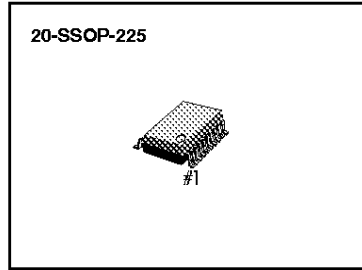


KS7221D

VERTICAL DRIVER FOR CCD

GENERAL DESCRIPTION

The KS7221D is a Vertical CCD Driver LSI which is fabricated by CMOS process for high voltage



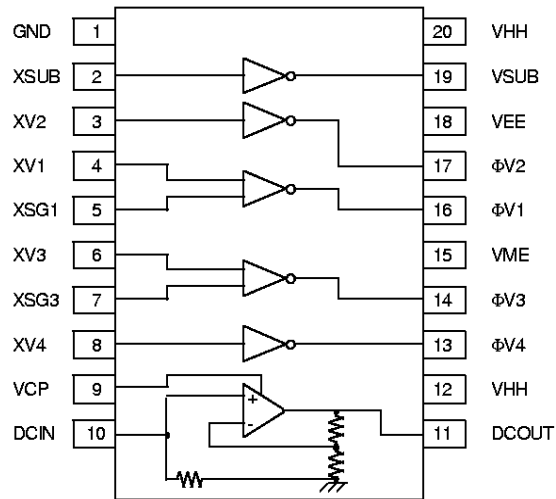
FEATURES

- Include voltage source circuit for CCD image sensor.
- Input voltage : 5V / 3.3V
- Package : 20 SSOP

ORDERING INFORMATION

Device	Package	Operating Temperature
KS7221D	20-SSOP-225	-20°C ~ + 85°C

BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Symbol	I/O	Description	Remark
1	GND	-	Ground control	
2	Xsub	I	Output Control (V_{sub})	
3	XV2	I	Output Control ($\Phi V2$)	
4	XV1	I	Output Control ($\Phi V1$)	
5	XSG1	I	Output Control ($\Phi V1$)	
6	XV3	I	Output Control ($\Phi V3$)	
7	XSG3	I	Output Control ($\Phi V3$)	
8	XV4	I	Output Control ($\Phi V4$)	
9	VCP	I	Power of amp	
10	DCIN	I	OP-Amp input (internal pull-down resistor)	
11	DCOUT	O	OP-Amp output	
12	VHH	-	Power (15V)	
13	$\Phi V4$	O	High Voltage Output (2 level : VME, VEE)	
14	$\Phi V3$	O	High Voltage Output (3 level : VME, VEE, VHH)	
15	VME	-	Power (0V)	
16	$\Phi V1$	O	High Voltage Output (3 level : VME, VEE, VHH)	
17	$\Phi V2$	O	High Voltage Output (2 level : VME, VEE)	
18	VEE	-	Power (-8.5V)	
19	V_{sub}	O	High Voltage Output (2 level : VEE, VHH)	
20	VHH	-	Power (15V)	

ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Value	Unit
Supply Voltage	VEE	0 ~ -10	V
	VHH	-0.3 ~ VEE +35	
	VME	VEE -0.3 ~ 3.0	
Input Voltage	VI	-0.3 ~ VHH +0.3	
	VCP	-0.3 ~ VEE+35	
Output Voltage	$\Phi V1, \Phi V2, \Phi V3, \Phi V4, \Phi V_{sub}$	VEE -0.3 ~ VHH +0.3	
OP-Amp output Current	I_{OUT}	± 5	mA
Operating Temperature	T_{OPR}	-25 ~ +85	$^\circ\text{C}$
Storage Temperature	T_{STG}	-45 ~ +120	

LOGIC FUNCTION TABLE

INPUT				OUTPUT		
XV1,3	XSG1,3	XV2,4	XSUB	FV1, 3	FV2, 4	VSUB
L	L	-	-	VHH	-	-
H	L	-	-	Z	-	-
L	H	-	-	VME	-	-
H	H	-	-	VEE	-	-
-	-	L	-	-	VME	-
-	-	H	-	-	VEE	-
-	-	-	L	-	-	VHH
-	-	-	H	-	-	VEE

AC CHARACTERISTICS(V_{HH} = 15V, V_{ME} = GND, V_{EE} = - 8.5V ; T_a = 25°C)

Description	Symbol	Test Condition	Min	Typ	Max	Unit
DELAY TIME	TPLM	NO LOAD (*1)	10	40	70	ns
	TPMH	NO LOAD (*1)	10	30	70	
	TPLH	NO LOAD (*1)	10	40	100	
	TPML	NO LOAD (*1)	10	100	200	
	TPHM	NO LOAD (*1)	10	100	180	
	TPHL	NO LOAD (*1)	10	60	100	
RISING TIME	TTLM	VEE → VME (*1)	400	700	930	
	TTMH	VME → VHH (*1)	400	650	930	
	TTLH	VEE → VHH (*1)	10	50	100	
	TTML	VME → VEE (*1)	200	300	500	
	TTHM	VHH → VME (*1)	400	600	820	
	TTHL	VHH → VME (*1)	10	50	100	
OUTPUT NOISE VOLTAGE	VCLH, VCLL VCMH, VCML	(*2)	-	-	0.5	V

(*1) REFER TIMING DIAGRAM

(*2) REFER NOISE DIAGRAM

DC CHARACTERISTICS(V_{HH} = 15V, V_{ME} = GND, V_{EE} = - 8.5, V_{CP} = 22V ; T_a = 25°C)

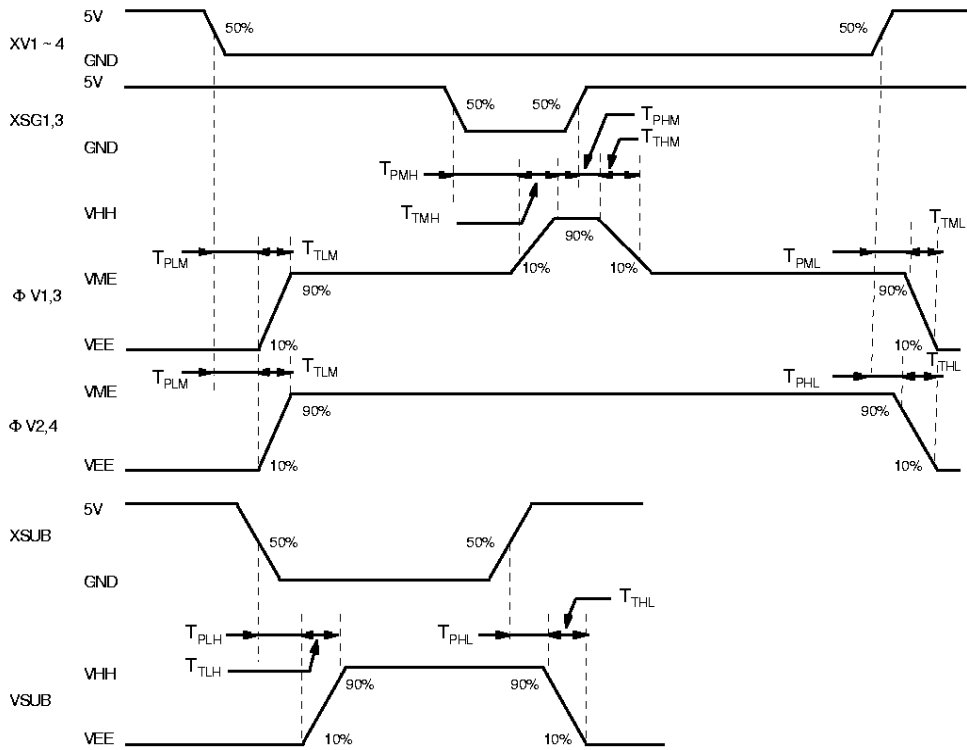
Description	Symbol	Test Conditon	Min	Typ	Max	Unit
Supply Voltage	V _{HH}		14.5	15	15.5	V
	V _{EE}		-9.5	-8.5	-7.5	
Input Voltage	V _{CP}	When V _{CP} is used	V _{HH}	22	23.5	
High level input voltage	V _{IH}	(*3)	2.3	-	-	
Low level input voltage	V _{IL}	(*3)	-	-	1.2	
Input Current	I _I	V _{IN} = 0~5V (*3)	-1.0	0.0	1.0	μA
	I _{DCIN}	V _{DCIN} = 1.0V	80	100	140	
Operation Current	I _{IH}	(*1)	-	2.0	3.5	mA
	I _{ME}	(*1)	-	4.5	5.0	
	I _{EE}	(*1)	-8.5	-6.5	-	
Output Current	I _{OL}	φV _{1~4} = -8.0V	25	37	-	
	I _{OM1}	φV _{1~4} = -0.5V	-	-15	-10	
	I _{OM2}	φV _{1,3} = 0.5V	9	13.5	-	
	I _{OH}	φV _{1,3} = 14.5V	-	-18	-12	
	I _{OSL}	V _{SUB} = -8.0V	12	18	-	
	I _{OSH}	V _{SUB} = 14.5V	-	-10.5	-7	
Op-Amp Gain	G	I _{OUT} = -200μA	x 4.0	x 4.2	x 4.7	
Gain Variation	ΔG	T _a = -20 ~ 75°C (*2), I _{out} = -200μA V _{DCIN} = 1.0 ~ 4.5V	-3	-	+3	%
Operation Current	I _{VCP}	V _{DCIN} = 1.0 ~ 4.5V I _{OUT} = 0μA	0.08	-	1.0	mA

(* 1) : Refer the test direct. Shutter speed : 1/1000000 SEC

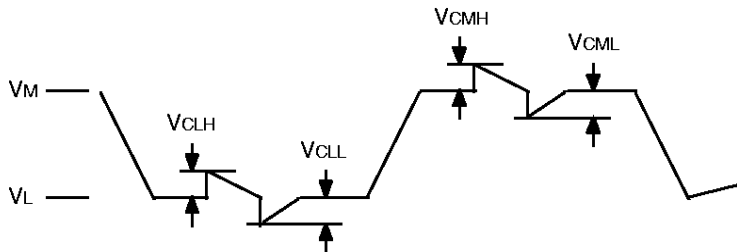
(* 2) : Refer the characteristics of OP - AMP

(* 3) : X_{V1} ~ 4, X_SG1, X_SG3, X_SUB PIN

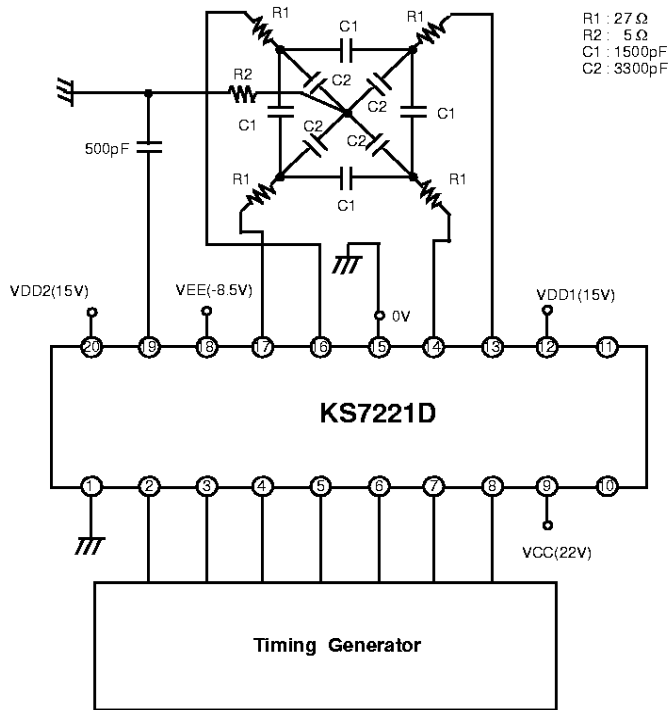
TIMING DIAGRAM



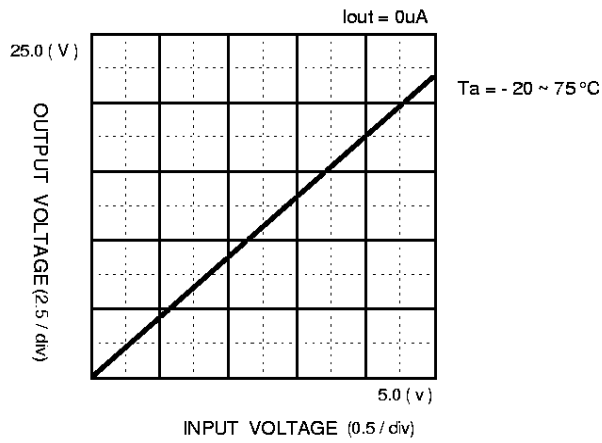
NOISE DIAGRAM



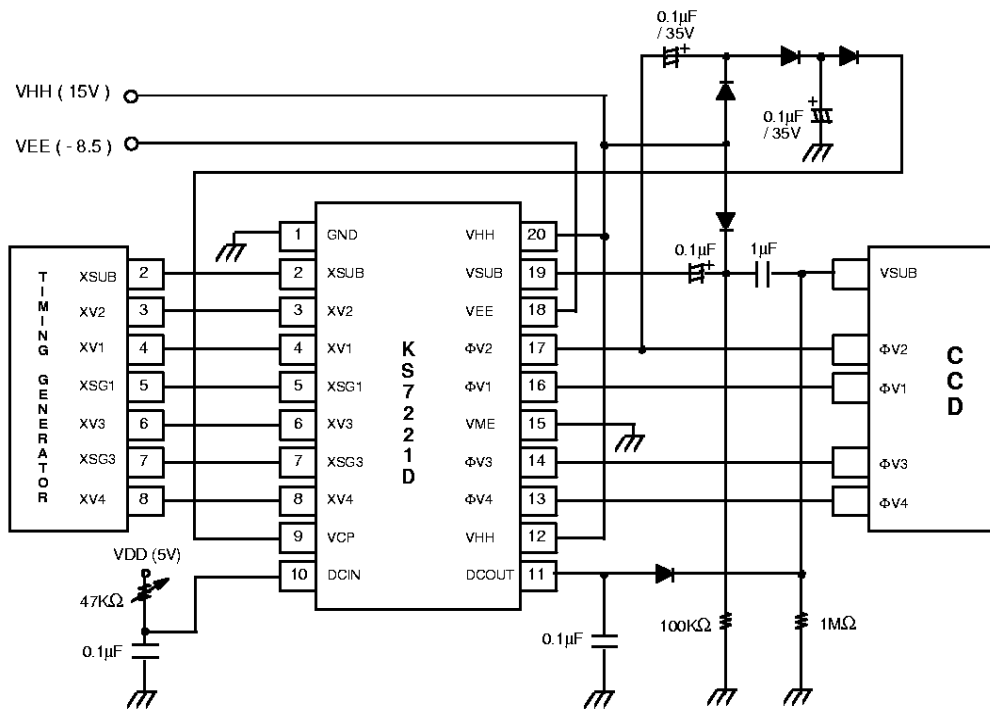
TEST CIRCUIT



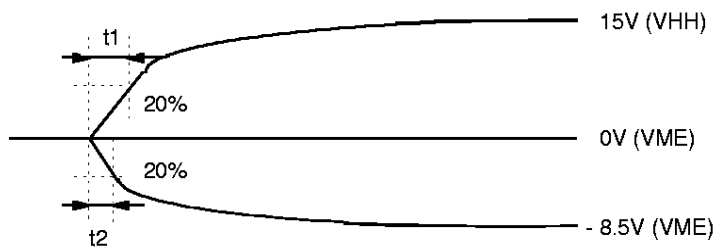
OP-AMP Gain Characteristics



APPLICATION CIRCUIT



* In case of $DCOUT \leq VHH - 1.0V$, V_{CP} PIN connects with VHH.
 Warning: When voltage is biased, You must keep this flow.
 if you don't this flow, Negative voltage is applied to CCD image sensor's SUB.



* $t1 > t2 \geq 10ms$

PACKAGE DIMENSION

