FUJITSU

CMOS 128K-BIT EEPROM CARD

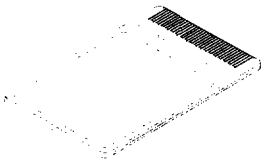
MB98804RC

February 1988
Edition 1.0

CMOS 128K (131,072)-BIT ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY CARD

The MB98804 is a memory card which is composed of two MBM28C64 EEPROM organized as 16,384 words x 8 bits housed in 38-pin plastic package. This card has TTL compatible Input/Output and three state output level with fully static operation and a single +5V power supply is required.

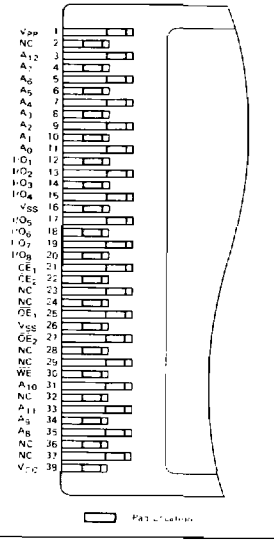
Dimensions of the card are Fujitsu standard.



PLASTIC CARD
CRD-38P-M03

- Card size: 2.216 width x 3.370 length x 0.081 height (inches)
- Organization: 16,384 words x 8 bits
- Access time: 350 ns max.
- Minimum endurance of 10,000 Erase/Write cycle per byte
- Write status identificator: $\overline{\text{DATA}}$ POLLING
- Single +5V power supply
- Power dissipation: 163 mW max. (Active)
  10.5 mW max. (Standby, TTL input level)
  1.05 mW max. (Standby, CMOS input level)
- Fujitsu's original recessed edge connector helps to prevent chip damage from static electricity.
- On-chip series resistors for further protection from Electro-Static Discharge

PIN ASSIGNMENT
(TOP VIEW)



ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V
All Inputs/Outputs Voltage	V_{IN}, V_{OUT}	-0.3 to V_{CC}+0.3	V
Voltage on $\overline{OE}$	V_{OE}	-0.3 to +13.5	V
Temperature under Bias	T_{BIAS}	-10 to +60	°C
Storage Temperature	T_{STG}	-30 to +70	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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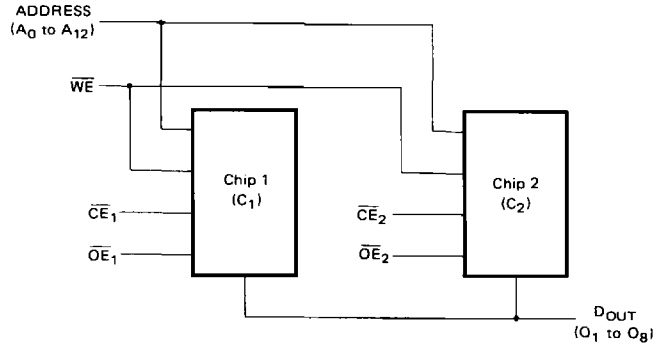
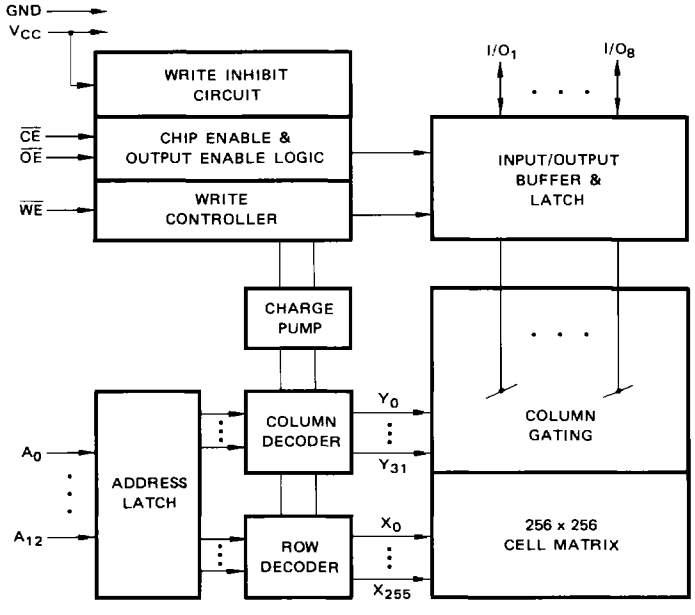
FUNCTIONAL BLOCK DIAGRAM



BLOCK DIAGRAM FOR EACH CHIP



PIN DESCRIPTION

Symbol	Pin Number	Parameter
A_0 to A_{12}	3, 4, 5, 6, 7, 8, 9, 10, 11, 31, 33, 34, 35	Address Input
I/O_1 to I/O_8	12, 13, 14, 15, 17, 18, 19, 20	Data I/O
$\overline{CE}_1$, $\overline{CE}_2$	21, 22	Chip Enable
$\overline{OE}_1$, $\overline{OE}_2$	25, 27	Output Enable
$\overline{WE}$	30	Write Enable
V_{CC}	1, 38	Supply Voltage (+5V)
V_{SS}	16, 26	Ground
NC	2, 23, 24, 28, 29, 32, 36, 37	Non Connection

CAPACITANCE (T_A = 25°C, f = 1MHz)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Input Capacitance (V_{IN} = 0V)	C_{IN}	–	T.B.D.	T.B.D.	pF
Output Capacitance (V_{OUT} = 0V)	C_{OUT}	–	T.B.D.	T.B.D.	pF

FUNCTIONAL TRUTH TABLE

Function / Mode	Address Input	$\overline{CE}_1$	$\overline{CE}_2$	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{WE}$	Data I/O	Power
Read (C_1)	A_{IN}	V_{IL}	V_{IH}	V_{IL}	Don't Care	V_{IH}	D_{OUT}	Read
Read (C_2)	A_{IN}	V_{IH}	V_{IL}	Don't Care	V_{IL}	V_{IH}	D_{OUT}	Read
Standby	Don't Care	V_{IH}	V_{IH}	Don't Care	Don't Care	Don't Care	High-Z	Standby
Write (C_1)	A_{IN}	V_{IL}	V_{IH}	V_{IH}	Don't Care	V_{IL}	D_{IN}	Write
Write (C_2)	A_{IN}	V_{IH}	V_{IL}	Don't Care	V_{IH}	V_{IL}	D_{IN}	Write
Write Inhibit 1 (C_1)	A_{IN}	Don't Care	V_{IH}	V_{IL}	Don't Care	Don't Care	–	–
Write Inhibit 1 (C_2)	A_{IN}	V_{IH}	Don't Care	Don't Care	V_{IL}	Don't Care	–	–
Write Inhibit 2 (C_1)	A_{IN}	Don't Care	V_{IH}	Don't Care	Don't Care	V_{IH}	–	–
Write Inhibit 2 (C_2)	A_{IN}	V_{IH}	Don't Care	Don't Care	Don't Care	V_{IH}	–	–
Data Polling (C_1)	A_{IN}	V_{IL}	V_{IH}	V_{IL}	Don't Care	V_{IH}	$I/O_8 = \overline{I}_8$, I/O_1 to I/O_7 = High-Z	Write
Data Polling (C_2)	A_{IN}	V_{IH}	V_{IL}	Don't Care	V_{IL}	V_{IH}		
Chip Erase (C_1)	Don't Care	V_{IL}	V_{IH}	V_{OE}	Don't Care	V_{IL}	V_{IH}	Write
Chip Erase (C_2)	Don't Care	V_{IH}	V_{IL}	Don't Care	V_{OE}	V_{IL}	V_{IH}	Write

Note: C_1 = Chip 1, C_2 = Chip 2
V_{OE} = 13.5V ± 1.5V
The address must be applied the written address and the all output data becomes input data from the point where the write mode is completed.

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
V_{CC} Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.2		V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.1		0.8	V
Ambient Temperature	T_A	0		50	°C

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DC CHARACTERISTICS

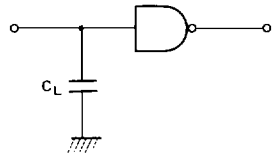
(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Value		Unit
			Min	Max	
V_{CC} Active Current	$\overline{CE}$ = V_{IL}*, I/O = OPEN	I_{CC1}		31	mA
	f = 4MHz, I/O = OPEN	I_{CC2}		31	mA
V_{CC} Write Current	$\overline{CE}$ = V_{IL}*, $\overline{WE}$ = V_{IL}	I_{CCW}		31	mA
V_{CC} Chip Erase Current	$\overline{CE}$ = $\overline{WE}$ = V_{IL}*, $\overline{OE}$ = V_{OE}	I_{CCE}		61	mA
V_{CC} Standby Current	$\overline{CE_1}$ = $\overline{CE_2}$ = V_{IH}, I/O = OPEN	I_{SB1}		2	mA
	$\overline{CE_1}$ = $\overline{CE_2}$ = V_{CC} ± 0.3V, I/O = OPEN	I_{SB2}		200	μA
Input Leakage Current	V_{IN} = 5.25V	I_{LI}		20	μA
Output Leakage Current	V_{OUT} = 5.25V	I_{LO}		20	μA
Output High Voltage	I_{OH} = -400μA	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 2.1mA	V_{OL}		0.45	V
Write Inhibit V_{CC} Level		V_{INH}	3.0		V
Chip Erase Voltage		V_{OE}	12	15	V

Note: * Either $\overline{CE_1}$ or $\overline{CE_2}$ must be satisfied V_{IH}.

AC TEST CONDITIONS

Input Pulse Level	:	0.8 to 2.2V
Input Pulse Rise/Fall Time	:	$t_T \leq 20$ns
Timing Reference Levels		
Input	:	V_{IL} = 0.8V, V_{IH} = 2.2V
Output	:	V_{OL} = 0.8V, V_{OH} = 2.0V
Output Load	:	1TTL gate and 100pF



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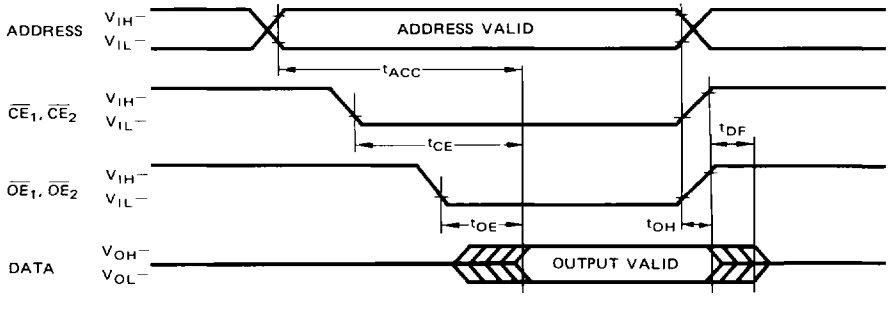
AC CHARACTERISTICS

READ MODE (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value		Unit
		Min	Max	
Address Access Time	t_{ACC}		350	ns
Chip Enable Access Time	t_{CE}		350	ns
Output Enable Access Time*1	t_{OE}		120	ns
Output Disable Time*2	t_{DF}		80	ns
Output Hold Time	t_{OH}	0		ns

Note: *1 t_{OE} delays up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
*2 t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
Output Float is defined as the point where data is no longer driven.

READ WAVEFORM



Note: Either $\overline{CE_1}$ or $\overline{CE_2}$ must be satisfied V_{IH}.

WRITE INFORMATION

BYTE WRITE

The MB98804's write mode is similar to that of static RAM. The write cycle is completely self-timed, and initiated by a low going TTL pulse on the $\overline{WE}$ pin. On the falling edge of $\overline{WE}$, the address data is latched. On the rising edge, the input data is latched. During the write cycle, the MB98804 automatically erases the memory data previously written and new data written into the memory is verified to ensure successfully the byte write.

CHIP ERASE

The MB98804 has a chip erase mode using external power supply which all data can be written to high state (= the erased state). The chip erase mode is initiated by setting $\overline{OE}$ to 13.5V and applying low TTL level to $\overline{WE}$ while holding all data inputs on high TTL level.

DATA POLLING

The MB98804 features Data Polling to signal the completion of a byte write cycle. During a write cycle, an attemped read of the last byte written results in the data complement of that byte at I/O_8. After completion of the write cycle, true data is available.

Data Polling allows a simple read/compare operation to determine the status of the chip eliminating the need for external hardware.

DATA PROTECTION

The MB98804 has three features to prevent a erroneous initiation of write mode.

- V_{CC} Detector: When the V_{CC} is less than +3V during V_{CC} power-on and power-off, the write function is inhibited.
- Noise Filter: When initiating write cycle, the write pulse of less than 20ns is locked.
- Write Inhibit: When $\overline{OE}$ is low TTL or $\overline{CE}$ is high TTL, the initiation of write cycle is inhibited.

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AC CHARACTERISTICS

DATA POLLING (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time to $\overline{WE}$	t_{ACS}	20			ns
Address Access Time	t_{ACC}			350	ns
Output Enable Access Time	t_{OE}			120	ns

Note: t_{OE} delays up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

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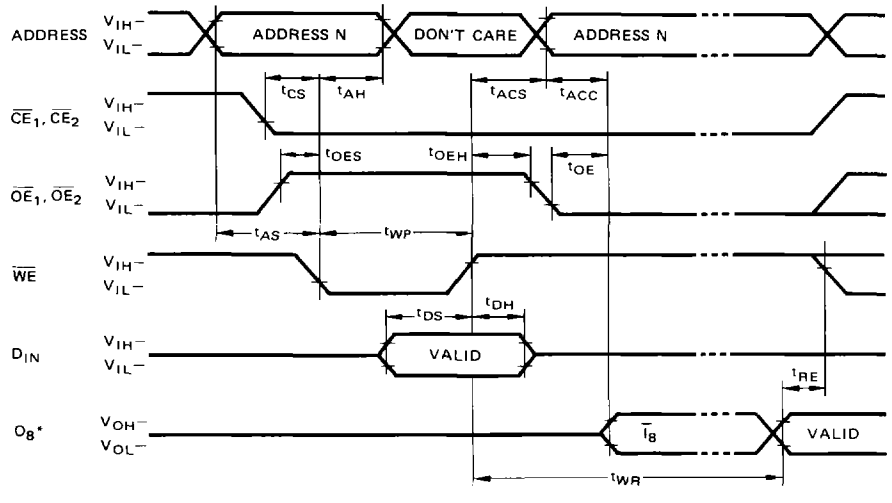
AC CHARACTERISTICS (continued)

BYTE WRITE (Recommended operating conditions unless otherwise noted.)

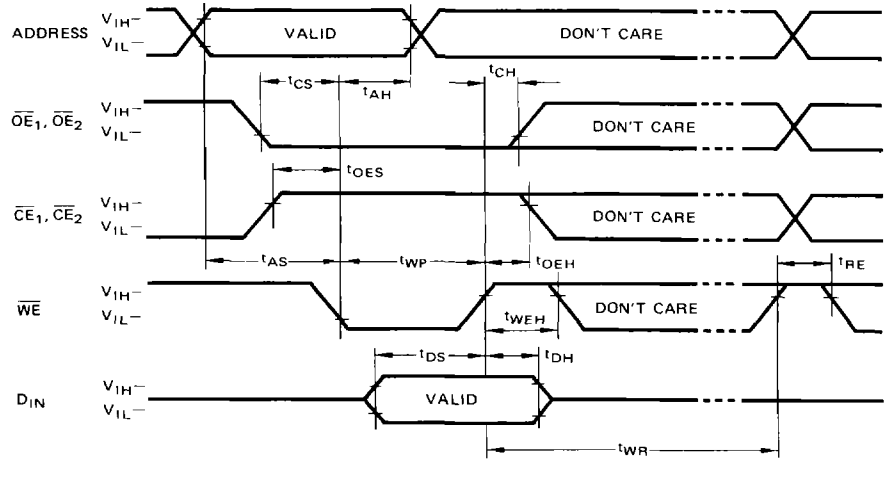
Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Address Setup Time	t_{AS}	20			ns
Data Setup Time	t_{DS}	50			ns
Address Hold Time	t_{AH}	50			ns
Data Hold Time	t_{DH}	20			ns
Output Enable Setup Time	t_{OES}	20			ns
Chip Enable Setup Time	t_{CS}	0			ns
Chip Enable Hold Time	t_{CH}	0			ns
Output Enable Hold Time	t_{OEH}	20			ns
Write Enable Hold Time	t_{WEH}	10			ns
Write Pulse Width	t_{WP}	100			ns
Write Recovery Time	t_{RE}	50			ns
Byte Write Cycle Time	t_{WR}			10	ms
Number of Write per Byte	n	10000			times

$\overline{\text{DATA}}$ POLLING WAVEFORM



Note: *O_1 through O_7 are in High-Z state till end of write.

BYTE WRITE WAVEFORM



AC CHARACTERISTICS (continued)

CHIP ERASE* (Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Data Setup Time	t_{DS}	150			ns
Data Hold Time	t_{DH}	100			ns
Output Enable Setup Time	t_{OES}	150			ns
Chip Enable Setup Time	t_{CS}	150			ns
Chip Enable Hold Time	t_{CH}	100			ns
Output Enable Hold Time	t_{OEH}	100			ns
Write Pulse Width	t_{WP}	5		20	ms

Note: * $\overline{OE}$ = 13.5V ± 1.5V

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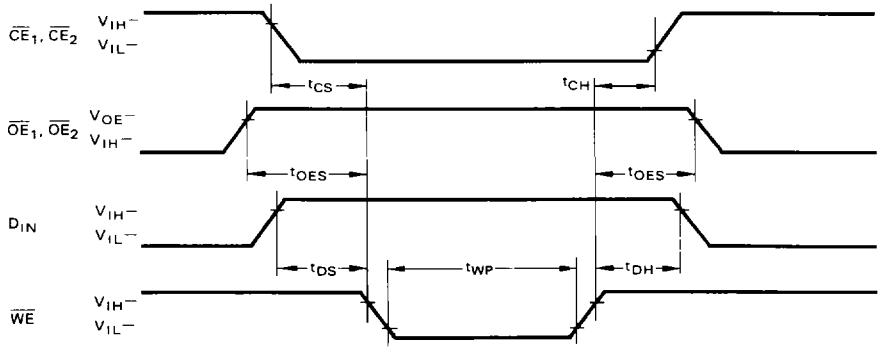
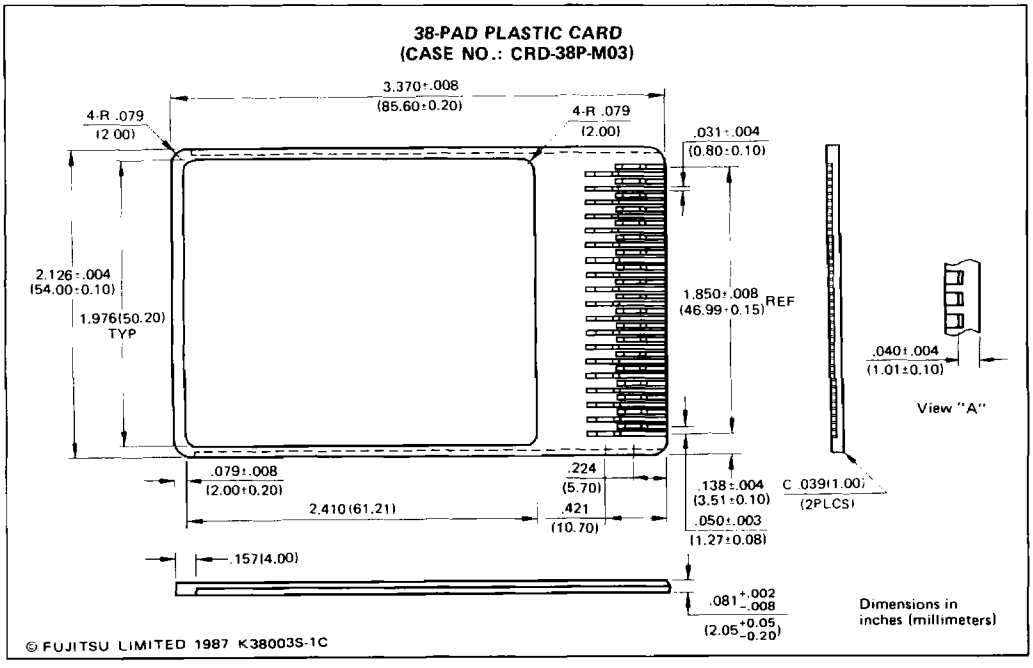
CHIP ERASE WAVEFORM



PACKAGE DIMENSIONS



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Memory Card Use Notice

- When not in use, it is recommended that the memory card be stored in its anti-static vinyl bag to prevent damage from static electricity.
- The card should be inserted before power-on to avoid possible data conflicts between the card and equipment. If the card is inserted or extracted with power-on, data may be output on the data pins even though $\overline{CE}$ and $\overline{OE}$ is at an "H".