

DAC-608, DAC-610, DAC-612

Microprocessor-Compatible, Double-Buffered D/A Converters

FEATURES

- Microprocessor-compatible
- Double-buffered inputs
- 8-, 10- and 12-Bit resolution
- 500 Nanoseconds settling time—DAC-610
- 4-Quadrant multiplication

GENERAL DESCRIPTION

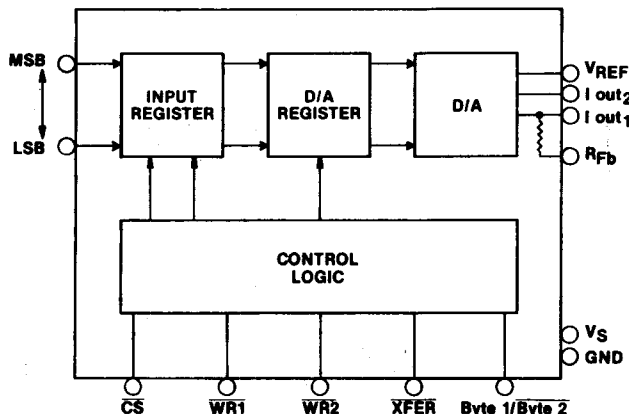
DATEL's DAC-608, DAC-610 and DAC-612 are low cost monolithic 8-, 10- and 12-bit multiplying D/A converters designed to operate directly with most popular microprocessors. Double-buffered inputs allow the converters to output an analog voltage corresponding to one digital word while holding the next, permitting simultaneous updating of multiple D/A's via a common strobe signal. The converters appear as a memory location or I/O port to the microprocessor and thus do not require interfacing logic. All models will operate as normal D/A's for non-microprocessor based applications.

Excellent temperature tracking characteristics are provided by precision silicon-chromium R-2R resistor ladder networks. Output settling time for a full-scale change to $\frac{1}{2}$ LSB, is as low as 500 nanoseconds and the maximum linearity error on all models is $\pm \frac{1}{2}$ LSB. Monotonicity is guaranteed over the full operating temperature range.

Other features include a low, 3 mV peak-to-peak, digital feedthrough error, 30 mW power dissipation and single supply operation. The reference input is selectable over a range of $\pm 10V$ and may also be used as the analog input for four quadrant multiplication applications.

The DAC-612C is packaged in a 24-pin ceramic DIP. Models DAC-608 and DAC-610 are packaged in a 20-pin plastic DIP. All units are specified to operate over the commercial $0^{\circ}C$ to $+70^{\circ}C$ temperature range. These devices are an ideal choice for innumerable applications involving industrial process control, programmable attenuators, audio signal processing and low frequency sine wave generation.

CAUTION: These devices contain CMOS circuits and should be handled with standard anti-static procedures.



INPUT/OUTPUT CONNECTIONS

DAC-608	
PIN	FUNCTION
1	CS (CHIP SELECT)
2	WR1 (WRITE 1)
3	ANALOG GROUND
4	DI3
5	DI2
6	DI1
7	DI0 (LSB)
8	REFERENCE IN
9	FEEDBACK
10	DIGITAL GROUND
11	OUTPUT 1
12	OUTPUT 2
13	DI7 (MSB)
14	DI6
15	DI5
16	DI4
17	XFER (Trans. Cont.)
18	WR2 (Write 2)
19	ILE (In. Latch ENB)
20	Vs

DAC-610	
PIN	FUNCTION
1	CS (CHIP SELECT)
2	WR (WRITE)
3	BYTE 1/BYTE 2
4	XFER
5	DI5
6	DI6
7	DI7
8	DI8
9	DI9 (MSB)
10	GROUND
11	OUTPUT 2
12	OUTPUT 1
13	REFERENCE IN
14	FEEDBACK
15	DI0 (LSB)
16	DI1
17	DI2
18	DI3
19	DI4
20	Vs

DAC-612	
PIN	FUNCTION
1	CS (CHIP SELECT)
2	WR1
3	ANALOG GROUND
4	DI5
5	DI4
6	DI3
7	DI2
8	DI1
9	DI0 (LSB)
10	REFERENCE IN
11	FEEDBACK
12	DIGITAL GROUND
13	OUTPUT 1
14	OUTPUT 2
15	DI11 (MSB)
16	DI10
17	DI9
18	DI8
19	DI7
20	DI6
21	XFER (Trans. Cont.)
22	WR2 (Write 2)
23	BYTE 1/BYTE 2
24	Vs

both internal registers to follow the applied digital inputs, directly affecting the device output.

6. For stand alone operation where control signals are generated by discrete logic, double buffering can be controlled by applying a logic "0" to CS and XFER and a logic "1" to ILE and pulling WR1 low to load data in the input latch. Pulling WR2 low will then update the analog output. A logic "1" on either of these lines will prevent the changing of the analog output.
7. All unused digital inputs should be tied

to V_S or ground in order to prevent damage to the chip from static discharge. If any of the digital inputs are inadvertently left floating, the D/A will interpret the pin as a logic "1".

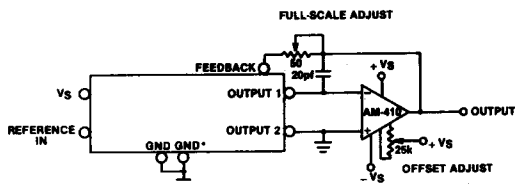
8. The input registers of the DAC-610 and DAC-612 are arranged to accept a left justified data word from the microprocessor with 8 bits coming first and the lower bits second. Left-justified means that the binary point is assumed to be located to the left of the most significant bit.
9. The use of good circuit board layout

techniques are required for rated performance. Minimization of lead lengths around analog circuitry is recommended. It is important that a good ground be used. A single point ground distribution technique for analog signals and supply returns will prevent other devices in the system from affecting the output of the D/A's. V_S should be bypassed as close to the V_S pin as possible with a low inductance $1 \mu F$ tantalum capacitor.

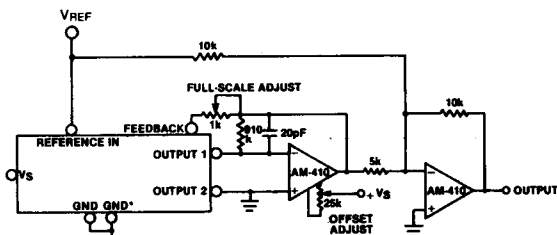
CODING AND CALIBRATION

CALIBRATION PROCEDURE

UNIPOLAR



UNIPOLAR CONFIGURATION



BIPOLAR CONFIGURATION

*ONE GROUND ON DAC-610

Zero Adjust—Set all data bits to logic "0" (logic "1" if using output 2) and adjust the OFFSET ADJUST pot on the external operational amplifier for 0.000V.

Full Scale—Set all data bits to logic "1" (logic "0" if using output 2) and set the FULL Scale ADJUST for an output equal to: $V_{out} = -V_{ref} (N - 1)/N$, where "N" is equal to: 256 (DAC-608), 1024 (DAC-610) or 4096 (DAC-612).

BIPOLAR

Zero Adjust—Set all data bits to logic "0" and adjust the OFFSET ADJUST for an output voltage equal to V_{ref} .

Full Scale—Set all data bits to logic "1" and adjust the FULL SCALE ADJUST for an output voltage equal to: $V_{out} = V_{ref} (N-X)/X$ where "N" is equal to: 255 (DAC-608), 1023 (DAC-610) or 4095 (DAC-612); and "X" is equal to: 128 (DAC-608), 512 (DAC-610) or 2048 (DAC-612).

OUTPUT CODING TABLES

UNIPOLAR OPERATION

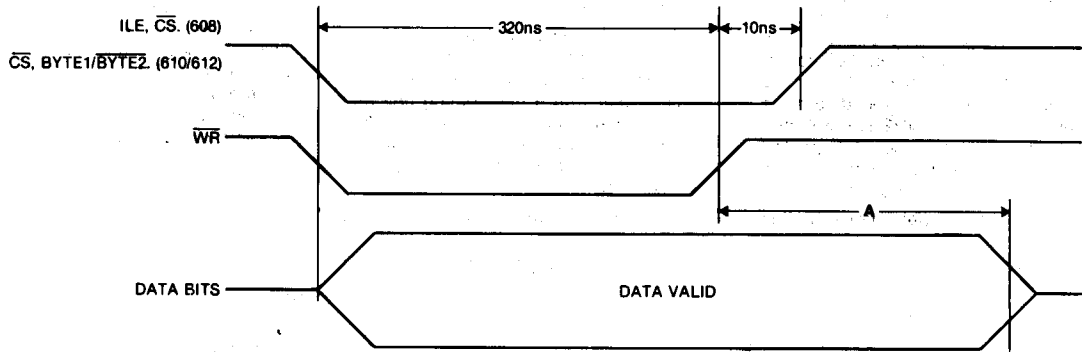
INPUT CODE		IDEAL OUTPUT
MSB	LSB	
111	111	$-(V_{REF} + 1 \text{ LSB})$
110	000	$-0.75 (V_{REF})$
100	000	$-0.5 (V_{REF})$
010	000	$-0.25 (V_{REF})$
000	000	0

BIPOLAR OPERATION

INPUT CODE		IDEAL OUTPUT	
MSB	LSB	+ V_{REF}	- V_{REF}
111	111	+ $V_{REF} - 1 \text{ LSB}$	- $V_{REF} + 1 \text{ LSB}$
110	000	$0.5 (+ V_{REF})$	$0.5 (- V_{REF})$
100	000	0	0
010	000	$0.5 (- V_{REF})$	$0.5 (+ V_{REF})$
000	000	- V_{REF}	+ V_{REF}

TIMING AND PERFORMANCE

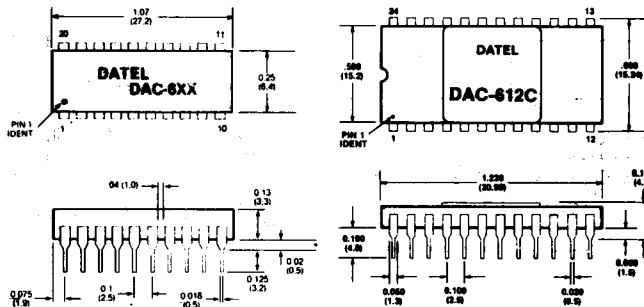
TIMING DIAGRAM



MODEL	A
DAC-608	90ns
DAC-610	200ns
DAC-612	90ns

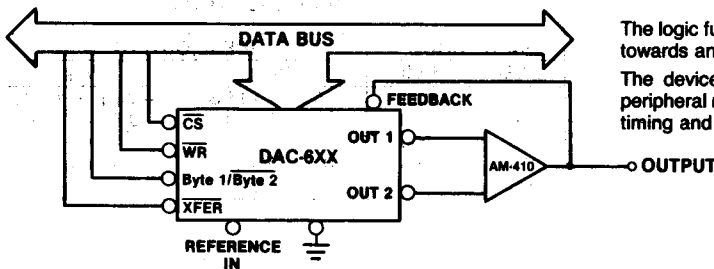
- NOTE:**
1. Settling time is measured from the leading edge of the WR pulse.
 2. All digital controls are level actuated.

**MECHANICAL DIMENSIONS
INCHES (MM)**



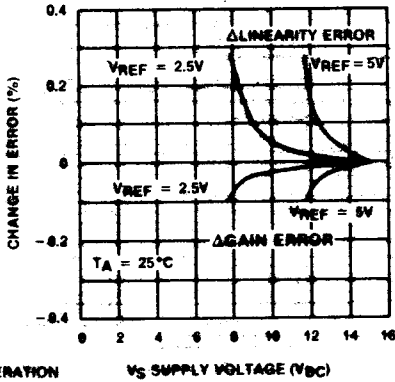
APPLICATIONS

Typical Connection to Popular Microprocessor Data Bus

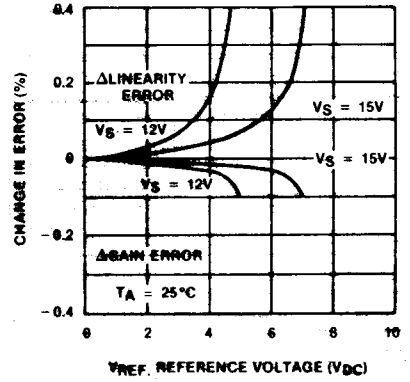


The logic functions of the DAC-608/610/612 have been oriented towards an ease of interface with all popular microprocessors. The devices are treated as a typical memory device or I/O peripheral requiring no external logic in most systems due to the timing and logic level convention of the input control signals.

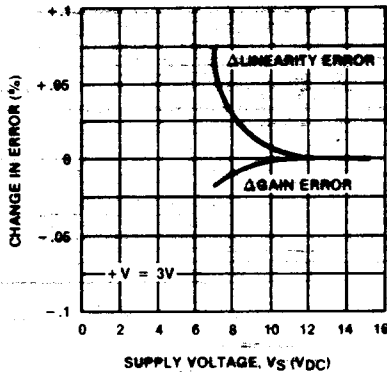
DAC-608 Gain and Linearity Error Variation vs. Supply Voltage



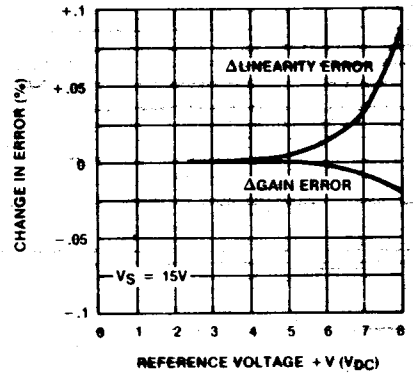
DAC-608 Gain and Linearity Error Variation vs. Reference Voltage



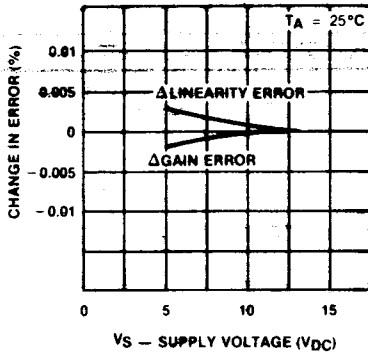
DAC-610 Gain and Linearity Error Variation vs. Supply Voltage



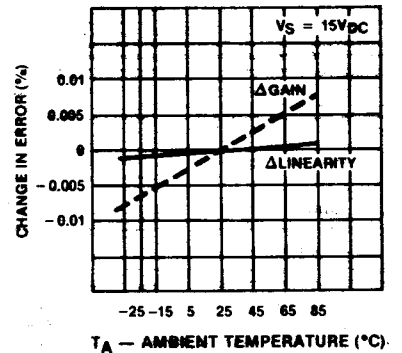
DAC-610 Gain and Linearity Error Variation vs. Reference Voltage



DAC-612 Gain and Linearity Error Variation vs. Supply Voltage

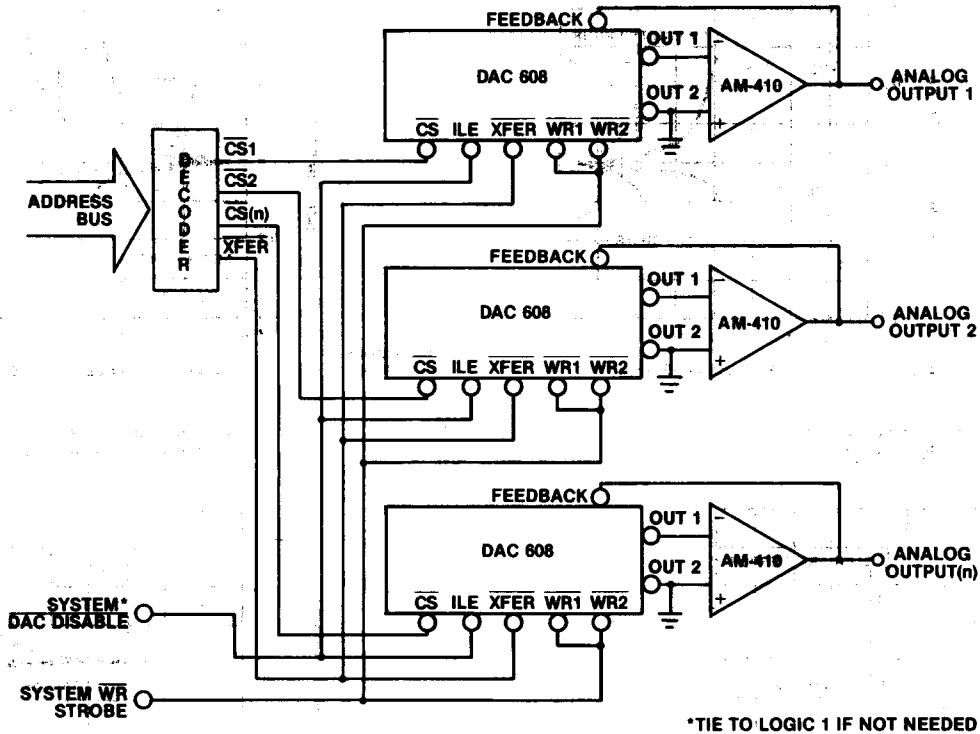


DAC-612 Gain and Linearity Error Variation vs. Temperature

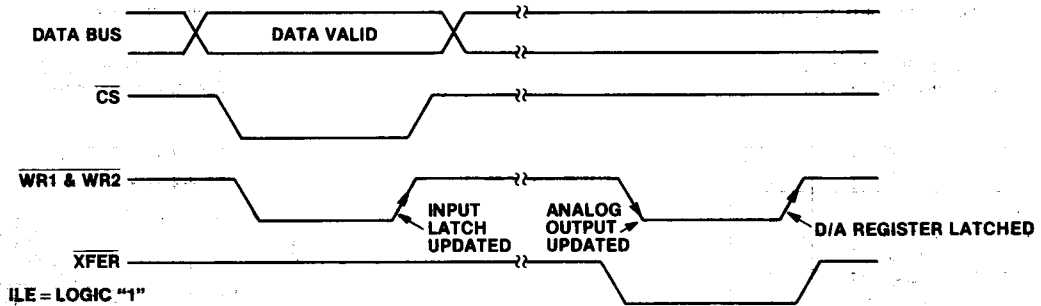


APPLICATIONS

MULTIPLE D/A SYSTEM



TIMING DIAGRAM



For simultaneous updating of multiple D/A's, the CS line of each device is decoded individually. However, the converter can share a common XFER.

The ILE function is very useful in applications where more than one processor is being used. If another processor took control of the data bus and control lines using the same addresses as the first, a low on the ILE pin would latch the data in the input register holding the outputs at their present state.

ORDERING INFORMATION

MODEL NO.	RESOLUTION	OPERATING TEMP. RANGE
DAC-608C	8 Bits	0°C to +70°C
DAC-610C	10 Bits	0°C to +70°C
DAC-612C	12 Bits	