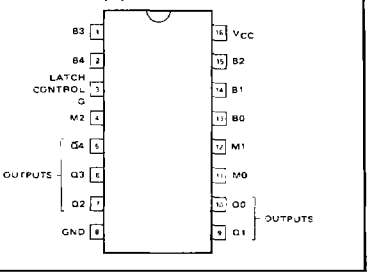
SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS B

PIN CONFIGURATION

B,F,W PACKAGE



DESCRIPTION

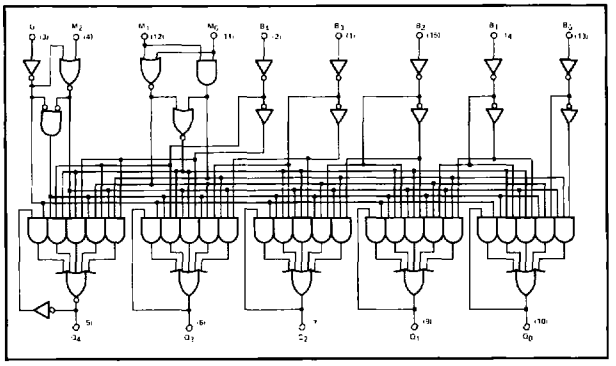
These low-power Schottky circuits are designed to be used in parallel multiplication applications. They perform binary multiplication in two's-complement form, two bits at a time.

The M inputs are for the multiplier bits and the B inputs are for the multiplicand. The Q outputs represent the partial product as a recoded base-4 number. This recoding effectively reduces the Wallace-tree hardware requirements by a factor of two.

The outputs represent partial products in one's-complement form generated as a result of multiplication. A simple rounding scheme using two additional gates is needed for each partial product to generate two's complement.

The leading (most significant) bit of the product is inverted for ease in extending the sign to square (left justify) the partial-product bits.

BLOCK DIAGRAM



FUNCTION TABLE

INPUTS				OUTPUTS				
LATCH CONTROL	MULTIPLIER							
G	M2	M1	M0	$\overline{Q4}$	Q3	Q2	Q1	Q0
L	X	X	X	$\overline{Q4}_0$	$Q3_0$	$Q2_0$	$Q1_0$	$Q0_0$
H	L	L	L	H	L	L	L	L
H	L	L	H	$\overline{B4}$	B4	B3	B2	B1
H	L	H	L	$\overline{B4}$	B4	B3	B2	B1
H	L	H	H	$\overline{B4}$	B3	B2	B1	B0
H	H	L	L	B4	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$	$\overline{B0}$
H	H	L	H	B4	$\overline{B4}$	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$
H	H	H	L	B4	B4	$\overline{B3}$	$\overline{B2}$	$\overline{B1}$
H	H	H	H	H	L	L	L	L

H = high level, L = low level, X = irrelevant
$\overline{Q4}_0 \ldots Q0_0$ = The logic level of the same output before the high-to-low- transition of G.
B4 . . . B0 = The logic level of the indicated multiplicand (b) input.

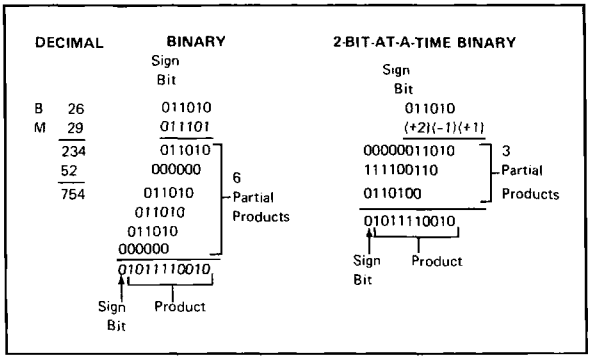
SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	LIMITS MIN	TYP	MAX	UNIT
t_w	Width of enable pulse				25			ns
t_{setup}	Input setup time							
		Any M input	Q		17↓			ns
		Any B input	Q		15↓			ns
t_{Hold}	Input hold time							
		Any M input	Q		0↓			ns
		Any B input	Q		0↓			ns
t_{PLH}	Propagation delay time Low-to-high-level output	Enable G	Any Q	C_L = 15pF, R_L = 2kΩ		22	35	ns
t_{PHL}	Propagation delay time High-to-low-level output	Enable G	Any Q			20	30	ns
t_{PLH}	Propagation delay time Low-to-high-level output	Any M input	Any Q			25	40	ns
t_{PHL}	Propagation delay time High-to-low-level output	Any M input	Any Q			22	35	ns
t_{PLH}	Propagation delay time Low-to-high-level output	Any B input	Any Q			27	42	ns
t_{PHL}	Propagation delay time High-to-low-level output	Any B input	Any Q			24	37	ns

Load circuits and typical waveforms are shown at the front of section.

TYPICAL APPLICATION DATA

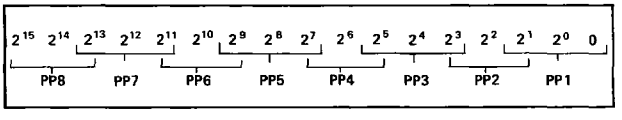
Multiplication of the numbers 26 (multiplicand) by 29 (multiplier) in decimal, binary, and 2-bit-at-a-time-binary is shown here:



Two points should be noted in the 2-bit-at-a-time-binary example above. First, in positioning the partial products beneath each other for final addition, each partial product is shifted two places to the left of the partial products above it instead of one place as is done in regular multiplication. Second, the msb of the partial product (the sign bit) is extended to the sign-bit column of the final answer. A substantial reduction of multiplication time, cost, and power is obtained by implementing a parallel partial-product-generation scheme using a 2-bit-at-a-time algorithm, followed by a Wallace Tree summation.

Partial-product-generation rules of the algorithm are:

1. Examine two bits of multiplier M plus the next lower bit. For the first partial product (PP1) the next lower bit is zero.



2. Generate partial product (PPi) as shown in the following table:
3. Weight the partial products by indexing each two places left relative to the next-less-significant product.
4. Extend the most-significant bit of the partial product to the sign-bit place value of the final product.

EXAMPLE OF ALGORITHM

M = 29 = 011101 — Operator Symbol — B = 26 = 011010

010 → +1B → 00000011010

110 → −1B → 111100110

011 → +2B → 0110100

The summation of these partial products was shown in the 2-bit-at-a-time binary multiplication example above.

The 54/74LS261 generates partial products according to this algorithm with two exceptions:

1. The one's complement is generated for the cases requiring the two's complement. The two's complement can be obtained by adding one to the one's complement; this rounding can be done by using one NAND gate and one AND gate as shown in Figure B.
2. The most-significant bit is complemented to reduce the hardware required to extend the sign bit. This extension can be accomplished by adding a hard-wired logic 1 in bit position 2^{2i+15} of each partial product and also in bit position 2^{16} of the first partial product (PP1).

MULTIPLER BITS FROM STEP 1			OPERATOR SYMBOL	TO OBTAIN PARTIAL PRODUCT
2^{2i-1}	2^{2i-2}	2^{2i-3}		
0	0	0	0	Replace multiplacand by zero
0	0	1	+1B	Copy multiplicand
0	1	0	+1B	Copy multiplicand
0	1	1	+2B	Shift multiplicand left one bit
1	0	0	−2B	Shift two's complement of multiplicand left one bit
1	0	1	−1B	Replace multiplicand by two's complement
1	1	0	−1B	Replace multiplicand by two's complement
1	1	1	0	Replace multiplicand by zero

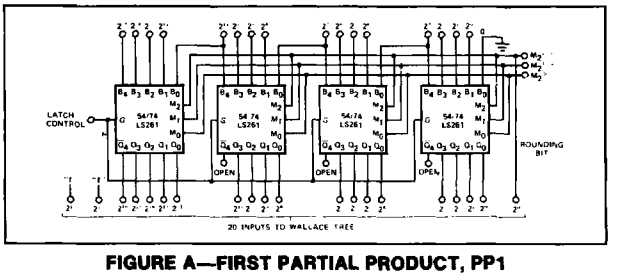


FIGURE A—FIRST PARTIAL PRODUCT, PP1

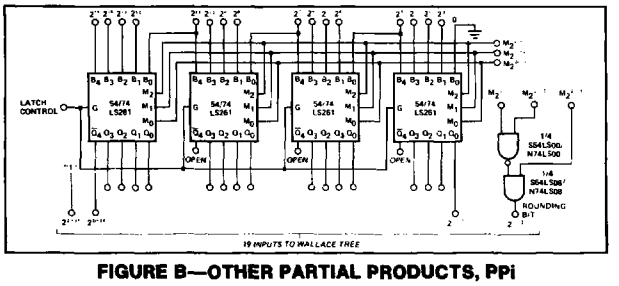


FIGURE B—OTHER PARTIAL PRODUCTS, PPi

LOGIC

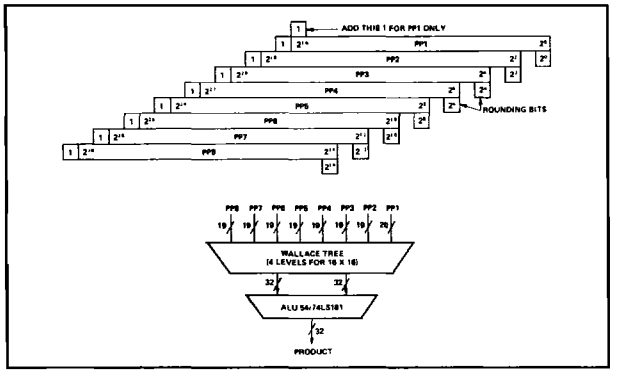


FIGURE C — MANIPULATION OF PARTIAL PRODUCTS FOR ENTRY INTO WALLACE TREE

In general, the 4 x 2 bit 54/74LS261 can be expanded for use in 4m x 2n bit multipliers. Partial-product generation uses m x n 54/74LS261s, m x n ÷ 16 54/74LS00s, and m x n ÷ 16 54/74LS08s. The size of the Wallace Tree and ALU requirements vary depending on the size of the problem. The count for the 16 x 16 bit multiplier is:

32	S54LS261/N74LS261
2	S54LS00/N74LS00
2	S54LS08/N74LS08
56	54H183/74H183*
7	S54LS181/N74LS181
2	S54LS182/N74LS182*

*Not currently available from Signetics.

QUAD 2-INPUT EXCLUSIVE-NOR GATE W/OPEN COLLECTOR OUTPUTS 54/74266

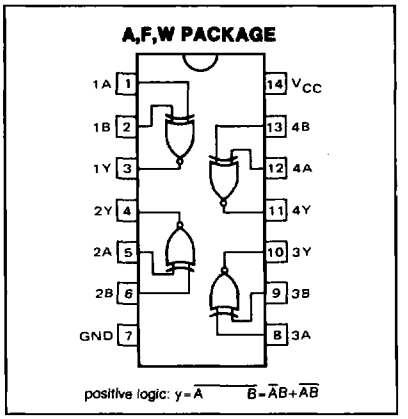
SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS A

DESCRIPTION

The 54/74LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for *multiple-bit comparisons.*

PIN CONFIGURATION



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

PARAMETER★	FROM (INPUT)	TEST CONDITIONS		LIMITS MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15pF,		18	30	ns
t_{PHL}			R_L = 2kΩ		18	30	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					18	30	

★t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Load circuit and waveforms are shown at the front of the book.

FUNCTION TABLE

INPUTS A	INPUTS B	OUTPUT Y
L	L	H
L	H	L
H	L	L
H	H	H

H = high level, L = low level