TC74HC192AP/AF
TC74HC193AP/AF/AFN

TC74HC192 Synchronous Up/Down Decade Counter
TC74HC193 Synchronous Up/Down Binary Counter

The TC74HC192A/193A are high speed CMOS SYNCHRONOUS 4-BIT UP/DOWN COUNTER fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

They have a clear input (CLEAR), a load input ($\overline{LOAD}$), load data inputs (A ~ D), two clock inputs (QA ~ QD), and other outputs ($\overline{CARRY}$, $\overline{BORROW}$).

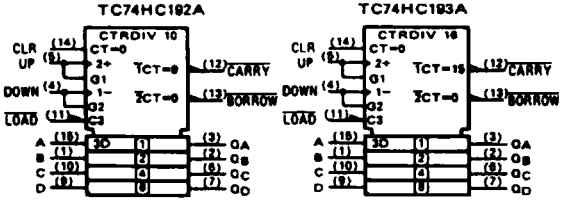
CLEAR is active high and forces Q_A through Q_D outputs low independent of the other inputs.

$\overline{CARRY}$ and $\overline{BORROW}$ outputs are provided in order to make a cascade connection without external circuitry.

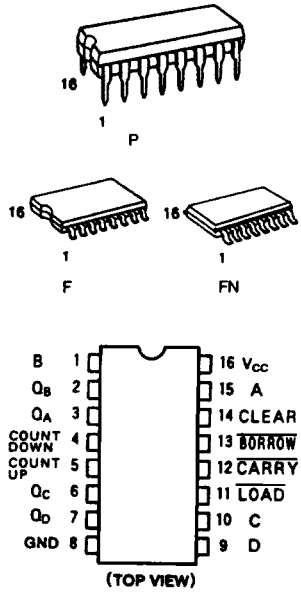
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features

- High Speed: f_{MAX} = 54MHz(Typ). at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ 28% V_{CC}(Min)
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS192/193



IEC Logic Symbol



Pin Assignment

Truth Table

Inputs				Function
Count Up	Count Down	Load	Clear	
⌐	H	H	L	Count Up
⌐	H	H	L	No Count
H	⌐	H	L	Count Down
H	⌐	H	L	No Count
X	X	L	L	Preset
X	X	X	H	Reset

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0~1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0~400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40 ~ 85°C Min.	Ta = -40 ~ 85°C Max.	Unit
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.5 3.15 4.2	– – –	– – –	1.5 3.15 4.2	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.5 1.35 1.8	– – –	0.5 1.35 1.8	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	– – –	1.9 4.4 5.9	– – –	V
			I_{OH} = -4 mA I_{OH} = 5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.0	0.1 0.1 0.1	– – –	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
3-State Output Off-State Current	I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		6.0	–	–	±0.5	–	±0.5	μA
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	4.0	–	40.0	

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (CLOCK)	$t_{W(H)}$ $t_{W(L)}$	–	2.0 4.5 6.0	– – –	100 20 17	125 25 21	ns
Minimum Pulse Width ($\overline{LOAD}$)	$t_{W(L)}$	–	2.0 4.5 6.0	– – –	75 15 13	95 19 16	
Minimum Hold Time (CLEAR)	$t_{W(H)}$	–	2.0 4.5 6.0	– – –	100 20 17	125 25 21	
Minimum Set-up Time (DATA-$\overline{LOAD}$)	t_s	–	2.0 4.5 6.0	– – –	75 15 13	95 19 16	
Minimum Hold Time (DATA-$\overline{LOAD}$)	t_h	–	2.0 4.5 6.0	– – –	0 0 0	0 0 0	
Minimum Removal Time ($\overline{LOAD}$)	t_{rem}	–	2.0 4.5 6.0	– – –	50 10 9	65 13 10	
Minimum Removal Time (CLEAR)	t_{rem}	–	2.0 4.5 6.0	– – –	50 10 9	65 13 10	
Clock Frequency	f	–	2.0 4.5 6.0	– – –	5 25 29	4 20 24	MHz

AC Electrical Characteristics (C_L = 15pF, V_{CC} = 5V, Ta = 25°C)

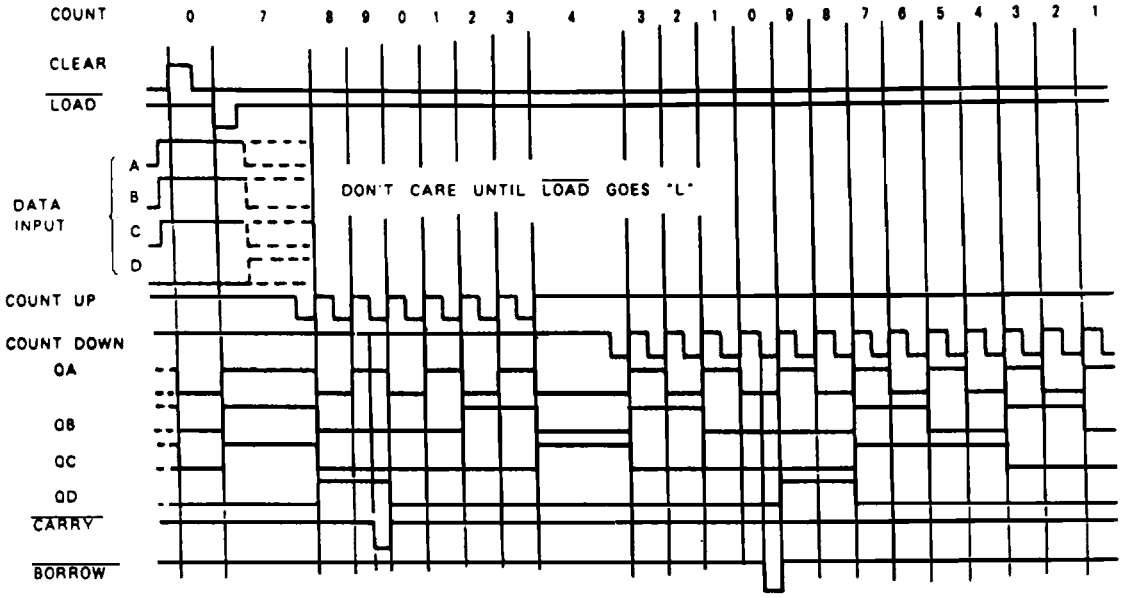
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	–	–	6	12	ns
Propagation Delay Time (UP, DOWN-Q)	t_{pLH} t_{pHL}	–	–	16	33	
Propagation Delay Time (UP-$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}	–	–	10	22	
Propagation Delay Time (DOWN-$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}	–	–	10	22	
Propagation Delay Time ($\overline{\text{LOAD}}$-Q)	t_{pLH} t_{pHL}	–	–	21	38	
Propagation Delay Time ($\overline{\text{LOAD}}$-$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}	–	–	25	44	
Propagation Delay Time ($\overline{\text{LOAD}}$-$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}	–	–	26	44	
Propagation Delay Time (DATA IN-Q)	t_{pLH} t_{pHL}	–	–	21	33	
Propagation Delay Time (DATA IN-$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}	–	–	29	44	
Propagation Delay Time (DATA IN-$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}	–	–	26	44	
Propagation Delay Time (CLEAR-Q)	t_{pHL}	–	–	25	39	
Propagation Delay Time (CLEAR-$\overline{\text{CARRY}}$)	t_{pLH}	–	–	30	44	
Propagation Delay Time (CLEAR-$\overline{\text{BORROW}}$)	t_{pHL}	–	–	30	44	
Maximum Clock Frequency	f_{MAX}	–	27	52	–	MHz

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6ns)

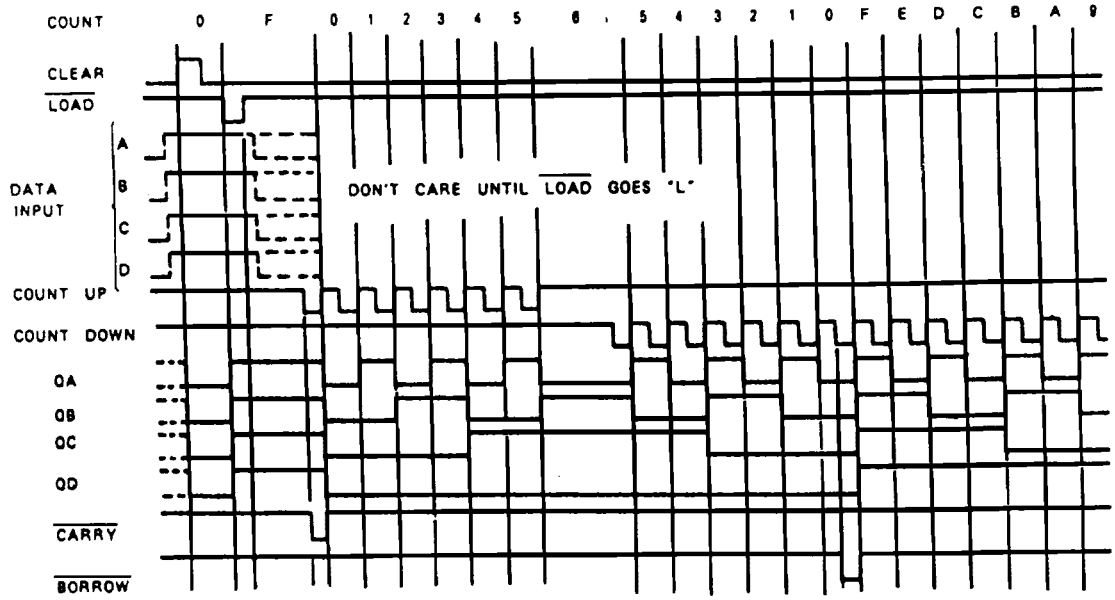
Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC}	Min	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time (UP, DOWN-Q)	t_{pLH} t_{pHL}	–	2.0	–	65	190	–	240	
			4.5	–	20	38	–	48	
			6.0	–	16	32	–	41	
Propagation Delay Time (UP-$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}	–	2.0	–	40	130	–	165	
			4.5	–	13	26	–	33	
			6.0	–	11	22	–	28	
Propagation Delay Time (DOWN-$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}	–	2.0	–	40	130	–	165	
			4.5	–	13	26	–	33	
			6.0	–	11	22	–	28	
Propagation Delay Time ($\overline{\text{LOAD}}$-Q)	t_{pLH} t_{pHL}	–	2.0	–	85	220	–	275	
			4.5	–	25	44	–	55	
			6.0	–	20	37	–	47	
Propagation Delay Time ($\overline{\text{LOAD}}$-$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}	–	2.0	–	110	250	–	315	
			4.5	–	30	50	–	63	
			6.0	–	25	43	–	54	
Propagation Delay Time ($\overline{\text{LOAD}}$-$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}	–	2.0	–	110	250	–	315	
			4.5	–	30	50	–	63	
			6.0	–	25	43	–	54	
Propagation Delay Time (DATA IN-Q)	t_{pLH} t_{pHL}	–	2.0	–	80	190	–	240	
			4.5	–	25	38	–	48	
			6.0	–	20	32	–	41	
Propagation Delay Time (DATA IN-$\overline{\text{CARRY}}$)	t_{pLH} t_{pHL}	–	2.0	–	120	250	–	315	
			4.5	–	34	50	–	63	
			6.0	–	28	43	–	54	
Propagation Delay Time (DATA IN-$\overline{\text{BORROW}}$)	t_{pLH} t_{pHL}	–	2.0	–	110	250	–	315	
			4.5	–	31	50	–	63	
			6.0	–	25	43	–	54	
Propagation Delay Time (CLEAR-Q)	t_{pHL}	–	2.0	–	100	225	–	280	
			4.5	–	30	45	–	56	
			6.0	–	25	38	–	48	
Propagation Delay Time (CLEAR-$\overline{\text{CARRY}}$)	t_{pLH}	–	2.0	–	120	250	–	315	
			4.5	–	35	50	–	63	
			6.0	–	29	43	–	54	
Propagation Delay Time (CLEAR-$\overline{\text{BORROW}}$)	t_{pHL}	–	2.0	–	120	250	–	315	
			4.5	–	35	50	–	63	
			6.0	–	29	43	–	54	
Maximum Clock Frequency	f_{MAX}	–	2.0	5	12	–	4	–	MHz
			4.5	25	48	–	20	–	
			6.0	29	55	–	24	–	
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	TC74HC192A		–	68	–	–	–	
		TC74HC193A		–	67	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

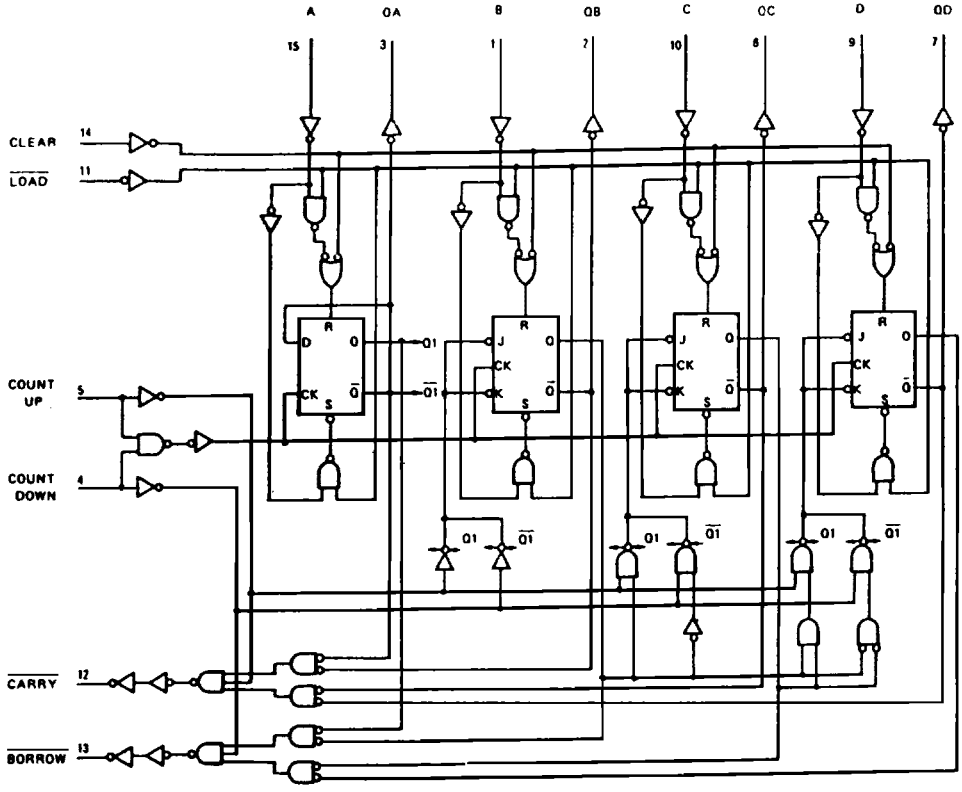
$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$



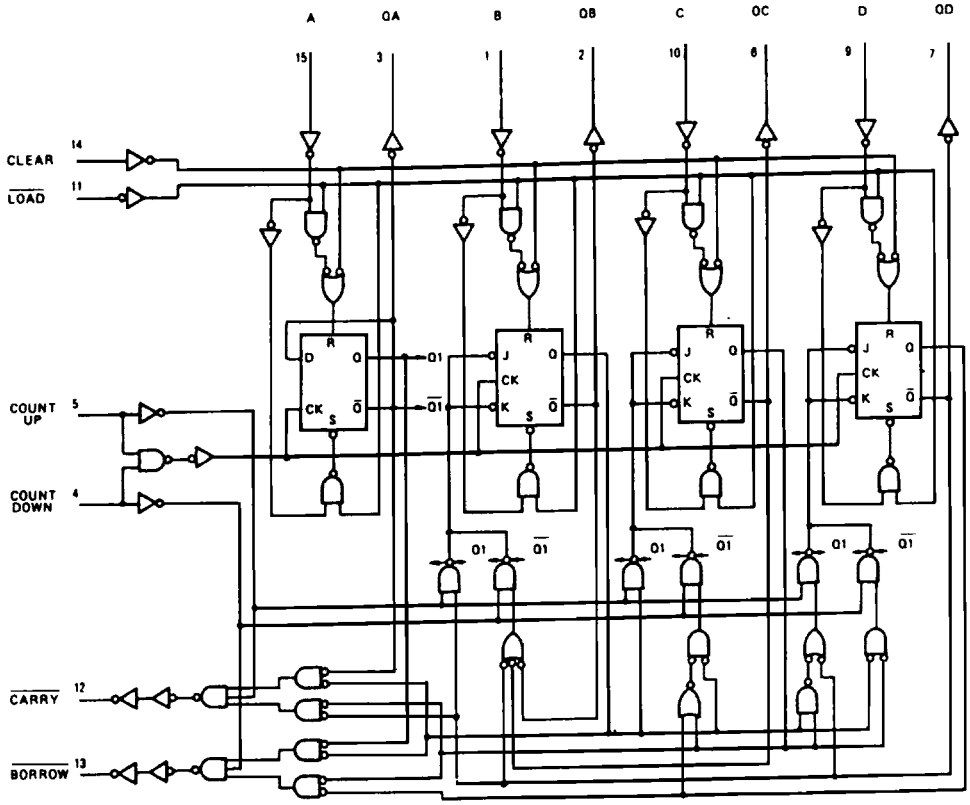
Timing Chart (YC74HC192A)



Timing Chart (TC74HC193A)



Logic Diagram (TC74HC192A)



Logic Diagram (TC74HC193A)