MC-421000A9
1,048,576 x 9-Bit
CMOS Dynamic RAM Module

Description

The MC-421000A9 is a fast-page, 1,048,576-word by 9-bit CMOS dynamic RAM module, designed to operate from a single +5 volt power supply. Advanced CMOS circuitry, including a single-transistor storage cell, 2048 sense amplifiers per data output, multiplexed address buffers and flexible refresh controls, provides good system operating margins.

The MC-421000A9 is functionally equivalent to eight μPD421000 standard 1M DRAMs plus a parity bit. Refreshing is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 512 address combinations of A_0-A_8 during an 8-ms period.

The Single Inline Memory Module (SIMM™) package reduces system cost, enhances reliability, and reduces the size and weight of a system. The SIMM includes nine μPD421000s in SOJ packages and nine power supply decoupling capacitors.

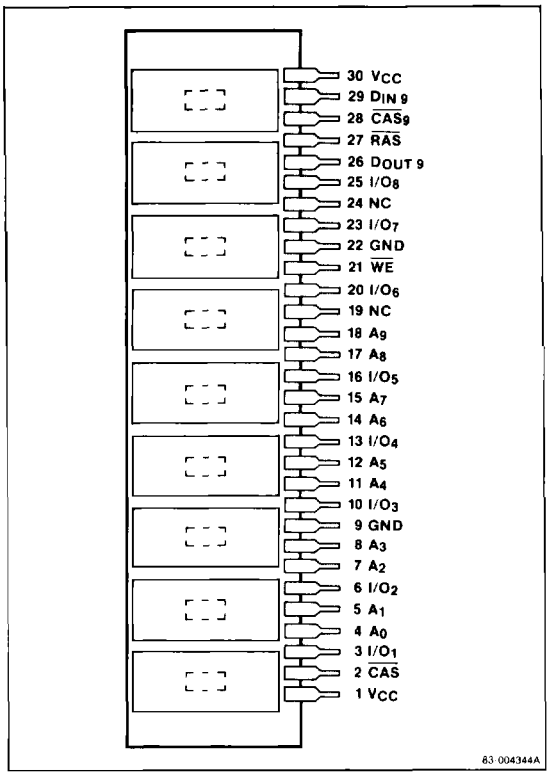
SIMM is a trademark of Wang Laboratories.

Features

- ☐ 1,048,576-word by 9-bit organization
- ☐ Single +5 V ± 10% power supply
- ☐ Standard 30-pin Single Inline Memory Module (SIMM) packaging
- ☐ Incorporates nine 1M dynamic RAMs in high-density SOJ packaging (μPD421000LA)
- ☐ Includes power supply decoupling capacitors
- ☐ Low power dissipation: 49.5 mW standby (max)
- ☐ TTL-compatible I/O
- ☐ 512 refresh cycles (A_0-A_8 are refresh address pins)
- ☐ Fast-page capability

Pin Configurations

30-Pin SIMM, MC-421000A9A



Ordering Information

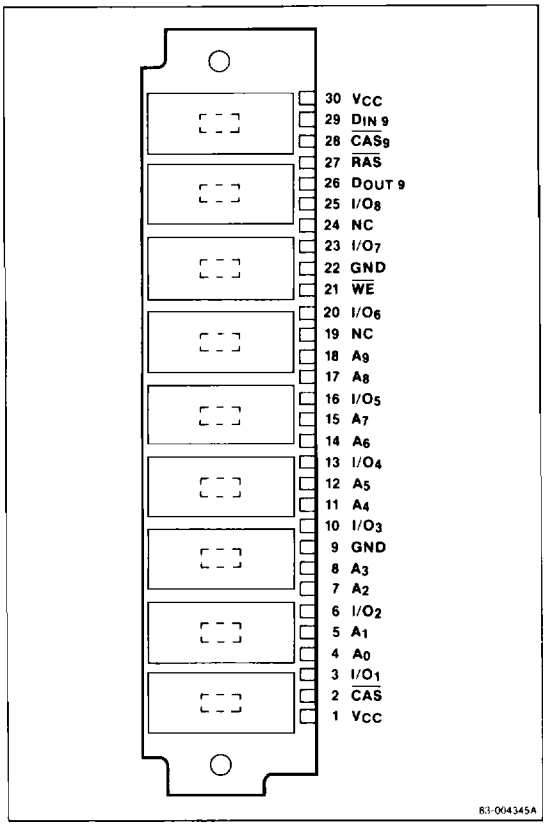
Part Number	Row Access Time (max)	Column Access Time (max)	Fast-Page Cycle Time (min)	Package
MC-421000A9A-70	70 ns	20 ns	45 ns	30-pin leaded SIMM
A-80	80 ns	20 ns	50 ns	
A-10	100 ns	25 ns	60 ns	
A-12	120 ns	30 ns	70 ns	
MC-421000A9B-70	70 ns	20 ns	45 ns	30-pin socketable SIMM
B-80	80 ns	20 ns	50 ns	
B-10	100 ns	25 ns	60 ns	
B-12	120 ns	70 ns	65 ns	

Notes:

(1) Contact your NEC sales representative for a copy of the MC-421000A9A-70 and MC-421000A9B-70 data sheets.

Pin Configurations (cont)

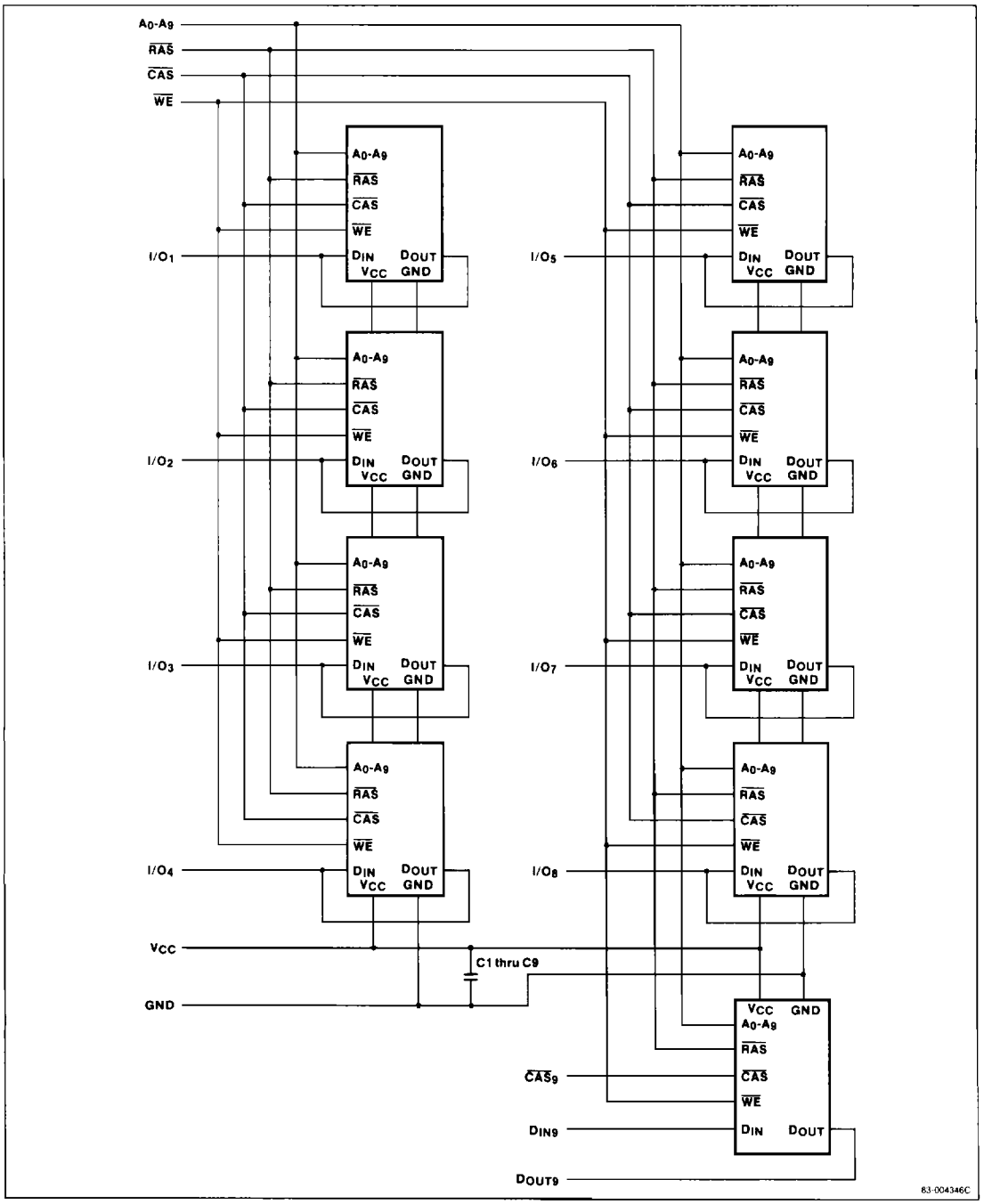
30-Pin SIMM, MC-421000A9B



Pin Identification

Symbol	Function
A_0-A_9	Address inputs
I/O_1-I/O_8	Common data inputs/outputs
$D_{IN\ 9}$	Data input 9
$D_{OUT\ 9}$	Data output 9
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{CAS_9}$	Column address strobe for data output 9
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Block Diagram



Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	9.0 W

Comment: Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	70	pF	A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
	C_{I2}	7	pF	$\overline{CAS}_9$, D_{IN9}
Input/output capacitance	C_D	15	pF	I/O_1-I/O_8
Output capacitance	C_O	10	pF	$D_{OUT\,9}$

DC Characteristics

T_A = 0 to +70°C; V_{CC} = 5 V ±10%; GND = 0 V

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			27	mA	$\overline{RAS} = \overline{CAS} \geq V_{IH}$
				9	mA	$\overline{RAS} = \overline{CAS} \geq V_{CC}$ −0.2 V
Input leakage current	I_{IL}	−90		90	μA	For A_0-A_9, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Input leakage current	I_{IL9}	−10		10	μA	For $\overline{CAS}_9$, $D_{IN\,9}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1-I/O_8 and $D_{OUT\,9}$: D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

		Limits							
		MC-421000A9-80		MC-421000A9-10		MC-421000A9-12			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		630		540		450	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ min (Note 5)
Operating current, refresh cycle, average	I_{CC3}		630		540		450	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$, $t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Fast-page operating current, average	I_{CC4}		540		450		360	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ min; I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refreshing, average	I_{CC5}		630		540		450	mA	$t_{RC} = t_{RC}$ min; I_O = 0 mA (Note 5)
Random read or write cycle time	t_{RC}	160		190		220		ns	(Note 6)
Read-write cycle time	t_{RWC}	190		225		260		ns	(Notes 6, 20)
Fast-page cycle time	t_{PC}	50		60		70		ns	(Note 6)
Refresh period	t_{REF}		8		8		8	ms	
Access time from $\overline{RAS}$	t_{RAC}		80		100		120	ns	(Notes 7, 8)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		25		30	ns	(Notes 7, 9, 10, 11)
Access time from column address	t_{AA}		45		50		60	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		45		55		65	ns	(Notes 7, 11)
Output buffer turnoff delay	t_{OFF}	0	20	0	25	0	30	ns	(Note 12)
Transition time (rise and fall)	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		80		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	120	10000	ns	
Fast-page $\overline{RAS}$ pulse width	t_{RASP}	80	100000	100	100000	120	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20		25		30		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	25	10000	30	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		100		120		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	60	25	75	25	90	ns	(Note 13)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 14)
$\overline{CAS}$ precharge time (non-page mode)	t_{CPN}	10		10		15		ns	
Fast-page $\overline{CAS}$ precharge time	t_{CP}	10	20	10	25	15	30	ns	(Note 11)
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	12		12		15		ns	
$\overline{RAS}$ to column address delay time	t_{RAD}	17	35	17	50	20	60	ns	(Note 10)
Column address setup time	t_{ASC}	0	20	0	20	0	25	ns	(Note 11)
Column address hold time	t_{CAH}	20		20		25		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	60		70		85		ns	

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AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%

Parameter	Symbol	Limits MC-421000A9-80 Min	Max	MC-421000A9-10 Min	Max	MC-421000A9-12 Min	Max	Unit	Test Conditions
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	45		55		65		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 15)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 15)
Write command hold time	t_{WCH}	15		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	55		70		85		ns	
Write command pulse width	t_{WP}	15		20		25		ns	(Note 16)
Write command to $\overline{RAS}$ lead time	t_{RWL}	25		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		25		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 17)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		70		85		ns	
Write command setup time	t_{WCS}	0		0		0		ns	(Note 18)
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	20		25		30		ns	(Notes 18, 20)
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80		100		120		ns	(Notes 18, 20)
Column address to $\overline{WE}$ delay time	t_{AWD}	45		55		65		ns	(Notes 18, 20)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CSR}	10		10		10		ns	(Note 19)
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refreshing	t_{CHR}	15		20		25		ns	(Note 19)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (−1 mA, +4 mA) loads and 100 pF (V_{OH} = 2.0 V, V_{OL} = 0.8 V).

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) For fast-page read operation, the definition of access time is as follows.

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} > t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

Notes [cont]:

(12) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(13) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), access time is controlled exclusively by t_{CAC}.

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) For $D_{OUT\ 9}$, parameters t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of $D_{OUT\ 9}$ (at access time and until $\overline{CAS}_9$ returns to V_{IH}) is indeterminate.

(19) $\overline{CAS}$ before $\overline{RAS}$ operation is specified.

(20) Read-write/read-modify-write operation can be performed only by the SOJ controlled by $\overline{CAS}_9$ because of its separate data input and output pins.

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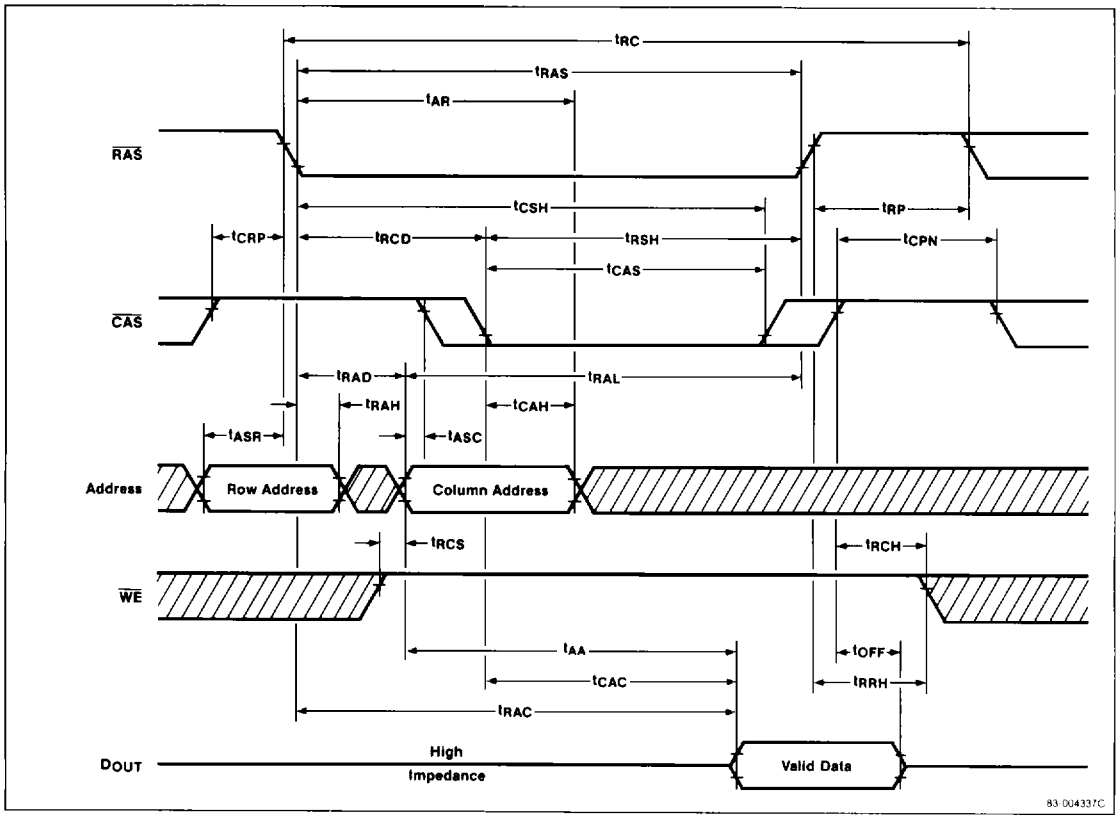
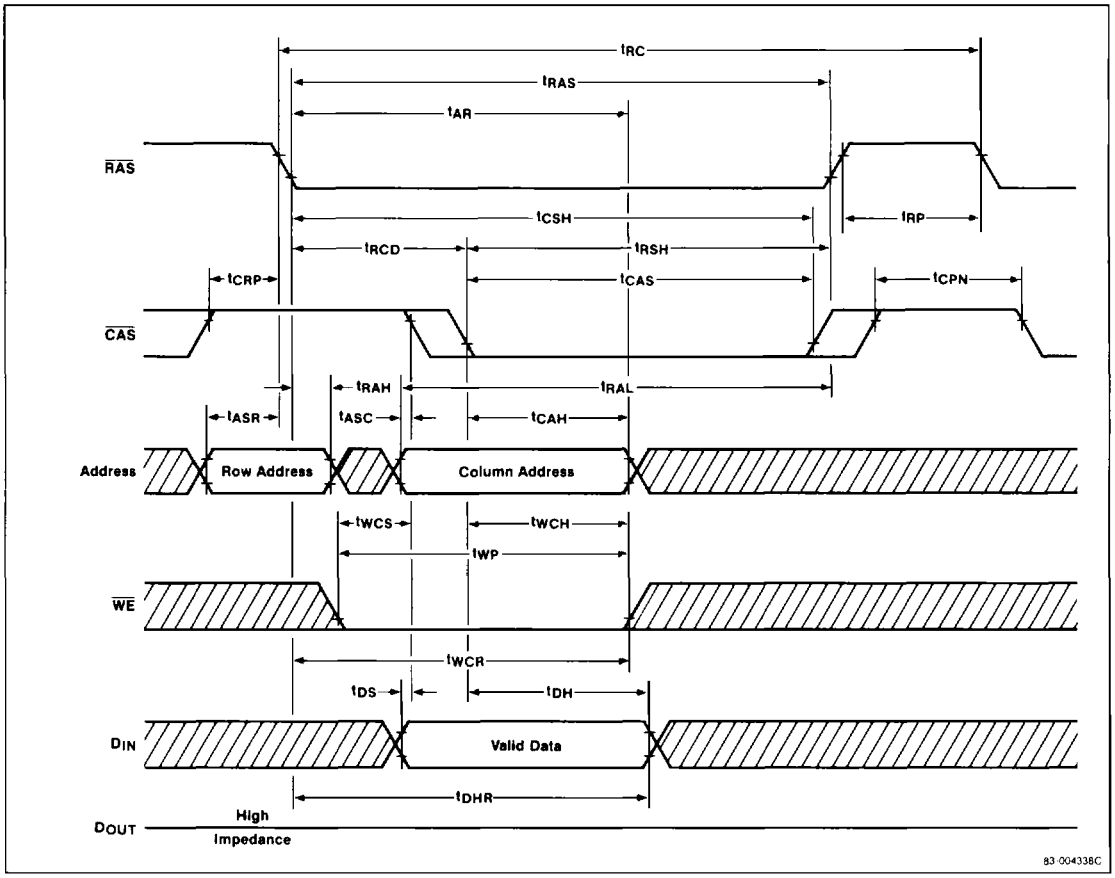
Timing Waveforms

Read Cycle



Timing Waveforms (cont)

Write Cycle (Early Write)



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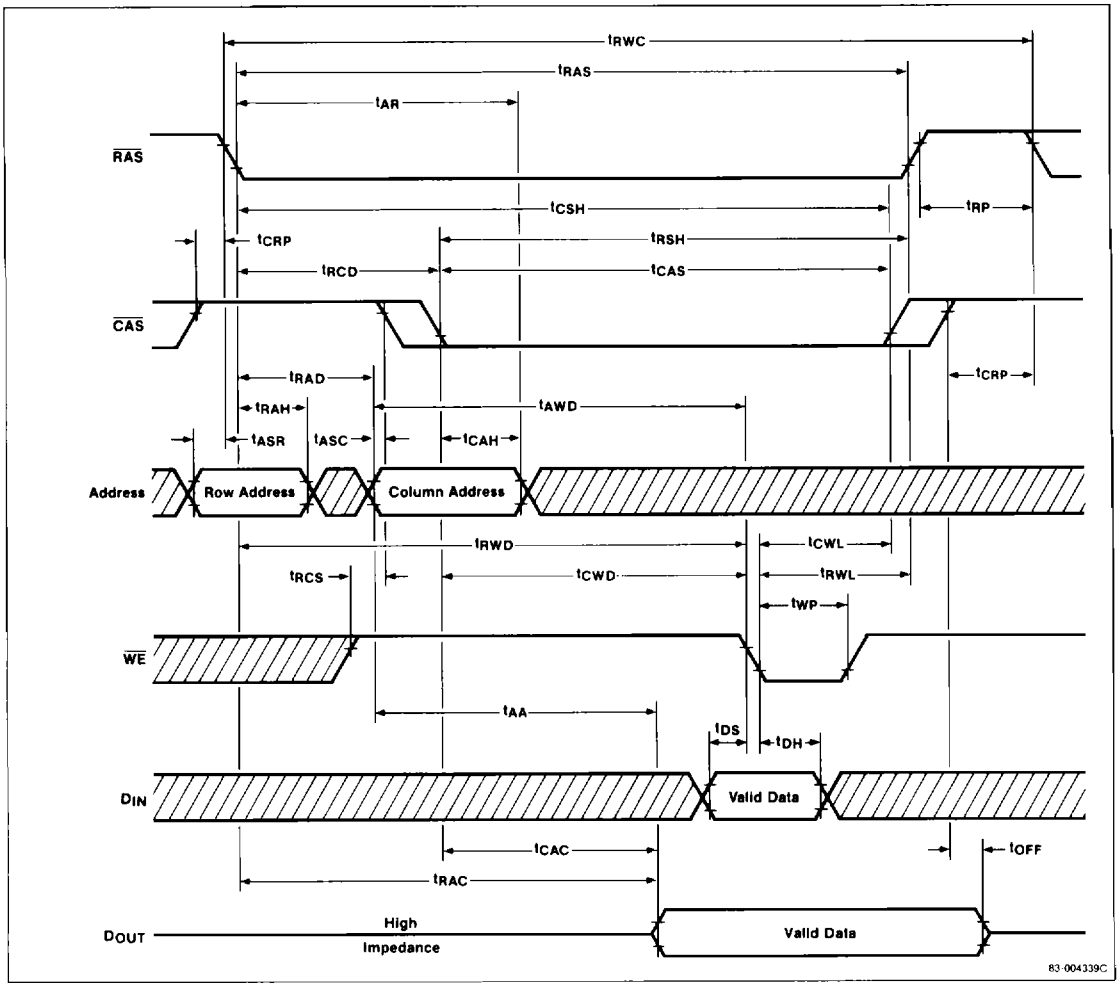
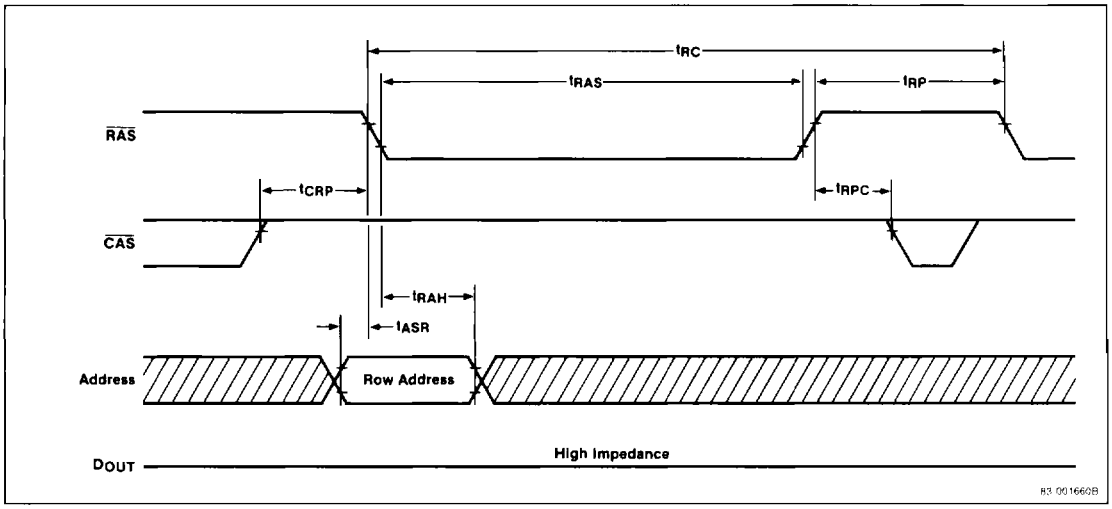
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle (D_{OUT} 9 only)



Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



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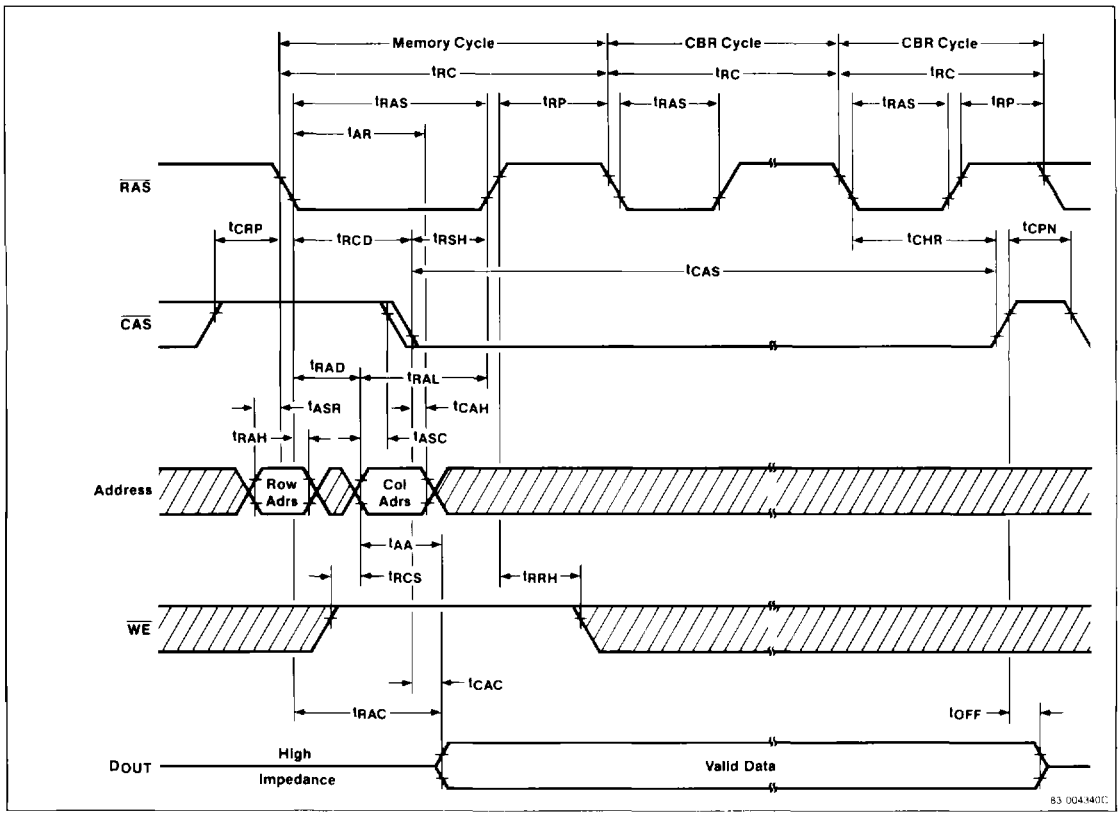
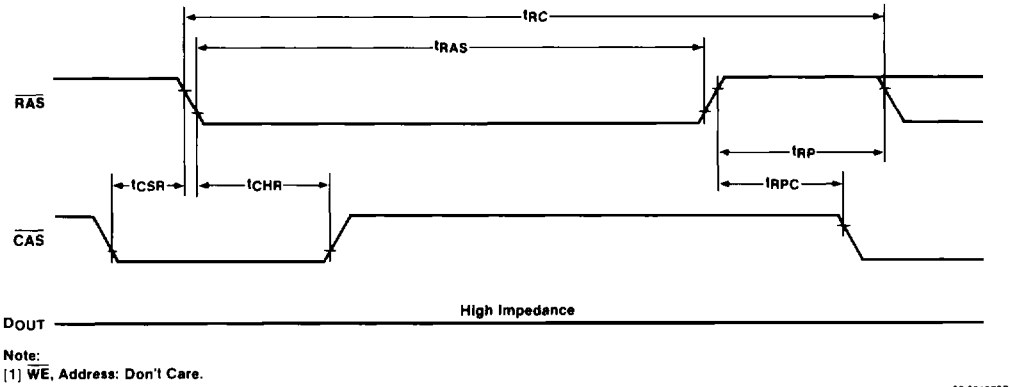
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$, Address: Don't Care.

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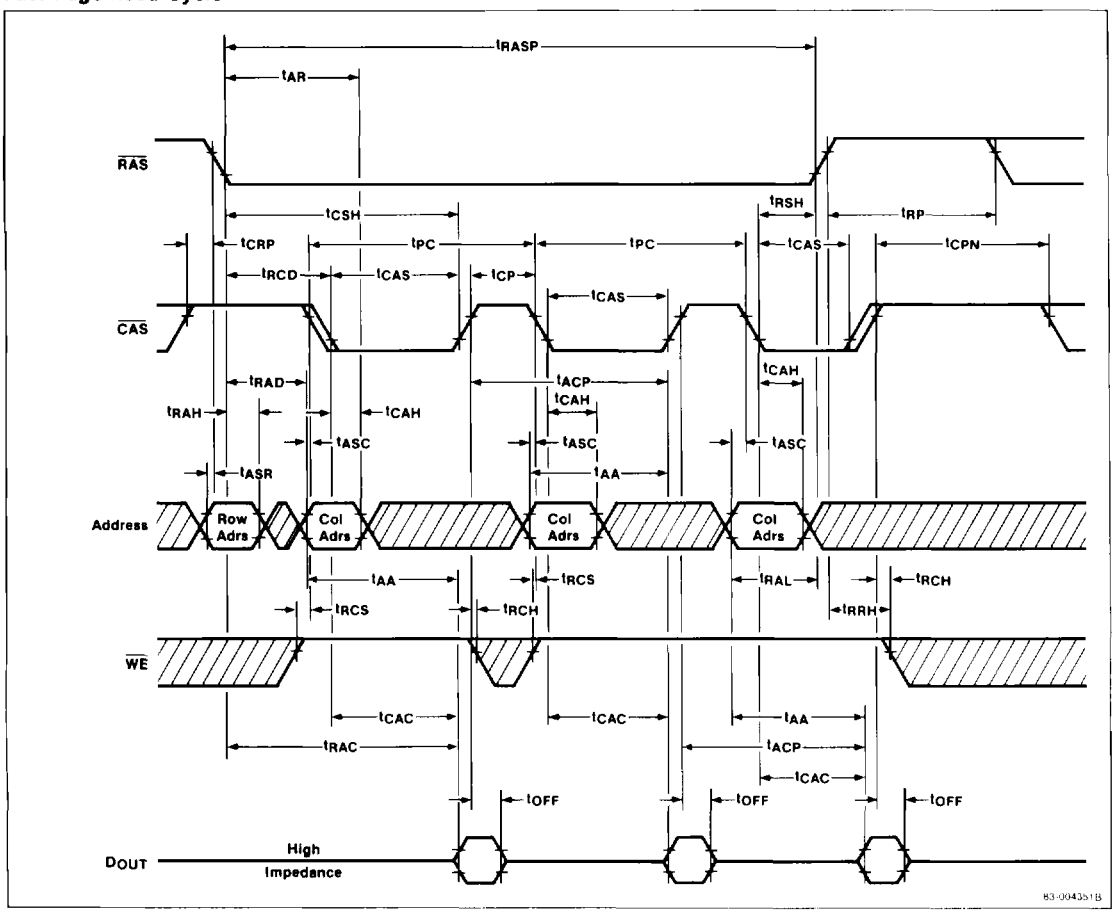
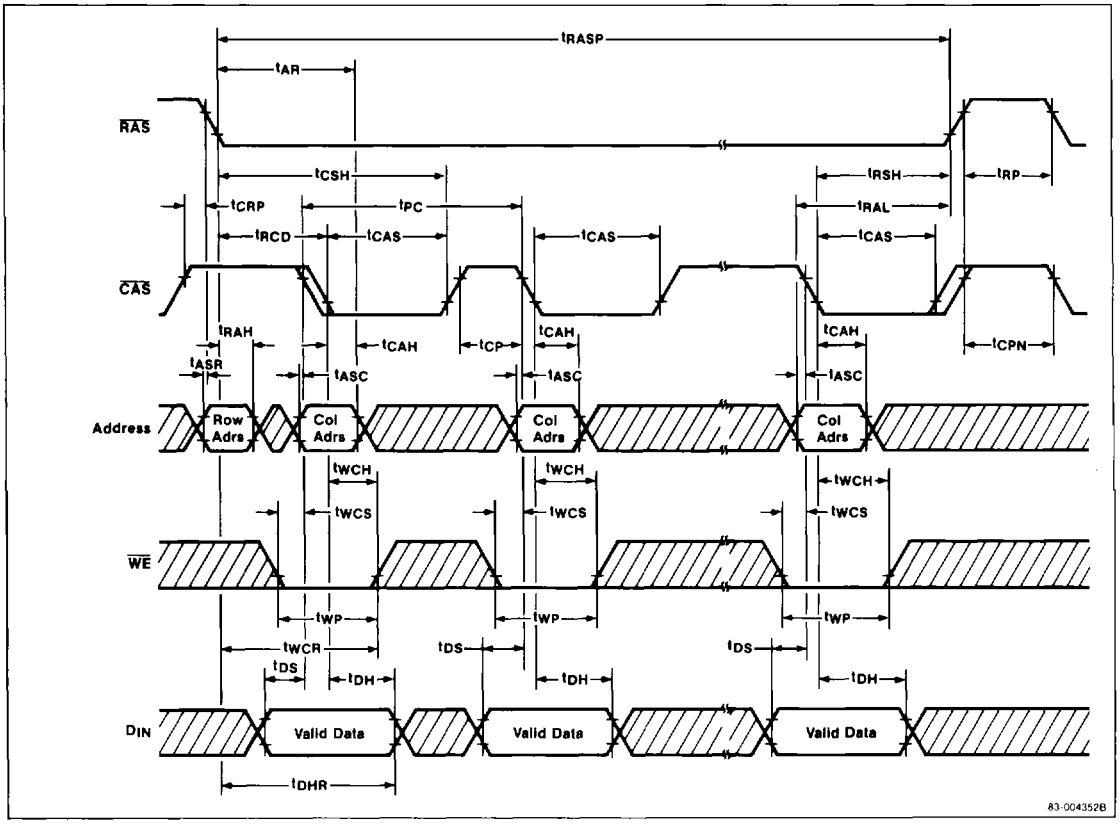
Timing Waveforms (cont)

Fast-Page Read Cycle



Timing Waveforms (cont)

Fast-Page Write Cycle (Early Write)



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Timing Waveforms (cont)

Fast-Page Read-Write/Read-Modify-Write Cycle (D_{OUT} only)