MOTOROLA

MC74F2960/ Am2960 MC74F2960A

ERROR DETECTION AND CORRECTION CIRCUIT

ADVANCED LOW POWER SCHOTTKY

Advance Information

ERROR DETECTION AND CORRECTION CIRCUIT

The MC74F2960 will be dual marked with the AMD part number Am2960 to indicate plug-in compatibility. However, the device will be referred to as the MC74F2960 in the remainder of this specification. The MC74F2960A is a high speed version of MC74F2960 and is a plug-in replacement for MC74F2960 where higher performance is required.

DESCRIPTION — The MC74F2960 and MC74F2960A Error Detection and Correction Units (EDAC) contain the logic necessary to generate check bits on a 16-bit data field according to a modified Hamming Code, and to correct the data word when check bits are supplied. Operating on data read from memory, the MC74F2960 and MC74F2960A will correct any single bit error* and will detect all double and some triple bit errors. For 16-bit words, 6 check bits are used. The MC74F2960 and MC74F2960A are expandable to operate on 32-bit words (7 check bits) and 64-bit words (8 check bits). In all configurations, the device makes the error syndrome available on separate outputs for data logging.

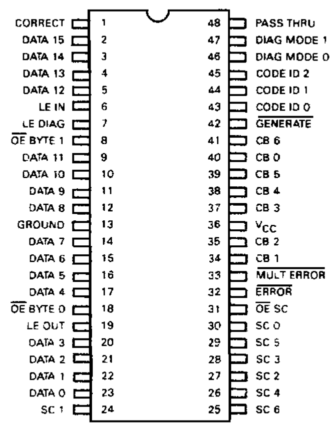
The MC74F2960 and MC74F2960A also feature two diagnostic modes, in which diagnostic data can be forced into portions of the chip to simplify device testing and to execute system diagnostic functions. The product will be supplied in a 48-lead DIP package.

*Double bit errors can also be corrected if at least one of the two errors is a hard error. This requires extra processor cycles.

- **PIN AND FUNCTIONALLY COMPATIBLE WITH THE Am2960**
- **BOOSTS MEMORY RELIABILITY**
- **EXPANDABLE TO 64-BIT DATA WORDS**
- **BUILT-IN DIAGNOSTICS PERMITS SOFTWARE SYSTEM CHECK**
- **SEPARATE BYTE CONTROLS FACILITATE BYTE OPERATIONS**
- **COMPATIBLE WITH MC68000 AND OTHER PROCESSORS**

16-Bit Timing (Worst Case)	74F2960	74F2960A	Units
Check Bit Generation	32	20	ns
Single Error Detection	32	19	ns
Single Error Correction	65	42	ns

CONNECTION DIAGRAM
Top View



J Suffix — Case 740-03 (Ceramic)
N Suffix — Case 767-02 (Plastic)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 1 — BLOCK DIAGRAM

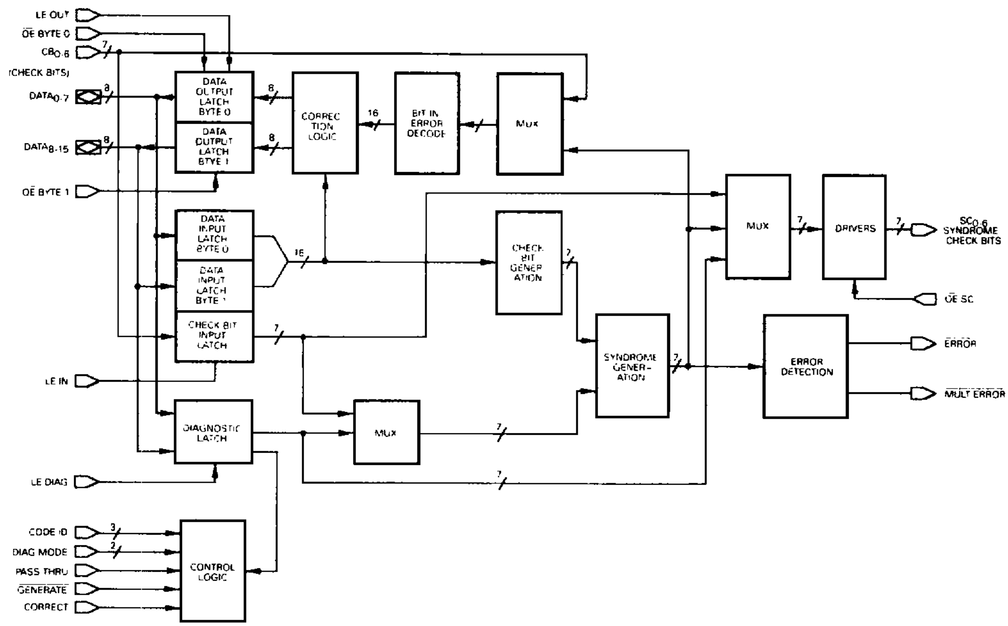


TABLE 1. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage (Except $DATA_{0-15}$)	V_{in}	−0.5 to +7.0	V
Input Voltage ($DATA_{0-15}$)	V_{in}	−0.5 to +5.5	V
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

TABLE 2. GUARANTEED OPERATING RANGES (θ_{JC} = 6°C/Watt)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current — High			−0.8	mA
I_{OL}	Output Current — Low			8.0	mA

Operating ranges define those limits over which the functionality of the device is guaranteed.

TABLE 3. DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS			UNITS	TEST CONDITIONS
			MIN	TYP	MAX		
V_{IH}	Input HIGH Voltage (1)		2.0			V	Guaranteed Input HIGH Voltage
V_{IL}	Input LOW Voltage (1)				0.8	V	Guaranteed Input LOW Voltage
V_{IK}	Input Clamp Diode Voltage				-1.5	V	V_{CC} = MIN, I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage		2.7			V	V_{CC} = MIN, I_{OH} = -0.8 mA
V_{OL}	Output LOW Voltage				0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
I_{OZH}	Output Off Current-HIGH	$DATA_{0-15}$			70	μA	V_{CC} = MAX, V_{OUT} = 2.4 V
		SC_{0-6}			50	μA	
I_{OZL}	Output Off Current-LOW	$DATA_{0-15}$			-410	μA	V_{CC} = MAX, V_{OUT} = 0.5 V
		SC_{0-6}			-50	μA	
I_{IH}	Input High Current	$DATA_{0-15}$			70	μA	V_{CC} = MAX, V_{IN} = 2.7 V
		OTHERS			50	μA	
		ALL			1.0	mA	V_{CC} = MAX, V_{IN} = 5.5 V
I_{IL}	Input Low Current	$DATA_{0-15}$			-410	μA	V_{CC} = MAX, V_{IN} = 0.5 V
		OTHERS			-360	μA	
I_{OS}	Short Circuit Current (2)		-25		-85	mA	V_{CC} = MAX, V_O = 0 V
I_{CC}	Power Supply Current				300	mA	V_{CC} = MAX

(1) These input levels provide zero noise immunity and should be tested only in a static, noise-free environment.
(2) Not more than one output should be shorted at a time

FIGURE 2 — AC TEST FIXTURE

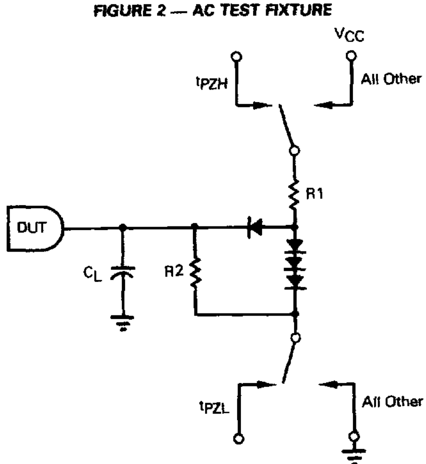


TABLE 4. TEST OUTPUT LOADS

Pin	Pin Label	R_1	R_2
-	D_0-D_{15}	430 Ω	1 kΩ
24-30	SC_0-SC_6	430 Ω	1 kΩ
32	$\overline{ERROR}$	470 Ω	3 kΩ
33	$\overline{MULT\ ERROR}$	470 Ω	3 kΩ

TABLE 5. AC CHARACTERISTICS (MAXIMUM LIMITS)

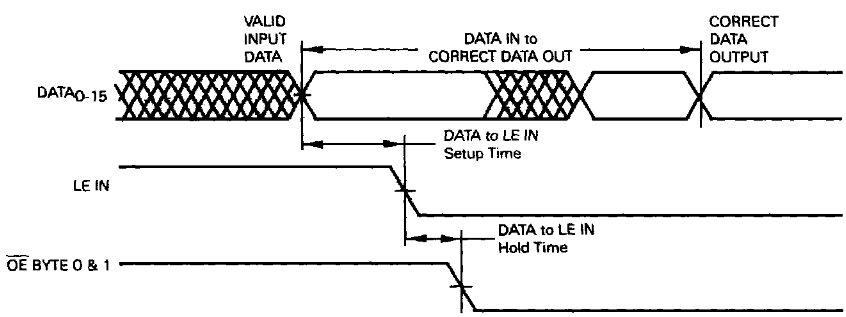
SYMBOL	PARAMETER		V_{CC} = 5.0 V ± 5%; T_A = 0 to +70°C; C_L = 50 pF; UNITS = ns***							
	From Input / To Output		SC_{0-6}		$DATA_{0-15}$		$\overline{ERROR}$		$\overline{MULT\ ERROR}$	
t_{PLH}, t_{PHL}	Propagation Delay		MC74F 2960	MC74F 2960A	MC74F 2960	MC74F 2960A	MC74F 2960	MC74F 2960A	MC74F 2960	MC74F 2960A
	$DATA_{0-15}$		32	20	65*	42*	32	19	50	26
	CB_{0-6} (CODE ID_{2-0} 000, 011)		28	18	56	34	29	16	47	24
	CB_{0-6} (CODE ID_{2-0} 010, 100, 101, 110, 111)		28	19	45	30	29	18	34	22
	$\overline{GENERATE}$		35	19	63	35	36	18	55	22
	CORRECT (Not Internal Control Mode)		—	—	45	32	—	—	—	—
	DIAG $MODE_{0-1}$ (Not Internal Control Mode)		50	35	78	55	59	42	75	53
	PASS THRU (Not Internal Control Mode)		36	18	44	30	29	18	46	22
	CODE ID_{0-2}		61	40	90	52	60	40	80	44
	LE IN (From latched to transparent)		39	24	72*	40*	39	22	59	26
	LE OUT (From latched to transparent)		—	—	31	22	—	—	—	—
	LE DIAG (From latched to transparent; Not Internal Control Mode)		45	32	78	55	45	32	65	46
	Internal Control Mode: LE DIAG (From latched to transparent)		67	47	96	67	66	46	86	60
	Internal Control Mode: $DATA_{0-15}$ (Via Diagnostic Latch)		67	47	96	67	66	46	86	60
t_{PZH}, t_{PZL}**	Output Enable Time	$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	—	—	30	30	—	—	—	—
		$\overline{OE}$ SC	30	30	—	—	—	—	—	—
t_{PHZ}, t_{PLZ}**	Output Disable Time	$\overline{OE}$ BYTE 0, $\overline{OE}$ BYTE 1	—	—	30	30	—	—	—	—
		$\overline{OE}$ SC	30	30	—	—	—	—	—	—

*Data In or LE In to Correct Data Out measurement requires timing as shown in Figure 3.
**C_L for t_{PZH}, t_{PZL}, t_{PHZ} and t_{PLZ} = 5.0 pF
***Inputs switching between 0V and 3V at 1V/ns, measurements made at 1.5V. All outputs have maximum DC load.

TABLE 6. AC OPERATING REQUIREMENTS (MINIMUM LIMITS)

SYMBOL	PARAMETER		T_A = 0 to +70°C V_{CC} = 5.0 V ±10% MC74F2960	MC74F2960A	UNITS
t_{su} t_h	Setup Time Hold Time	$DATA_{0-15}$ to LE IN	6 7	4 6	ns
t_{su} t_h	Setup Time Hold Time	CB_{0-6} to LE IN	5 6	3 5	ns
t_{su} t_h	Setup Time Hold Time	$DATA_{0-15}$ to LE OUT	44 5	18 3	ns
t_{su} t_h	Setup Time Hold Time	CB_{0-6} to LE OUT (Code ID 000, 011)	35 0	17 0	ns
t_{su} t_h	Setup Time Hold Time	CB_{0-6} to LE OUT (Code ID 010, 100, 101, 110, 111)	27 0	27 0	ns
t_{su} t_h	Setup Time Hold Time	$\overline{\text{GENERATE}}$ to LE OUT	42 0	27 0	ns
t_{su} t_h	Setup Time Hold Time	CORRECT to LE OUT	26 1	19 0	ns
t_{su} t_h	Setup Time Hold Time	DIAG $MODE_{0-1}$, to LE OUT	69 0	69 0	ns
t_{su} t_h	Setup Time Hold Time	PASS THRU to LE OUT	26 0	20 0	ns
t_{su} t_h	Setup Time Hold Time	CODE ID_{0-2}, to LE OUT	81 0	24 0	ns
t_{su} t_h	Setup Time Hold Time	LE IN to LE OUT	51 5	30 5	ns
t_{su} t_h	Setup Time Hold Time	$DATA_{0-15}$ to LE DIAG	6 8	6 8	ns
t_w	Minimum Pulse Width, High or Low	LE IN, LE OUT, or LE DIAG	15	15	ns

FIGURE 3 — TIMING REQUIRED for DATA IN (or LE IN) to CORRECTED DATA OUT



PIN DEFINITIONS

$DATA_{0-15}$

16 bidirectional data lines. They provide input to the Data Input Latch and Diagnostic Latch, and receive output from the Data Output Latch. $DATA_0$ is the least significant bit; $DATA_{15}$ the most significant.

CB_{0-6}

Seven Check Bit input lines. The check bit lines are used to input check bits for error detection. They are also used to input syndrome bits for error correction in 32 and 64-bit configurations.

LE IN

Latch Enable — Data Input Latch. Controls latching of the input data. When HIGH the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.

$\overline{\text{GENERATE}}$

Generate Check Bits input. When this input is LOW the EDAC is in the Check Bit Generate Mode. When HIGH the EDAC is in the Detect Mode or Correct Mode.

In the Generate Mode the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs.

In the Detect or Correct Modes the EDAC detects single and multiple errors, and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct Mode, single-bit errors are also automatically corrected — corrected data is placed at the inputs of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates in a coded form the number of errors and the bit-in-error.

SC_{0-6}

Syndrome/Check Bit outputs. These seven lines hold the check/partial-check bits when the EDAC is in Generate Mode, and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct Modes. These are 3-state outputs.

$\overline{\text{OE}}$ SC

Output Enable — Syndrome/Check Bits. When LOW, the 3-state output lines SC_{0-6} are enabled. When HIGH, the SC outputs are in the high impedance state.

$\overline{\text{ERROR}}$

Error Detected output. When the EDAC is in Detect or Correct Mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate Mode, $\overline{\text{ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{ERROR}}$ must be externally implemented.)

$\overline{\text{MULT ERROR}}$

Multiple Errors Detected output. When the EDAC is in Detect or Correct Mode, this output if LOW indicates that there are two or more bit errors that have been detected. If HIGH this indicates that either one or no errors have been detected. In Generate mode, $\overline{\text{MULT ERROR}}$ is forced HIGH. (In a 64-bit configuration, $\overline{\text{MULT ERROR}}$ must be externally implemented.)

CORRECT

Correct input. When HIGH this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it onto the Data Output Latch. When LOW the EDAC will drive data directly from the Data Input Latch to the Data Output Latch without correction.

LE OUT

Latch Enable — Data Output Latch. Controls the latching of the Data Output Latch. When LOW the Data Output Latch is latched to its previous state. When HIGH the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct Mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect Mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are unspecified if the EDAC is in Generate Mode.

$\overline{\text{OE}}$ BYTE 0, $\overline{\text{OE}}$ BYTE 1

Output Enable — Bytes 0 and 1, Data Output Latch. These lines control the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW these lines enable the Data Output Latch and when HIGH these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output Latch at a time.

PASS THRU

Pass Thru input. This line when HIGH forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC_{0-6}) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.

DIAG $MODE_{0-1}$

Diagnostic Mode Select. These two lines control the initialization and diagnostic operation of the EDAC.

CODE ID_{0-2}

Code Identification inputs. These three bits identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDAC is processing. The three allowable data word sizes are 16, 32 and 64-bits and their respective modified Hamming codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID_2, ID_1, ID_0) is also used to instruct the EDAC that the signals CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU are to be taken from the Diagnostic Latch, rather than from the input control lines.

LE DIAG

Latch Enable — Diagnostic Latch. When HIGH the Diagnostic Latch follows the 16-bit data on the input lines. When LOW the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits, and internal control signals for CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU.

FUNCTIONAL DESCRIPTION

The MC74F2960 and MC74F2960A contain the necessary logic to generate check bits on a 16-bit data field according to a modified Hamming code. This code allows the EDAC to 1) be cascaded, 2) detect all double bit errors, 3) detect RAM failure (all 1 or 0 data).

The EDAC may be configured to work on data words from 8- to 64-bits in length. When cascaded for word lengths in excess of 16 bits, each EDAC must know which bits it is processing. This is done with Code ID inputs as shown in Table 7. The Internal Control Mode is described later.

MODE SELECTION

The device control lines are $\overline{\text{GENERATE}}$, CORRECT, PASS THRU, DIAG $MODE_{0-1}$ and CODE ID_{0-2}. Table 8 lists the MC74F2960 and MC74F2960A modes of operation. The data flow for each of these modes is shown in Figures 3 through 6.

PASS THRU MODE

In this mode, the unmodified contents of the Data Input Latch are placed on the inputs of the Data Output Latch and the contents of the Check Bit Input Latch are placed on the SC outputs. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in this mode.

GENERATE MODE

In this mode check bits will be generated that correspond to the contents of the Data Input Latch. The check bits generated are placed on the SC outputs.

DETECT MODE

In this mode the device examines the contents of the Data Input Latch against the Check Bit Input Latch, and will detect all single-bit errors, all double-bit errors and some triple-bit errors. If one or more errors are detected, $\overline{\text{ERROR}}$ goes LOW. If two or more errors are detected, $\overline{\text{MULT ERROR}}$ goes LOW. Both error indicators are HIGH if there are no errors.

Also available on the SC outputs are the syndrome bits generated by the error detection step. The syndrome bits may be decoded to determine if a bit error was detected and, for single-bit errors, which of the data or check bits is in error.

In Detect Mode, the contents of the Data Input Latch are driven directly to the inputs of the Data Output Latch without correction.

CORRECT MODE

In this mode, the EDAC functions the same as in Detect Mode except that the correction network is allowed to correct (complement) any single-bit error of the Data Input Latch before putting it onto the inputs of the Data Output Latch. If multiple errors are detected, the output of the correction network is unspecified.

If the single-bit error is a check bit there is no automatic correction. If check bit correction is desired, this can be done by placing the device in GENERATE MODE to produce a correct check bit sequence for the data in the Data Input Latch.

DIAGNOSTIC GENERATE
DIAGNOSTIC DETECT
DIAGNOSTIC CORRECT

These are special diagnostic modes where check bits loaded into the Diagnostic Latch are substituted for either normal check bit inputs or outputs.

INITIALIZE

The inputs of the Data Output Latch are forced to zeroes. The check bit outputs (SC) are generated to correspond to the all-zero data. $\overline{\text{ERROR}}$ and $\overline{\text{MULT ERROR}}$ are forced HIGH in the initialize Mode.

Initialize Mode is useful after power up when RAM contents are random. The EDAC may be placed in initialize mode and its' outputs written into all memory locations by the processor.

INTERNAL CONTROL MODE

When in the internal control mode, the EDAC takes the CODE ID_{0-2}, DIAG $MODE_{0-1}$, CORRECT and PASS THRU control signals from the Internal Diagnostic Latch rather than from the external input lines or Memory Controller.

TABLE 7. HAMMING CODE AND SLICE IDENTIFICATION

CODE ID_2	CODE ID_1	CODE ID_0	Hamming Code and Slice Selected
0	0	0	Code 16/22
0	0	1	Internal Control Mode
0	1	0	Code 32/39, Bytes 0 and 1
0	1	1	Code 32/39, Bytes 2 and 3
1	0	0	Code 64/72, Bytes 0 and 1
1	0	1	Code 64/72, Bytes 2 and 3
1	1	0	Code 64/72, Bytes 4 and 5
1	1	1	Code 64/72, Bytes 6 and 7

TABLE 8. F2960/F2960A MODES OF OPERATION

	CONTROL INPUTS*				
OPERATING MODE*	DIAG MODE 1	DIAG MODE 0	PASS THRU	$\overline{\text{GENERATE}}$	CORRECT
PASS THRU	X	X	1	X	X
GENERATE	X	0	0	0	X
DETECT	0	X	0	1	0
CORRECT	0	X	0	1	1
DIAGNOSTIC GENERATE	0	1	0	0	X
DIAGNOSTIC DETECT	1	0	0	1	0
DIAGNOSTIC CORRECT	1	0	0	1	1
INITIALIZE	1	1	0	X	X

*The internal control mode overrides control inputs (See Text).

FIGURE 4 — CHECK BIT GENERATION

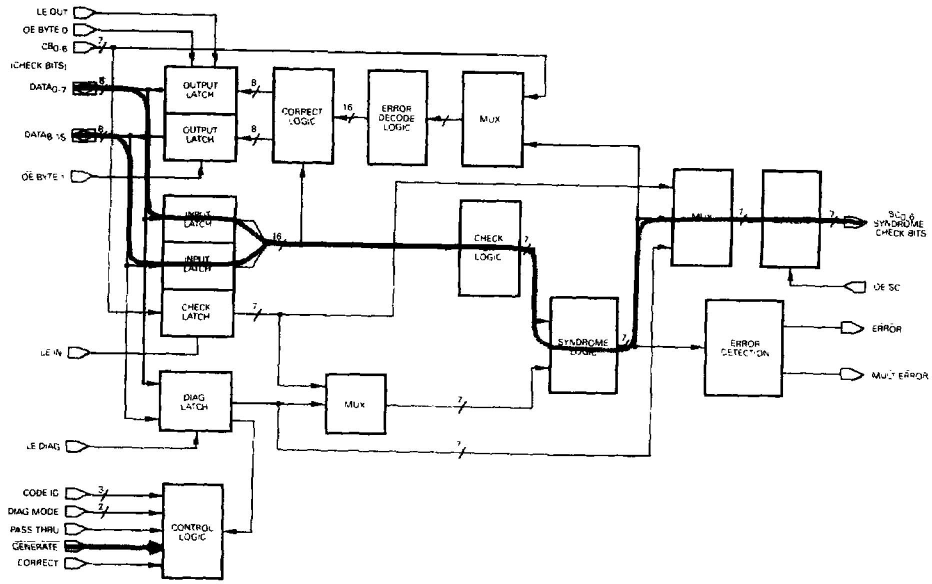


FIGURE 5 — ERROR DETECTION AND CORRECTION

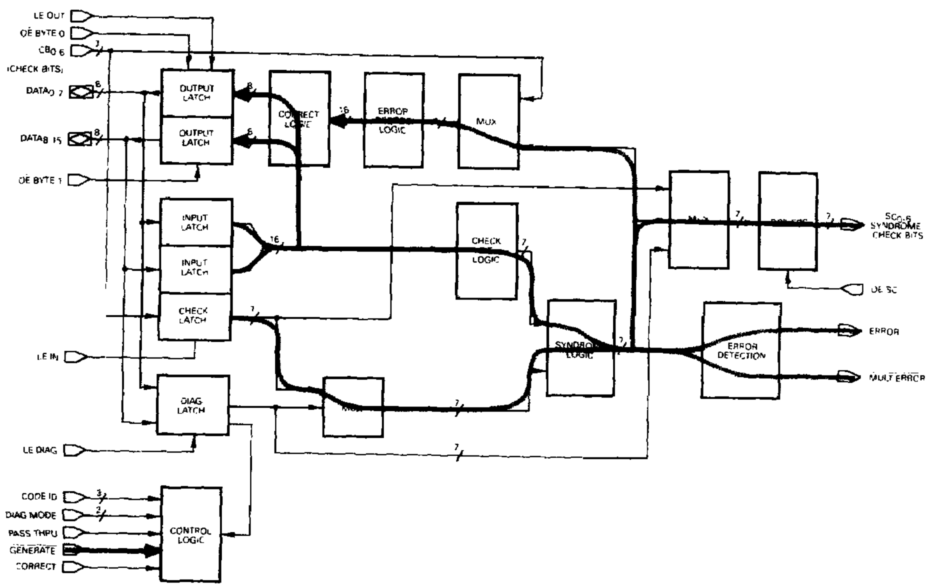


FIGURE 6 — DIAGNOSTIC CHECK BIT GENERATION

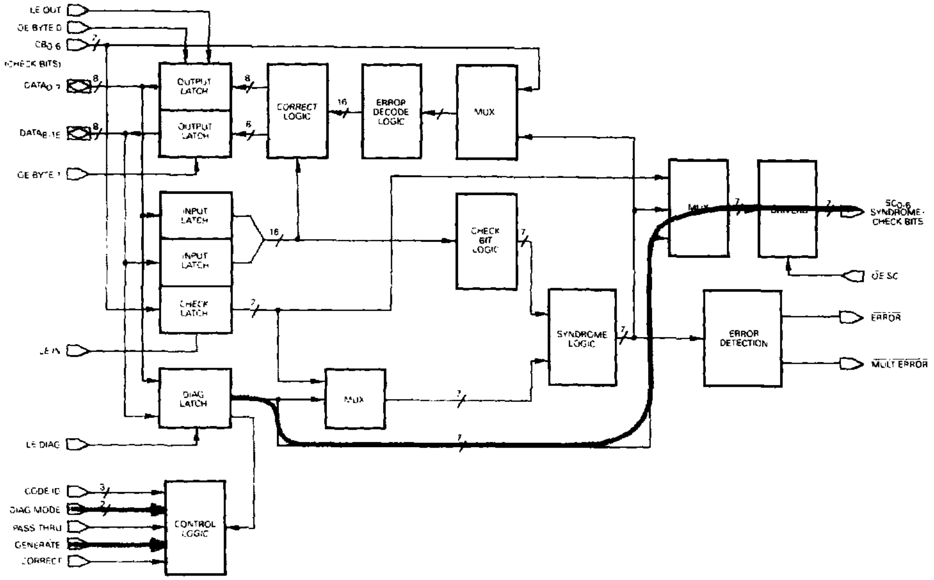
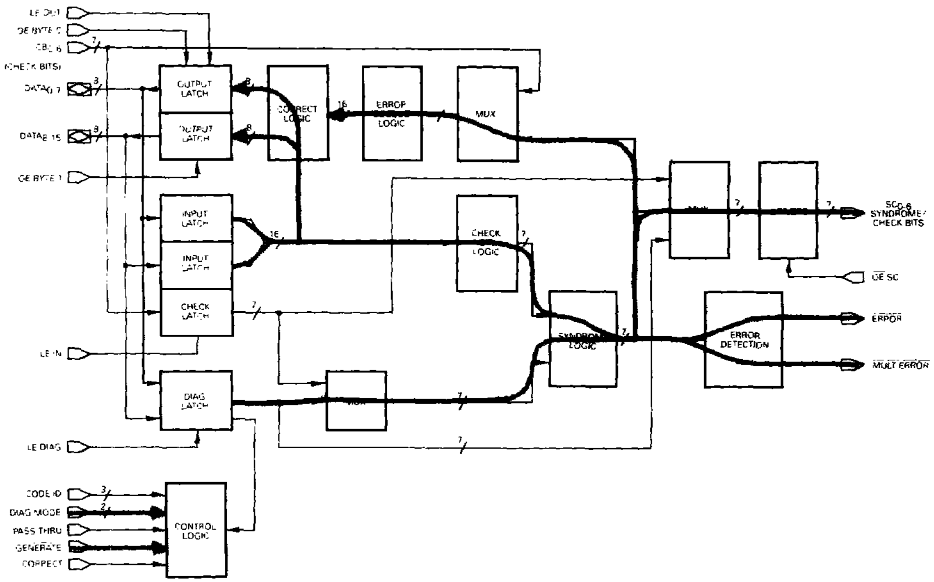


FIGURE 7 — DIAGNOSTIC DETECT AND CORRECT



CASCADING THE MC74F2960/MC74F2960A

The system configuration, as well as the specific function of various EDAC inputs and outputs, varies slightly depending upon the width of the data word.

The system configuration for 16-bit, 32-bit and 64-bit data words is shown in Figures 7, 8 and 9. In addition, accompanying figures and tables indicate the memory word format, diagnostic latch format, check bit encode, syndrome decode and ac calculations for each configuration.

When cascading to 32- or 64-bit configurations, syndrome bits must be fed back to the check bit inputs to correct an erroneous data word. Figure 9 and Table 18 illustrate the use of a 3-state buffer to control the multiplexing of check bits and syndrome bits into the EDAC(s).

Cascading to a 64-bit configuration requires additional MSI logic to generate a portion of the Syndrome and also the $\overline{\text{ERROR}}$ flag. The implementation shown in Figure 10 results in a different meaning for the $\overline{\text{MULT ERROR}}$ flag than in other configurations. $\overline{\text{MULT ERROR}}$ is HIGH if no errors or a 1-bit error is detected, but it is also HIGH for some 2-bit errors. In order to determine if an error is correctable, a DOUBLE ERROR output indicates that 2 errors have been detected when HIGH. Otherwise DOUBLE ERROR is Low.

16-BIT DATA WORD WIDTH

TABLE 9. 16-BIT DATA FORMAT

DATA		CHECK BITS					
BYTE 1	BYTE 0	CX	C0	C1	C2	C4	C8
15 8	7 0						

Uses Modified Hamming Code 16/22
- 16 data bits
- 6 check bits
- 22 bits in total

FIGURE 8 — 16-BIT CONFIGURATION

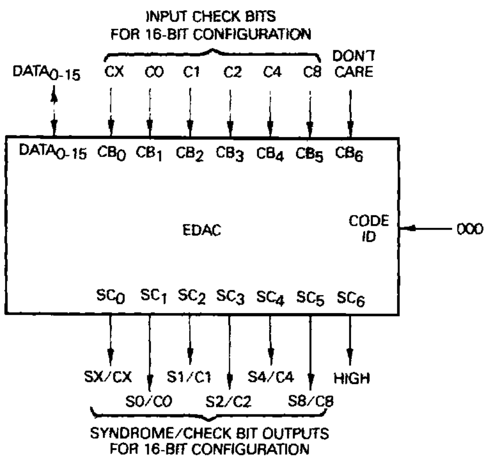


TABLE 10. 16-BIT MODIFIED HAMMING CODE — CHECK BIT ENCODE CHART

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X

The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

16-BIT DATA WORD WIDTH (continued)

TABLE 11. SYNDROME DECODE TO BIT-IN-ERROR

Syndrome Bits			S8	0	1	0	1	0	1	0	1
			S4	0	0	1	1	0	0	1	1
			S2	0	0	0	0	1	1	1	1
SX	S0	S1									
0	0	0		*	C8	C4	T	C2	T	T	M
0	0	1		C1	T	T	15	T	13	7	T
0	1	0		C0	T	T	M	T	12	6	T
0	1	1		T	10	4	T	0	T	T	M
1	0	0		CX	T	T	14	T	11	5	T
1	0	1		T	9	3	T	M	T	T	M
1	1	0		T	8	2	T	1	T	T	M
1	1	1		M	T	T	M	T	M	M	T

* — *no errors detected*
Number — *the location of the single bit-in-error*
T — two errors detected
M — three or more errors detected

TABLE 12. DIAGNOSTIC LATCH LOADING — 16-BIT FORMAT

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	CODE ID 0
9	CODE ID 1
10	CODE ID 2
11	DIAG MODE 0
12	DIAG MODE 1
13	CORRECT
14	PASS THRU
15	Don't Care

32-BIT DATA WORD WIDTH

TABLE 13. SYNDROME DECODE TO BIT-IN-ERROR

Syndrome Bits				S16	0	1	0	1	0	1	0	1
				S8	0	0	1	1	0	0	1	1
				S4	0	0	0	0	1	1	1	1
SX	S0	S1	S2									
0	0	0	0		*	C16	C8	T	C4	T	T	30
0	0	0	1		C2	T	T	27	T	5	M	T
0	0	1	0		C1	T	T	25	T	3	15	T
0	0	1	1		T	M	13	T	23	T	T	M
0	1	0	0		C0	T	T	24	T	2	M	T
0	1	0	1		T	1	12	T	22	T	T	M
0	1	1	0		T	M	10	T	20	T	T	M
0	1	1	1		16	T	T	M	T	M	M	T
1	0	0	0		CX	T	T	M	T	M	14	T
1	0	0	1		T	M	11	T	21	T	T	M
1	0	1	0		T	M	9	T	19	T	T	31
1	0	1	1		M	T	T	29	T	7	M	T
1	1	0	0		T	M	8	T	18	T	T	M
1	1	0	1		17	T	T	28	T	6	M	T
1	1	1	0		M	T	T	26	T	4	M	T
1	1	1	1		T	0	M	T	M	T	T	M

* — no errors detected
Number — the location of the single bit-in-error
T — two errors detected
M — three or more errors detected

TABLE 14. DIAGNOSTIC LATCH LOADING — 32-BIT FORMAT

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6	Diagnostic Check Bit 16
7	Don't Care
8	Slice 0/1 — CODE ID 0
9	Slice 0/1 — CODE ID 1
10	Slice 0/1 — CODE ID 2
11	Slice 0/1 — DIAG MODE 0
12	Slice 0/1 — DIAG MODE 1
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 — CODE ID 0
25	Slice 2/3 — CODE ID 1
26	Slice 2/3 — CODE ID 2
27	Slice 2/3 — DIAG MODE 0
28	Slice 2/3 — DIAG MODE 1
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASS THRU
31	Don't Care

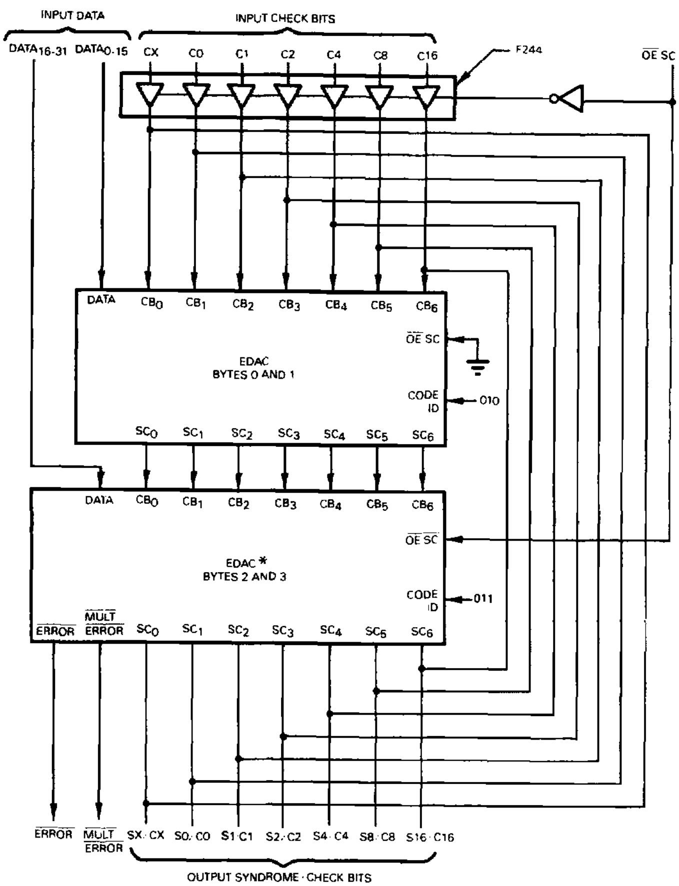
32-BIT DATA WORD WIDTH (continued)

TABLE 15. 32-BIT DATA FORMAT

DATA				CHECK BITS						
BYTE 3	BYTE 2	BYTE 1	BYTE 0	CX	C0	C1	C2	C4	C8	C16
31 24	23 16	15 8	7 0							

Uses Modified Hamming Code 32/39
- 32 data bits
- 7 check bits
- 39 bits in total

FIGURE 9 — 32-BIT CONFIGURATION



*Check Bit Latch is Forced Transparent in this Code ID Combination for this Slice

32-BIT DATA WORD WIDTH (continued)

TABLE 16. 32-BIT MODIFIED HAMMING CODE — CHECK BIT ENCODE CHART

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)	X				X		X	X	X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X					X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X

TABLE 17. KEY AC CALCULATIONS FOR THE 32-BIT CONFIGURATION

32-Bit Propagation Delay		Delay Calculation
From	To	
DATA	Check Bits Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA IN	Corrected DATA OUT	(DATA to SC) + (CB to SC, CODE ID 011) + (CB to DATA, CODE ID 010)
DATA	Syndromes Out	(DATA to SC) + (CB to SC, CODE ID 011)
DATA	$\overline{\text{ERROR}}$ for 32 Bits	(DATA to SC) + (CB to $\overline{\text{ERROR}}$, CODE ID 011)
DATA	$\overline{\text{MULT ERROR}}$ for for 32 Bits	(DATA to SC) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 011)

64-BIT DATA WORD WIDTH

TABLE 18. 64-BIT DATA FORMAT

DATA								CHECK BITS							
BYTE 7	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0	CX	C0	C1	C2	C4	C8	C16	C32
63 — 48	47 —	— 32	31 —	— 16	15 —		— 0								

Uses Modified Hamming Code 64/72
- 64 data bits
- 8 check bits
- 72 bits in total

64-BIT DATA WORD WIDTH (continued)

TABLE 19. 64-BIT MODIFIED HAMMING CODE — CHECK BIT ENCODE CHART

Generated Check Bits	Parity	Participating Data Bits															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)	X	X	X	X	X	X	X	X								

Generated Check Bits	Parity	Participating Data Bits															
		16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
CX	Even (XOR)		X	X	X		X			X	X		X			X	
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)									X	X	X	X	X	X	X	X

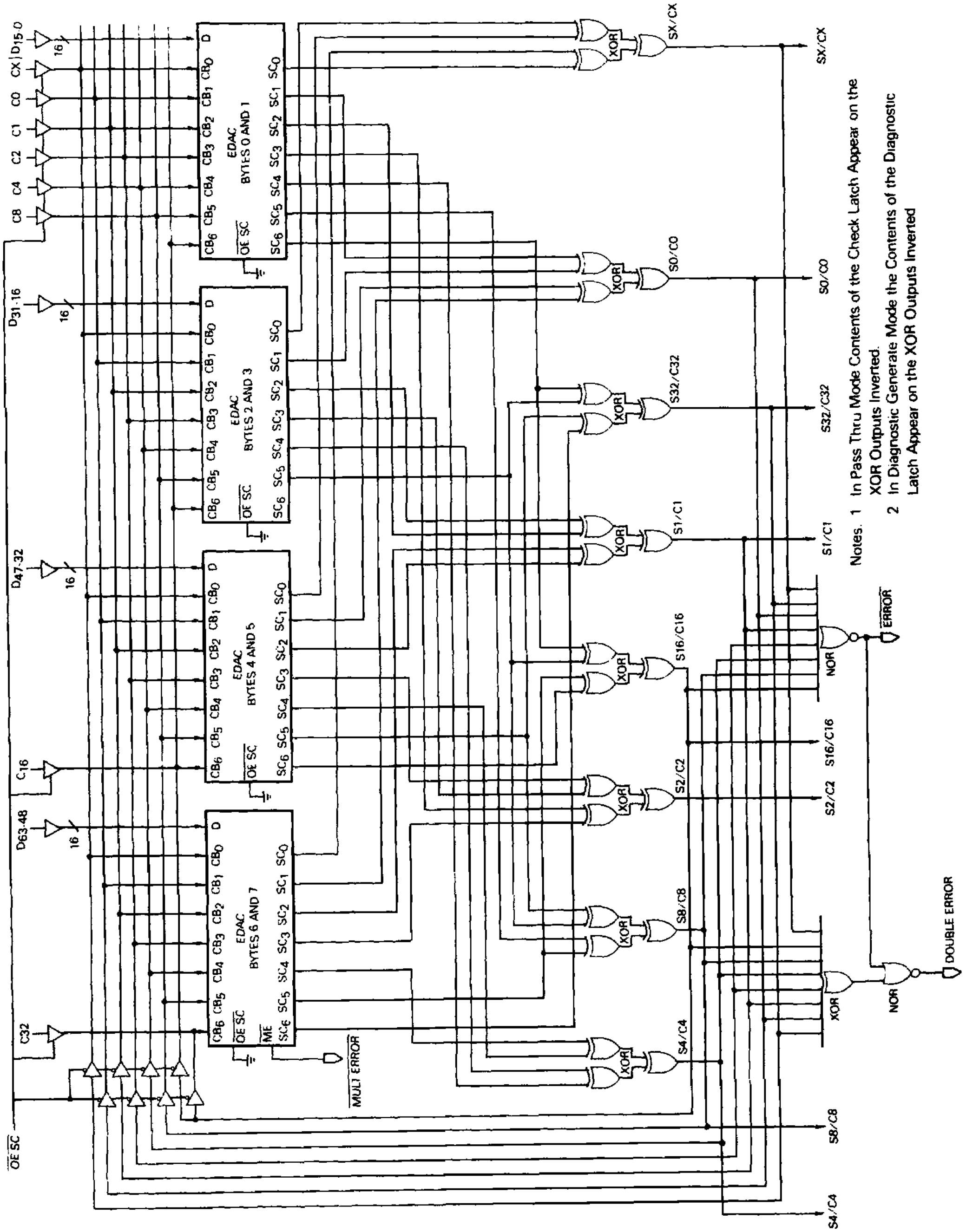
Generated Check Bits	Parity	Participating Data Bits															
		32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)	X	X	X	X	X	X	X	X								
C32	Even (XOR)									X	X	X	X	X	X	X	X

Generated Check Bits	Parity	Participating Data Bits															
		48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CX	Even (XOR)	X				X		X	X			X		X	X		X
C0	Even (XOR)	X	X	X		X		X		X		X		X			
C1	Odd (XNOR)	X			X	X			X		X	X			X		X
C2	Odd (XNOR)	X	X				X	X	X				X	X	X		
C4	Even (XOR)			X	X	X	X	X	X							X	X
C8	Even (XOR)									X	X	X	X	X	X	X	X
C16	Even (XOR)									X	X	X	X	X	X	X	X
C32	Even (XOR)	X	X	X	X	X	X	X	X								

The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

64-BIT DATA WORD WIDTH (continued)

FIGURE 10 — 64-BIT DATA CONFIGURATION



Notes. 1 In Pass Thru Mode Contents of the Check Latch Appear on the XOR Outputs Inverted.
2 In Diagnostic Generate Mode the Contents of the Diagnostic Latch Appear on the XOR Outputs Inverted

64-BIT DATA WORD WIDTH (continued)

TABLE 20. SYNDROME DECODE TO BIT-IN-ERROR

Syndrome Bits																			
				S32	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
				S16	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
				S8	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
				S4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
SX	S0	S1	S2																	
0	0	0	0		*	C32	C16	T	C8	T	T	M	C4	T	T	M	T	46	62	T
0	0	0	1		C2	T	T	M	T	43	59	T	T	53	37	T	M	T	T	M
0	0	1	0		C1	T	T	M	T	41	57	T	T	51	35	T	15	T	T	31
0	0	1	1		T	M	M	T	13	T	T	29	23	T	T	7	T	M	M	T
0	1	0	0		C0	T	T	M	T	40	56	T	T	50	34	T	M	T	T	M
0	1	0	1		T	49	33	T	12	T	T	28	22	T	T	6	T	M	M	T
0	1	1	0		T	M	M	T	10	T	T	26	20	T	T	4	T	M	M	T
0	1	1	1		16	T	T	0	T	M	M	T	T	M	M	T	M	T	T	M
1	0	0	0		CX	T	T	M	T	M	M	T	T	M	M	T	14	T	T	30
1	0	0	1		T	M	M	T	11	T	T	27	21	T	T	5	T	M	M	T
1	0	1	0		T	M	M	T	9	T	T	25	19	T	T	3	T	47	63	T
1	0	1	1		M	T	T	M	T	45	61	T	T	55	39	T	M	T	T	M
1	1	0	0		T	M	M	T	8	T	T	24	18	T	T	2	T	M	M	T
1	1	0	1		17	T	T	1	T	44	60	T	T	54	38	T	M	T	T	M
1	1	1	0		M	T	T	M	T	42	58	T	T	52	36	T	M	T	T	M
1	1	1	1		T	48	32	T	M	T	T	M	M	T	T	M	T	M	M	T

* — no errors detected
Number — the location of the single bit-in-error
T — two errors detected
M — three or more errors detected

TABLE 21. DIAGNOSTIC LATCH LOADING — 64-BIT FORMAT

Data Bit	Internal Function
0	Diagnostic Check Bit X
1	Diagnostic Check Bit 0
2	Diagnostic Check Bit 1
3	Diagnostic Check Bit 2
4	Diagnostic Check Bit 4
5	Diagnostic Check Bit 8
6, 7	Don't Care
8	Slice 0/1 — CODE ID 0
9	Slice 0/1 — CODE ID 1
10	Slice 0/1 — CODE ID 2
11	Slice 0/1 — DIAG MODE 0
12	Slice 0/1 — DIAG MODE 1
13	Slice 0/1 — CORRECT
14	Slice 0/1 — PASS THRU
15	Don't Care
16-23	Don't Care
24	Slice 2/3 — CODE ID 0
25	Slice 2/3 — CODE ID 1
26	Slice 2/3 — CODE ID 2
27	Slice 2/3 — DIAG MODE 0
28	Slice 2/3 — DIAG MODE 1
29	Slice 2/3 — CORRECT
30	Slice 2/3 — PASS THRU

Data Bit	Internal Function
31	Don't Care
32-37	Don't Care
38	Diagnostic Check Bit 16
39	Don't Care
40	Slice 4/5 — CODE ID 0
41	Slice 4/5 — CODE ID 1
42	Slice 4/5 — CODE ID 2
43	Slice 4/5 — DIAG MODE 0
44	Slice 4/5 — DIAG MODE 1
45	Slice 4/5 — CORRECT
46	Slice 4/5 — PASS THRU
47	Don't Care
48-54	Don't Care
55	Diagnostic Check Bit 32
56	Slice 6/7 — CODE ID 0
57	Slice 6/7 — CODE ID 1
58	Slice 6/7 — CODE ID 2
59	Slice 6/7 — DIAG MODE 0
60	Slice 6/7 — DIAG MODE 1
61	Slice 6/7 — CORRECT
62	Slice 6/7 — PASS THRU
63	Don't Care

64-BIT DATA WORD WIDTH (continued)

TABLE 22. KEY AC CALCULATIONS FOR THE 64-BIT CONFIGURATION

64-Bit Propagation Delay		Delay Calculation
From	To	
DATA	Check Bits Out	(DATA to SC) + (XOR Delay)
DATA IN	Corrected DATA OUT	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)
DATA	Syndromes	(DATA to SC) + (XOR Delay)
DATA	$\overline{\text{ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (NOR Delay)
DATA	$\overline{\text{MULT ERROR}}$ for 64 Bits	(DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to $\overline{\text{MULT ERROR}}$, CODE ID 1xx)
DATA	DOUBLE ERROR for 64 Bits	(DATA to SC) + (XOR Delay) + (XOR/NOR Delay)

FIGURE 11 — HIGH PERFORMANCE COMPUTER MEMORY