

# F386-Series Specifications (MIL-PRF-38534)



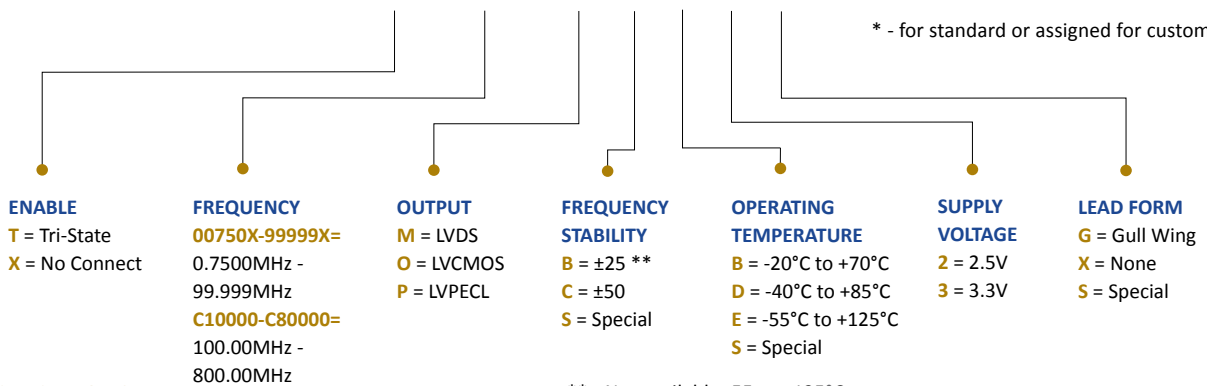
## Flat Pack



PDI Model F386 series is a high reliability product designed, processed and tested in our Middleton facility and certified to MIL-PRF-38534H. This “flat pack” product with hybrid assembly design and construction provides for superior long term reliability. Standard and custom frequencies are available and make this product ideal for Aerospace, Military, Avionic, Medical, and any other application requiring MIL-PRF-38534 certified content.

ex) **F386-T-25000X-M-C-D-3-X-X\***

\* - for standard or assigned for customization.



## CMOS SPECIFICATIONS

\*\* - Not available -55 to +125°C

Parameter	Supply Voltage*1 (±10%)		Units	
	3.3	2.5		
Frequency Range*1	0.750000 to 200.0000		MHz	
Frequency Stability*1	All Causes (Maximum)*2		ppm	
Temperature Range*1	Operating		°C	
	Storage		°C	
Supply Current (Maximum)	0.030000 to 23.999999 MHz	15	mA	
	24.000000 to 49.999999 MHz	20		
	50.000000 to 69.999999 MHz	30		
	70.000000 to 200.000000 MHz	45		
Output Load	Per Option			
Duty Cycle (at 50% Vcc)	15pF/10 TTL gates			
Rise/Fall Times (Maximum)	40 to 60% (45 to 55% option)			
	Rise Time (10% to 90% Vcc)	8	7	ns
Start up Time (Maximum)	Fall Time (90% to 10% Vcc)		8	7
Output Voltage Levels	10		ms	
	High (Minimum)	90		% Vcc
Low (Maximum)	10			
Pin 1 (Tri-State) (Option)	High (See below) or Open	Enable		
	Low (See below)*3	Disable		
	High Value (Minimum)	80	80	% Vcc
	Low Value (Maximum)*3	20	20	% Vcc
	Disable Current (Maximum)*3	10	10	uA
	Enable Delay Time (Maximum)	10		ms
Disable Delay Time (Maximum)	150		ns	

\*1 - Not all Frequency/Temperature/Voltage combinations are available.

\*2 - Inclusive of Tolerance @25°C, Operating Temperature, Supply Voltage, Load, Aging, Shock and Vibration.

\*3 - Internal crystal oscillation halted.

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## LVDS SPECIFICATIONS

Parameter		Supply Voltage* <sup>1</sup> (±5%)		Units
		3.3	2.5	V
Frequency Range* <sup>1</sup>		24.000000 to 800.000000		MHz
Frequency Stability* <sup>1</sup>	All Causes (Maximum)* <sup>2</sup>	Per Option		ppm
Temperature Range* <sup>1</sup>	Operating	Per Option		°C
	Storage	-55 to +125		°C
Supply Current (Maximum)		80		mA
Output		LVDS		
Load (Typical)	Between Output and Comp Output	100		Ω
Duty Cycle (Maximum)	@ 50% Vcc	45/55		%
Rise/Fall Times (Maximum)	Rise Time (20% to 80% Vcc)	0.4		nS
	Fall Time (80% to 20% Vcc)	0.4		
Start up Time (Maximum)		10.0		mS
Output Voltage Levels	High Voh (RL = 100Ω)	1.43 Typical , 1.60 Maximum		V
	Low Vol (RL = 100Ω)	0.90 Minimum , 1.10 Typical		
Differential Voltage		250 Min , 350 Typ , 450 Max		mV
Pin 1 (Tri-State) (Option)	High (See below) or Open	Enable		
	Low (See below)* <sup>3</sup>	Disable		
	High Value (Minimum)	70		% Vcc
	Low Value (Maximum)* <sup>3</sup>	30		% Vcc
	Disable Current (Typical)* <sup>3</sup>	10		uA
	Enable Delay Time (Maximum)	2.0		mS
	Disable Delay Time (Maximum)	0.2		uS
Integrated Phase Jitter (RMS)	12KHz to 20MHz	0.3 Typical , 1.0 Maximum		pS
Phase Noise (Typical)	@ 10KHz Offset	-138		dBc/Hz
	@ 100KHz Offset	-144		

## LVPECL SPECIFICATIONS

Parameter		Supply Voltage* <sup>1</sup> (±5%)		Units
		3.3	2.5	V
Frequency Range* <sup>1</sup>		24.000000 to 800.000000		MHz
Frequency Stability* <sup>1</sup>	All Causes (Maximum)* <sup>2</sup>	Per Option		ppm
Temperature Range* <sup>1</sup>	Operating	Per Option		°C
	Storage	-55 to +125		°C
Supply Current (Maximum)		100		mA
Output		LVPECL		
Load (Typical)	Into Vcc-2V	50		Ω
Duty Cycle (Maximum)	@ 50% Vcc	45/55		%
Rise/Fall Times (Maximum)	Rise Time (20% to 80% Vcc)	0.5		nS
	Fall Time (80% to 20% Vcc)	0.5		
Start up Time (Maximum)		10.0		mS
Output Voltage Levels	High Voh (50Ω to Vcc-2V)	Vcc-1.025 Min, Vcc-0.95 Typ, Vcc-0.88 Max		V
	Low Vol (50Ω to Vcc-2V)	Vcc-1.810 Min, Vcc-1.70 Typ, Vcc-1.62 Max		
Differential Voltage		595 Min , 750 Typ , 930 Max		mV
Pin 1 (Tri-State) (Option)	High (See below) or Open	Enable		
	Low (See below)* <sup>3</sup>	Disable		
	High Value (Minimum)	70		% Vcc
	Low Value (Maximum)* <sup>3</sup>	30		% Vcc
	Disable Current (Typical)* <sup>3</sup>	10		uA
	Enable Delay Time (Maximum)	2.0		mS
	Disable Delay Time (Maximum)	0.2		uS
Integrated Phase Jitter (RMS)	12KHz to 20MHz	0.2 Typical , 1.0 Maximum		pS
Phase Noise (Typical)	@ 10KHz Offset	-138		dBc/Hz
	@ 100KHz Offset	-144		

## MIL-PRF-38534H , Class H Device Screening

Test or Inspection	MIL-STD-883		Requirement	Reference Paragraph
	Method	Condition		
Preseal Burn-In	1030		Optional	C.5.3
Non-Destructive Bond Pull	2023		Optional	C.5.4
Internal Visual	2017		100%	C.5.5
Temperature Cycling	1010	C , 10 Cycles	100%	C.5.6
Mechanical Shock or Constant Acceleration	2002 or 2001	B , (Y1 direction only) 3,000 G's (Y1 direction only)	100%	C.5.6
PIND	2020		Optional	C.5.7
Pre-Burn-In Electrical Test	IAW applicable device specification		Optional	C.5.8
Burn-In	1015		100%	C.5.9
Final Electrical Test	IAW applicable device specification		100%	C.5.10
Seal (Fine and Gross)	1014		100%	C.5.11
Radiographic	2012		Optional	C.5.12
External Visual Screen	2009		100%	C.5.13

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## PACKAGE DIMENSIONS

Tolerance:  $\pm 0.008$  [.20mm] (Unless otherwise specified)

PIN	CONNECTION
1	Tri-State or No Connect
2-7	DNC
8	Ground/Case
9	Output
10	Comp. Out or No Connect
11-15	No Connect
16	Supply Voltage

