



Integrated Device Technology, Inc.

# FAST CMOS PARITY BUS TRANSCEIVER

**IDT54/74FCT833A**  
**IDT54/74FCT833B**

## FEATURES:

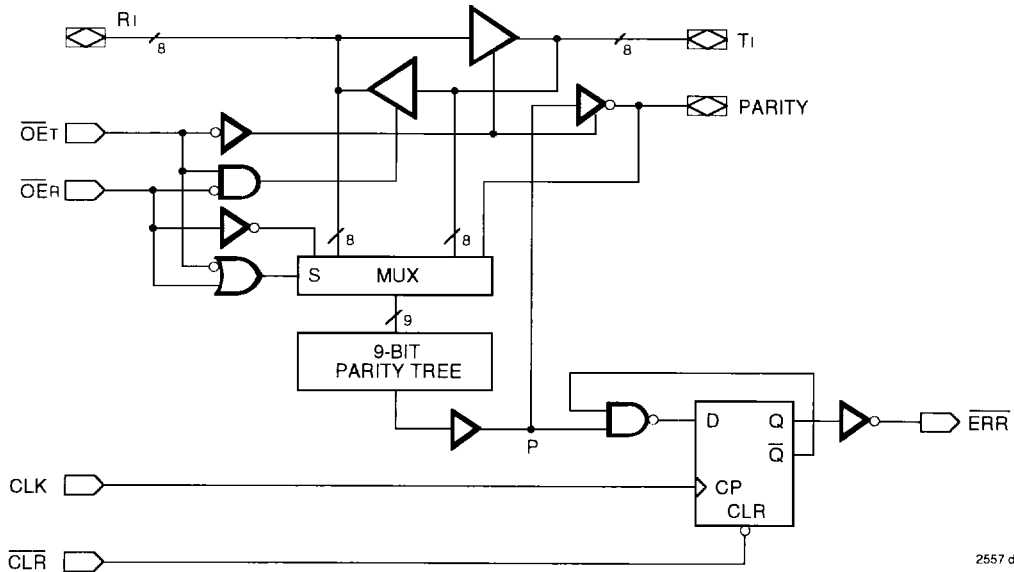
- Equivalent to AMD's Am29833 bipolar parity bus transceiver in pinout/function, speed and output drive over full temperature and voltage supply extremes
- High-speed bidirectional bus transceiver for processor-organized devices
- IDT54/74FCT833A equivalent to Am29833A speed and output drive
- **IDT54/74FCT833B 30% faster than Am29833A**
- Buffered direction and three-state controls
- Error flag with open-drain output
- $I_{OL} = 48\text{mA}$  (commercial) and  $32\text{mA}$  (military)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than AMD's bipolar Am29800 series ( $5\mu\text{A}$  max.)
- Available in plastic DIP, Cerdip, LCC and SOIC
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT54/74FCT833s are high-performance bus transceivers designed for two-way communications. They each contain an 8-bit data path from the R (port) to the T (port), an 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. The error flag can be clocked and stored in a register and read at the ERR output. The clear (CLR) input is used to clear the error flag register.

The output enables  $\overline{OE}_T$  and  $\overline{OE}_R$  are used to force the port outputs to the high-impedance state so that the device can drive bus lines directly. In addition,  $\overline{OE}_R$  and  $\overline{OE}_T$  can be used to force a parity error by enabling both lines simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability. The devices are specified at 48mA and 32mA output sink current over the commercial and military temperature ranges, respectively.

## FUNCTIONAL BLOCK DIAGRAM



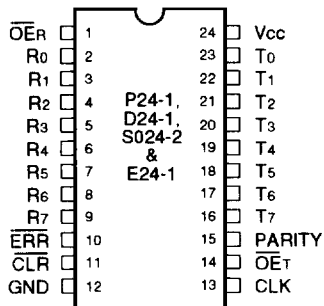
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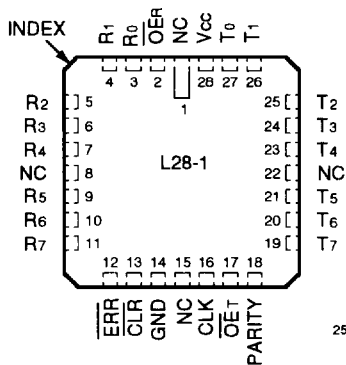
**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

**MAY 1992**

**PIN CONFIGURATIONS**



DIP/SOIC/CERPACK  
TOP VIEW



LCC  
TOP VIEW

2557 drw 02

**PIN DESCRIPTION**

Pin Name	I/O	Description
OER	I	RECEIVE enable input.
Ri	I/O	8-bit RECEIVE data input/output.
ERR	O	Output from fault registers. Register detection of odd parity fault on rising clock edge (CLK). A registered ERR output remains LOW until cleared. Open drain output, requires pull up resistor.
CLR	I	Clears the fault register output.
Ti	I/O	8-bit TRANSMIT data input/output.
PARITY	I/O	1-bit PARITY output.
OET	I	TRANSMIT enable input.
CLK	I	External clock pulse input for fault register flag.

2557 tbl 01

**ERROR FLAG OUTPUT FUNCTION TABLE<sup>(1,2)</sup>**

Inputs		Internal To Device	Output Pre-State	Output	Function
CLR	CLK	Point "P"	ERR <sub>n-1</sub>	ERR	
H	↑	H	H	H	Sample (1's Capture)
H	↑	—	L	L	
H	↑	L	—	L	
L	—	—	—	H	Clear

2557 tbl 02

**NOTES:**

- OET is HIGH and OER is LOW.
- H = HIGH  
L = LOW  
↑ = LOW-to-HIGH transition of clock  
— = Don't Care or Irrelevant

FUNCTION TABLE<sup>(2)</sup>

Inputs						Outputs				Function
OE <sub>T</sub>	OE <sub>R</sub>	CLR	CLK	Ri (Σ or H's)	Ti Incl Parity (Σ of H's)	Ri	Ti	Parity	ERR <sup>(1)</sup>	
L	H	H	↑	H (Odd)	NA	NA	H	L	H	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	H	↑	H (Even)	NA	NA	H	H	L	
L	H	H	↑	L (Odd)	NA	NA	L	L	H	
L	H	H	↑	L (Even)	NA	NA	L	H	L	
H	L	H	↑	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	↑	NA	H (Even)	H	NA	NA	L	
H	L	H	↑	NA	L (Odd)	L	NA	NA	H	
H	L	H	↑	NA	L (Even)	L	NA	NA	L	
—	—	L	—	—	—	NA	NA	NA	H	Clear the state of error flag register.
H	H	H	H or L	—	—	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	—	—	—	Z	Z	Z	H	
H	H	H	↑	H or L (Odd)	—	Z	Z	Z	H	
H	H	H	↑	H or L (Even)	—	Z	Z	Z	L	
L	L	H	↑	H (Odd)	NA	NA	H	H	L	Forced-error checking.
L	L	H	↑	H (Even)	NA	NA	H	L	H	
L	L	H	↑	L (Odd)	NA	NA	L	H	L	
L	L	H	↑	L (Even)	NA	NA	L	L	H	

NOTES:

1. Output state assumes HIGH output pre-state.

2. H = HIGH

L = LOW

↑ = LOW-to-HIGH transition of clock

\*No change to stored Error State

Z = High Impedance

NA = Not Applicable

— = Don't Care or Irrelevant

Odd = Odd number of logic one's

Even = Even number of logic one's

l = 0, 1, 2, 3, 4, 5, 6, 7

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**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Rating	Commercial	Military	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V <sub>TERM</sub> <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub>	-0.5 to V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	0 to +70	-55 to +125	°C
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	0.5	0.5	W
I <sub>OUT</sub>	DC Output Current	120	120	mA

NOTES: 2557 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V<sub>CC</sub> by +0.5V unless otherwise noted.
- Inputs and V<sub>CC</sub> terminals.
- Outputs and I/O terminals.

**CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)**

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	10	pF
C <sub>I/O</sub>	I/O Capacitance	V <sub>OUT</sub> = 0V	8	12	pF

NOTE: 2557 tbl 05

- This parameter is guaranteed by characterization but not tested.

**DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE**

Following Conditions Apply Unless Otherwise Specified: V<sub>LC</sub> = 0.2V; V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

Commercial: T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5.0V ± 5%; Military: T<sub>A</sub> = -55°C to +125°C, V<sub>CC</sub> = 5.0V ± 10%

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit		
V <sub>IH</sub>	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V		
V <sub>IL</sub>	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V		
I <sub>IH</sub>	Input HIGH Current (Except I/O Pins)	V <sub>CC</sub> = Max. V <sub>I</sub> = V <sub>CC</sub> V <sub>I</sub> = 2.7V V <sub>I</sub> = 0.5V	—	—	5	μA		
I <sub>IL</sub>	Input LOW Current (Except I/O Pins)		—	—	-5 <sup>(4)</sup>			
			—	—	-5			
I <sub>IH</sub>	Input HIGH Current (I/O Pins Only)	V <sub>CC</sub> = Max. V <sub>I</sub> = V <sub>CC</sub> V <sub>I</sub> = 2.7V V <sub>I</sub> = 0.5V V <sub>I</sub> = GND	—	—	15	μA		
I <sub>IL</sub>	Input LOW Current (I/O Pins Only)		—	—	15 <sup>(4)</sup>			
			—	—	-15 <sup>(4)</sup>			
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>N</sub> = -18mA	—	-0.7	-1.2	V		
I <sub>OS</sub>	Short Circuit Current	V <sub>CC</sub> = Max. <sup>(3)</sup> , V <sub>O</sub> = GND	-60	-120	—	mA		
V <sub>OH</sub>	Output HIGH Voltage (Except ERR)	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OH</sub> = -32μA	V <sub>HC</sub>	V <sub>CC</sub>	—	V		
		V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -300μA	V <sub>HC</sub>	V <sub>CC</sub>		—	
			I <sub>OH</sub> = -15mA MIL.	2.4	4.3		—	
			I <sub>OH</sub> = -24mA COM'L.	2.4	4.3	—		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 3V, V <sub>IN</sub> = V <sub>LC</sub> or V <sub>HC</sub> , I <sub>OL</sub> = 300μA	—	GND	V <sub>LC</sub>	V		
		V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	Except ERR	I <sub>OL</sub> = 300μA	—		GND	V <sub>LC</sub> <sup>(4)</sup>
				I <sub>OL</sub> = 32 mA MIL.	—		0.3	0.5
				I <sub>OL</sub> = 48mA COM'L.	—		0.3	0.5
			ERR	I <sub>OL</sub> = 48mA	—	0.3	0.5	

NOTES: 2557 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- This parameter is guaranteed but not tested.

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**POWER SUPPLY CHARACTERISTICS**  $V_{LC} = 0.2V$ ;  $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit	
I <sub>CC</sub>	Quiescent Power Supply Current	$V_{CC} = \text{Max.}; V_{IN} \geq V_{HC}, V_{IN} \leq V_{LC}$	—	0.2	1.5	mA	
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$	—	0.5	2.0	mA	
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>(4)</sup> Outputs Open	$V_{CC} = \text{Max.}$ $V_{IN} \leq V_{LC}$ $\overline{OET} = \overline{OER} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$	0.15	0.25	mA/ MHz	
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OET} = \text{GND}$ $\overline{OER} = V_{CC}$ $f_i = 2.5\text{MHz}$ One Bit Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.4	3.4	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.9	5.4	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OET} = \text{GND}$ $f_i = 2.5\text{MHz}$ $\overline{OER} = V_{CC}$ Eight Bits Toggling	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8 <sup>(5)</sup>	
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6.2	16.8 <sup>(5)</sup>	

**NOTES:**

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- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ , +25°C ambient.
- Per TTL driven input ( $V_{IN} = 3.4V$ ); all other inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$   
 $I_C = I_{CC} + \Delta I_{CC} \text{ DHNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 $I_{CC} = \text{Quiescent Current}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$   
 $\text{DH} = \text{Duty Cycle for TTL Inputs High}$   
 $\text{NT} = \text{Number of TTL Inputs at DH}$   
 $I_{CCD} = \text{Dynamic Current Caused by an Output Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$   
 $f_i = \text{Input Frequency}$   
 $N_i = \text{Number of Inputs at } f_i$   
 All currents are in milliamps and all frequencies are in megahertz.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE**

Symbol	Parameter	Conditions <sup>(1)</sup>	IDT54/74FCT833A				IDT54/74FCT833B				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
tPLH	Propagation Delay	CL = 50pF	—	10.0	—	14.0	—	7.0	—	10.0	ns
tPHL	RI to TI, TI to RI	CL = 300pF <sup>(3)</sup>	—	17.5	—	21.5	—	14.5	—	17.5	
tPLH	Propagation Delay	CL = 50pF	—	15.0	—	20.0	—	10.5	—	14.0	ns
tPHL	RI to PARITY	CL = 300pF <sup>(3)</sup>	—	22.5	—	27.5	—	18.0	—	21.5	
tPZH	Output Enable Time	CL = 50pF	—	12.0	—	16.0	—	8.5	—	11.0	ns
tPZL	OE <sub>R</sub> , OE <sub>T</sub> to RI, TI	CL = 300pF <sup>(3)</sup>	—	19.5	—	23.5	—	16.0	—	18.5	
tPHZ	Output Disable Time	CL = 5pF <sup>(3)</sup>	—	10.7	—	14.7	—	7.2	—	9.8	ns
tPLZ	OE <sub>R</sub> , OE <sub>T</sub> to RI, TI	CL = 50pF	—	12.0	—	16.0	—	8.5	—	11.0	
tSU	TI, PARITY to CLK Set-up Time	CL = 50pF	12.0	—	16.0	—	8.5	—	11.0	—	ns
tH	TI, PARITY to CLK Hold Time		0	—	0	—	0	—	0	—	ns
tREM	Clear Recovery Time CLR to CLK		15.0	—	20.0	—	10.5	—	14.0	—	ns
tw	Clock Pulse Width HIGH or LOW		7.0	—	9.5	—	5.5	—	7.0	—	ns
tw	Clear Pulse Width LOW		7.0	—	9.5	—	5.5	—	7.0	—	ns
tPHL	Propagation Delay CLK to ERR		—	12.0	—	16.0	—	8.5	—	11.0	ns
tPLH	Propagation Delay CLR to ERR		—	16.0	—	20.0	—	15.0	—	18.0	ns
tPLH	Propagation Delay	CL = 50pF	—	15.0	—	20.0	—	10.5	—	14.0	ns
tPHL	OE <sub>R</sub> to PARITY	CL = 300pF <sup>(3)</sup>	—	22.5	—	27.5	—	18.0	—	21.5	

**NOTES:**

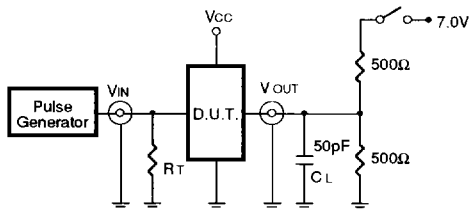
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed but not tested.

2557 tbl 08



## TEST CIRCUITS AND WAVEFORMS

### TEST CIRCUITS FOR ALL OUTPUTS



### SWITCH POSITION

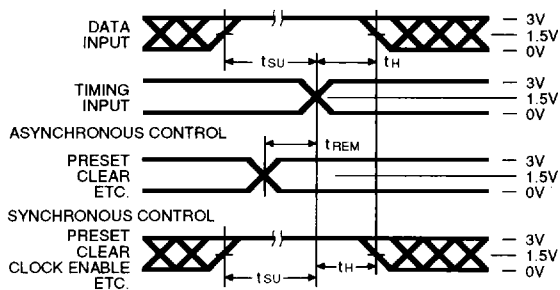
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

#### DEFINITIONS:

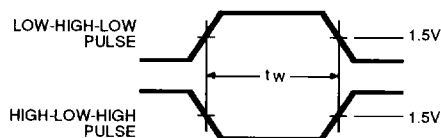
CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to Zout of the Pulse Generator.

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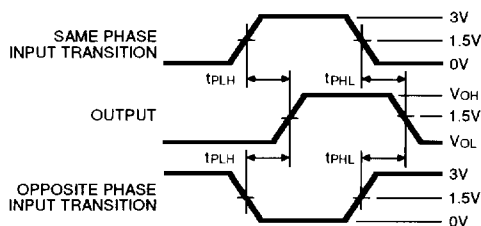
### SET-UP, HOLD AND RELEASE TIMES



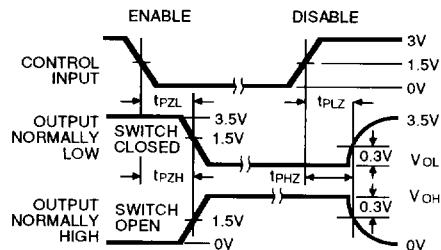
### PULSE WIDTH



### PROPAGATION DELAY



### ENABLE AND DISABLE TIMES

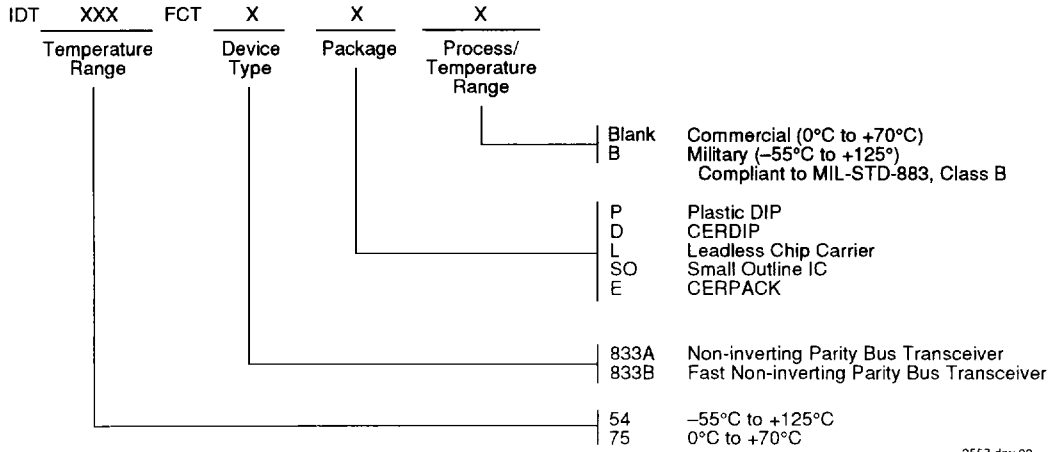


#### NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate  $\leq 1.0$  MHz;  $Z_o \leq 50\Omega$ ;  $t_r \leq 2.5$ ns;  $t_f \leq 2.5$ ns.

2557 drw 04

**ORDERING INFORMATION**



2557 drw 03