TELEDYNE COMPONENTS

4731
4733

3

HIGH-RELIABILITY HYBRID VOLTAGE-TO-FREQUENCY CONVERTERS

FEATURES

- **Power Supply Range ..... ±9V to ±18V**
- **Ultra-Linear**
- **Overrange 100%**
- **Dynamic Range ..... 126 dB**
- **Common-Mode Rejection Ratio ..... 60 dB**
- **Low Full-Scale Drift**
- **Low Zero-Offset Voltage Drift**
- **TTL, CMOS, HNIL Compatible Output**

APPLICATIONS

- **No Drift Integrate/Hold**
- **High Common-Mode Voltage Isolation**
- **2-Wire Digital Transmission**
- **20-Bit Analog-to-Digital Converters**
- **Optical Data Link**

GENERAL DESCRIPTION

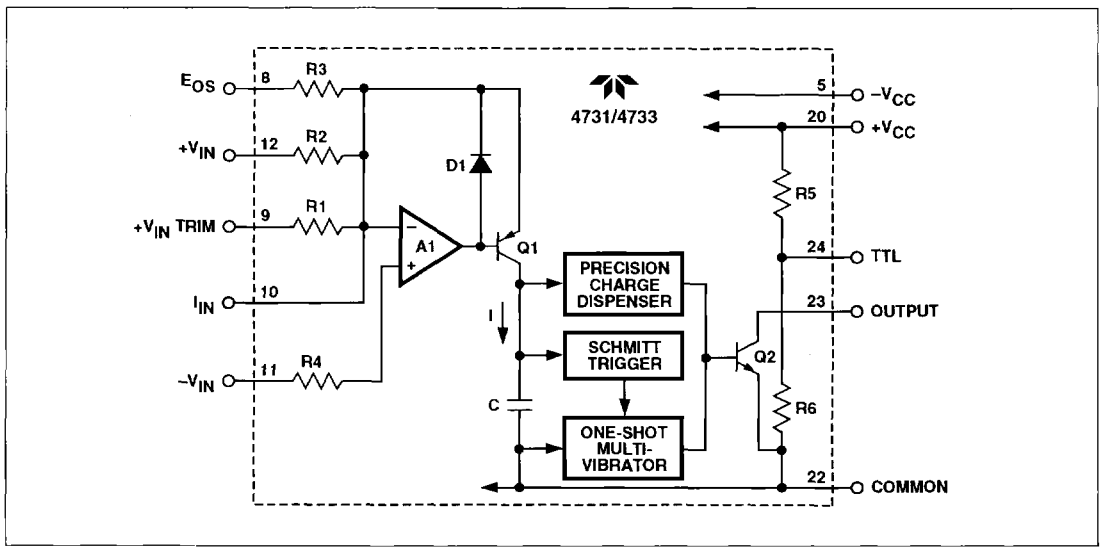
The 4731 and 4733 low-drift voltage-to-frequency (V-to-F) converters produce output pulse trains whose repetition rate is a precision linear function of the input voltage. These low-drift, ultra-linear devices can handle positive, negative and differential input signals, and can operate with a wide range of power supply voltages.

With 126 dB of dynamic range, 70 dB CMRR, and 100% overrange, these devices provide linear operation with input voltages from ±10 μV to +20V. Their current input pin (actually the summing point of an op amp) can resolve currents as low as 1000 pA, making it possible to operate with full-scale input voltages from less than 250 mV to greater than 100V.

Their 0.002% nonlinearity is the equivalent of 16-bit end-point linearity. Differential nonlinearity and dynamic range approach 20 bits.

The 4731 and 4733 are packaged in 24-pin hermetic metal packages. Standard devices are specified for 0°C to +70°C operation. The High Reliability (HR) versions are specified for –55°C to +125°C operation.

SIMPLIFIED BLOCK DIAGRAM

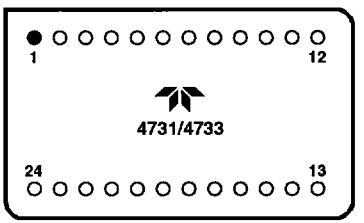


4731
4733

PIN CONFIGURATION

Pin No.	Designation	Pin No.	Designation
1	NC	24	TTL
2	NC	23	f_{OUT}
3	NC	22	COMMON
4	NC	21	NC
5	$-V_{cc}$	20	$+V_{CC}$
6	NC	19	NC
7	NC	18	NC
8	E_{OS}	17	NC
9	$+V_{IN}$ TRIM	16	NC
10	I_{IN}	15	NC
11	$-V_{IN}$	14	NC
12	$+V_{IN}$	13	NC

NC = No internal connection



ABSOLUTE MAXIMUM RATINGS

V_{CC} Power Supplies ..... ±18V
$+V_{IN}$ Positive Input Voltage (Note 1) ..... ±21V
$-V_{IN}$ Negative Input Voltage ..... $\pm V_{CC}$
V_{ID} Differential Input Voltage (Note 1) ..... V_{CC}
I_{IN} Current Input ..... 210 µA
T_C Specified Temperature Range (Case)
4731/4733 ..... 0°C to +70°C
4731-HR/4733-HR ..... –55°C to +125°C
T_{STG} Storage Temperature Range ..... –65°C to +150°C

ELECTRICAL CHARACTERISTICS: T_C = +25°C, $\pm V_{CC}$ = ±15V, unless otherwise indicated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Input						
$+V_{IN}$	Positive Input Voltage		—	10	20	V
$-V_{IN}$	Negative Input Voltage		–8	–10	—	V
V_{CM}	Common-Mode Input Voltage		–7	—	+7	V
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±6V, V_{DIFF} = 0.5V	60	—	—	dB
V_{ID}	Differential Input Voltage	Referenced to $-V_{IN}$ (Note 1)	—	10	—	V
I_{IN}	Current Input Range		.001	—	120	µA
	Input Dynamic Range		100	—	—	dB
V_{OS}	Input Offset Voltage	Adjustable to Zero	—	±1	±5	**mV**
V_{OS}/TC	Input Offset Voltage vs Temperature	–25°C to +85°C	—	±6	±20	µV/°C
		+25°C to +125°C } Typical for standard	—	±20	±100	**µV/°C**
		+25°C to –55°C } tested for HR	—	±20	±50	**µV/°C**
R_{+IN}	$+V_{IN}$ Input Impedance		75	100	125	kΩ
R_{-IN}	$-V_{IN}$ Input Impedance		10	100	—	MΩ
$R_{I\,IN}$	Current Input Impedance	Virtual Ground	—	<0.1	—	Ω

ELECTRICAL CHARACTERISTICS (Cont.)

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
Output							
V_{OH}	Output High Voltage		I_{OH} = 4 mA	**2.4**	—	**5.0**	**V**
V_{OL}	Output Low Voltage		I_{OL} = −16 mA	—	—	**0.4**	**V**
R_O	Output Impedance			2.8	3.5	4.2	kΩ
Transfer							
f_{OUT}	Output Frequency		ΔV_{IN} Equals $V_{IN} - (-V_{IN})$		$[\Delta V_{IN} \times fA] \div 10V$ $[I_{IN} \times fA] \div I_{FS}$		kHz kHz
fA	Scaling Frequency	4731 4733	Adjustable to Typical Adjustable to Typical	**9.95** **99.5**	**10** **100**	**10.05** **100.5**	**kHz** **kHz**
fA/TC	fA vs Temperature	4731	-55°C to +125°C	—	±8	±50	ppm/°C
			-25°C to +85°C	—	±7	±25	ppm/°C
		4733	-55°C to +125°C	—	±12	±50	ppm/°C
			-25°C to +85°C	—	±10	±30	ppm/°C
	fA vs Time	Per Day		—	±10	—	ppm/D
		Per Month		—	±30	—	ppm/M
I_{FS}	Full-Scale Current			75	100	125	µA
I_{FS}/TC	I_{FS} vs Temperature	4731	+25°C to +85°C	—	±4	—	ppm/°C
			+25°C to −25°C	—	±7	—	ppm/°C
		4733	+25°C to +85°C	—	±6	—	ppm/°C
			+25°C to −25°C	—	±10	—	ppm/°C
	I_{FS} vs Time	Per Day		—	±10	—	ppm/D
		Per Month		—	±30	—	ppm/M
$+V_{INLE}$	$+V_{IN}$ Linearity Error (Note 2)		V_{IN} = 100 µV to 12V	—	**±0.002**	**±0.005**	**%FS**
			−55°C to +125°C } Tested for	—	**±0.005**	**±0.03**	**%FS**
			−25°C to +125°C } HR only	—	**±0.005**	**±0.01**	**%FS**
$-V_{INLE}$	$-V_{IN}$ Linearity Error (Note 2)		V_{IN} = −100 µV to $(-V_{CC} + 7V)$	—	±0.01	±0.02	%FS
I_{INLE}	I_{IN} Linearity Error (Note 2)		I_{IN} = 1 nA to 120 µA	—	±0.002	±0.005	%FS
t_{PW}	Output Pulse Width	4731		10	—	30	µs
		4733		1	—	3	µs
	Warm-Up Time		0.01% Accuracy	—	1	—	s
			0.002% Accuracy	—	100	—	s
Dynamic							
t_S	Settling Time			1 to 2 Pulses@New Freq+(5 µs)			
	Overload Recovery		ΔV_{IN} = 100V to 10V or ΔI_{IN} = 1 mA to 0.1 mA	—	0.14	1	ms
Power Supplies							
V_{CC}	Voltage Range			±9	±15	±18	V
	Voltage Asymmetry		$\lvert V_{CC}\rvert - \lvert -V_{CC}\rvert$	—	—	±2	V
I_{CC}	Quiescent Current			—	**±17**	**±25**	**mA**
$PSRR_1$	f_A vs Power Supplies			—	±10	±20	ppm/%
$PSRR_2$	I_{FS} vs Power Supplies			—	±10	±20	ppm/%
$PSRR_3$	V_{OS} vs Power Supplies		Constant Voltage at Pin 8	—	±3	±20	µV/%

NOTES: 1. $+V_{IN}$ has a 100 kΩ internal resistor and a 210 µA maximum input current limit. The voltage input, if current-limited by a series input resistor, is virtually unlimited.
2. Linearity specifications apply only after offset and gain have been trimmed to nominal.
3. Limits printed in **boldface** type are guaranteed and 100% production tested. Limits in normal font are guaranteed but not 100% production tested.

THEORY OF OPERATION

To take maximum advantage of the 4731/4733's versatility, a functional block diagram and theory of operation are provided herein. With this information, input and output circuitry is easily modified to handle virtually any input signal or output load.

The 4731 and 4733 are free-running (astable), voltage-controlled multivibrators (see Block Diagram). The effective currents from the four inputs ($+V_{IN}$, $+V_{IN}$ TRIM, $+I_{IN}$ and E_{OS}) are summed at the inverting input of op-amp A1. A1 and transistor Q1 form a precision current pump, producing current (I). Current charges capacitor C at a rate which is a precise linear function of the device's input signal.

When the voltage impressed on C (due to I) reaches a fixed precision threshold, the Schmitt trigger output changes state and triggers the one-shot (monostable) multivibrator, which in turn produces a single constant-width output pulse. This pulse performs two functions. Amplified by Q2, it is the output of the V-to-F converter and also activates the precision charge dispenser (PCD). The PCD discharges C to the same "zero" level every time an output pulse is produced. Thus, capacitor C is repeatedly charged and discharged between two precise voltages at a rate which is a linear function of the device's voltage and/or current input signal. This action produces the waveforms shown in the timing diagram of Figure 11.

TRIM THEORY

The V-to-F input circuit zero and full-scale trim are performed at the input circuit amp A1 (see block diagram). The user may treat the V-to-F input as an operational amplifier, within certain limits.

No signal combination should be applied to the V-to-F inputs which will drive the A1 output positive. A frequency output will not result if total current into the V-to-F positive inputs (A1, summing point) becomes negative with respect to the V-to-F negative input. If this occurs, D1 becomes forward-biased, Q1 will cut off, and current (I) and f_{OUT} will be zero.

The inherent input current full-scale factor is 100 µA ±25% for a full-scale output. All current adjustment trimming must take this ±25% tolerance into account. Resistor R1 (see block diagram) is factory laser trimmed so that a full-scale input to $+V_{IN}$ TRIM (pin 9) produces an output 101% ±0.5% of nominal full scale; i.e., a +10V input to $+V_{IN}$ TRIM of the 4731 produces a 10.1 kHz ±0.05 kHz output. Resistor R2 is factory trimmed so that $+V_{IN}$ is within ±0.5% of nominal full scale; i.e., a +10V input to $+V_{IN}$ of the 4731 produces a 10 kHz ±0.05 kHz output. Both $+V_{IN}$ and $+V_{IN}$ TRIM inputs are trimmed with and specified for V_{CC} = ±15V at 25°C.

Basic Connections

The 4731 and 4733 are factory trimmed and operate as specified without additional components. Figures 1 and 2 illustrate the basic connections for positive or negative input signals and also show the optional offset adjustment connection. Pin 9 ($+V_{IN}$ TRIM) and pin 12 ($+V_{IN}$) are inputs for positive voltage signals. $+V_{IN}$ is used when accuracy to ±0.1% full scale is acceptable or when external components cannot be accommodated. $+V_{IN}$ TRIM is used when greater full-scale accuracy is required because it allows the use of an external trim adjustment potentiometer. Pin 10 (I_{IN}) is a direct input to the input amplifier summing junction, and is used to input positive-current signals. Its full-scale accuracy is limited to ±25% of the inherent input current full-scale factor mentioned earlier. Pin 11 ($-V_{IN}$) can be used to input negative voltage signals, as shown in Figure 2.

Zero and Full-Scale Trim

When greater accuracy is required, input offset voltage (E_{OS}) is trimmed to zero. For positive inputs only, full-scale output frequency (f_{OUT}) is trimmed to 10 kHz or 100 kHz, depending on the device being used, with external potentiometers (illustrated in Figures 1 and 2). Note that full-scale trim components should have temperature coefficients similar to the full-scale TC of the device being used.

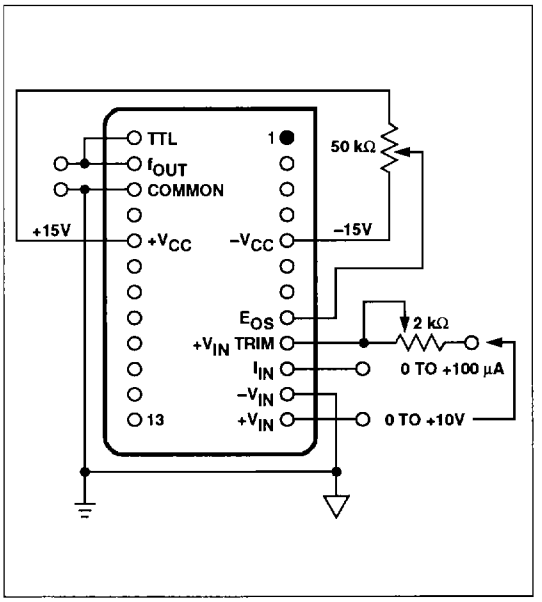


Figure 1. Positive Voltage/Current Inputs

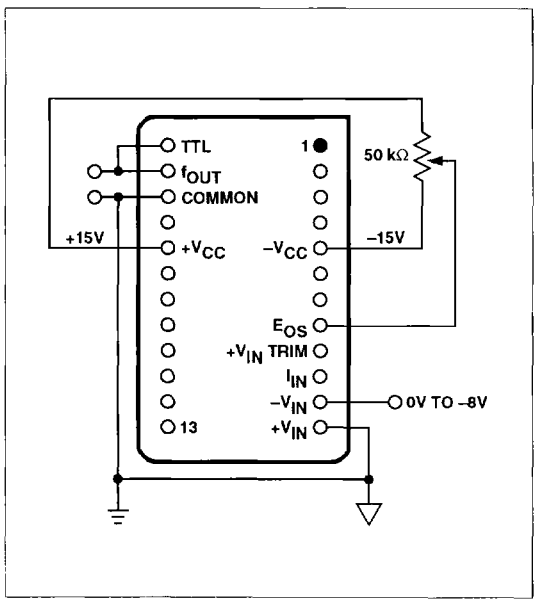


Figure 2. Negative Voltage Input

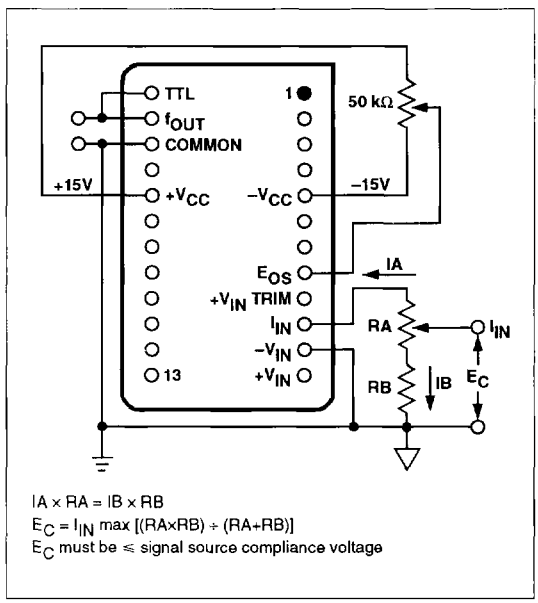


Figure 3. Zero and Full-Scale Trim for Positive Input Currents

TRIM PROCEDURES

1. Apply 10 mV between $+V_{IN}$ and ground. Adjust the 50 kΩ potentiometer to set f_{OUT} equal to 10 Hz (4731) or 100 Hz (4733).
2. Apply +10V between $+V_{IN}$ and ground. Adjust R1 to set f_{OUT} equal to 10 kHz (4731) or 100 kHz (4733).
3. Repeat (1) and (2) until zero and full scale are set precisely. **Note:** Zero is set at 10 Hz to 100 Hz out for 10 mV in, because it is impractical to measure 0 Hz out for 0V in.

Full-scale accuracy for $+I_{IN}$ is ±25%. Greater accuracy is obtained by using the full-scale and zero trim circuit shown in Figure 3. Resistor dividers RA and RB are only used when the actual input current is greater than that necessary to produce a nominal full-scale output frequency.

FULL-SCALE FACTOR CHANGE

The specified input voltage full-scale factor for the 4731 and 4733 is 9.9V ±0.5% with respect to $-V_{IN}$ (or +100 µA ±25% I_{IN}) to produce a full-scale output frequency. Many applications require a full-scale output for other (larger or smaller) full-scale input signals or input polarities. Figures 4, 5 and 6 illustrate how to operate with such input signals.

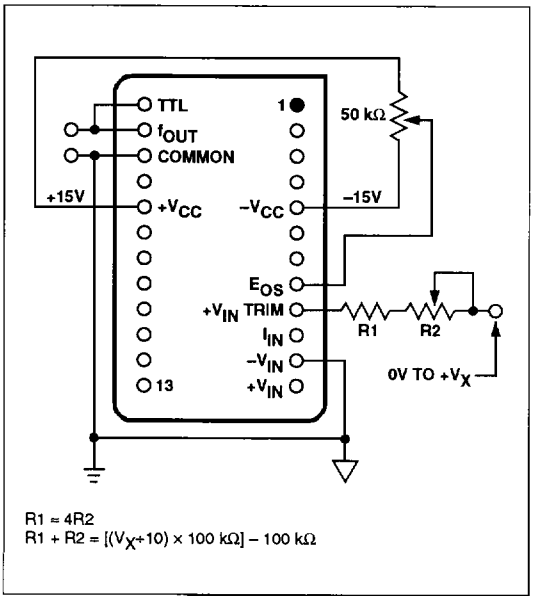
−8V > V_{IN} > +10V

This series of V-to-F converters can be operated with input voltages greater than +10V by connecting a fixed resistor and trim potentiometer in series with the $+V_{IN}$ or $+V_{IN}$ TRIM inputs (see Figure 4). The same effect can be realized by using a properly selected series resistor and inputting the signal to the current input ($+I_{IN}$). For inputs more negative than −8V, the attenuator network of Figure 5 performs well. For either positive or negative inputs the zero trim and other adjustments remain the same as in Figures 1 and 2.

−10V < Full-Scale V_{IN} < +10V

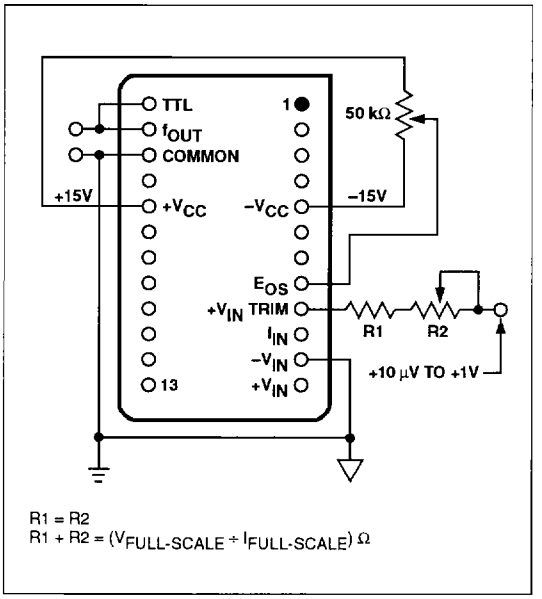
If full-scale input voltage is between +10 µV and +1V, the full-scale output is set to nominal full scale by using the current-input terminal with a series resistor, as shown in Figure 6.

If full-scale input signal is between −10V and −10 µV, a low-drift amplifier (such as the 1435) should be used to amplify the signal full scale to −10V, or even +10V, and then apply the signal as usual (i.e., Figures 1 and 2). This preamplification technique can also be used with positive input signals.



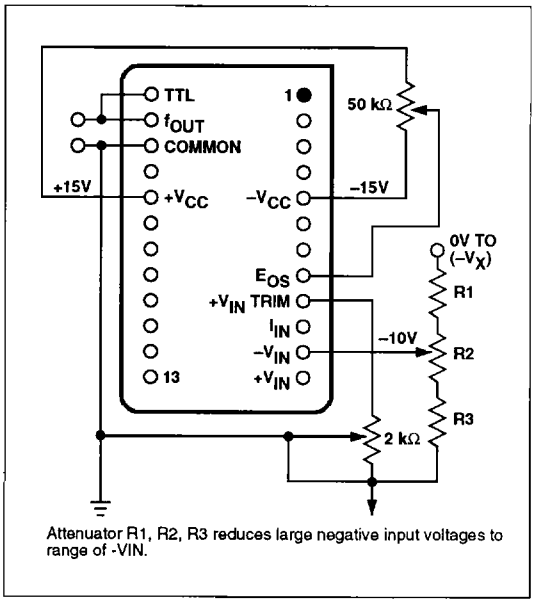
R1 ≈ 4R2
R1 + R2 = [(VX÷10) x 100 kΩ] – 100 kΩ

Figure 4. Full Scale $+V_{IN}$ Greater Than +10V



R1 = R2
R1 + R2 = ($V_{FULL-SCALE}$ ÷ $I_{FULL-SCALE}$) Ω

Figure 6. Full-Scale Output for Less Than Full-Scale Input



Attenuator R1, R2, R3 reduces large negative input voltages to range of -VIN.

Figure 5. Full-Scale Input More Negative Than –8V

Reduced Full-Scale f_{OUT}

In some applications, a reduced full-scale output frequency is required when the input signal is ±10V or greater. The circuits of Figures 4 and 5 show attenuation of an overrange input signal can also be used to attenuate a nominal ±10V input signal below ±10V, thereby reducing the full-scale f_{OUT} below nominal 10 kHz to 100 kHz.

To make maximum use of the device's dynamic range, the input signal should be conditioned to ±10V full scale and a binary (or BCD) frequency divider (counter) should be connected to the output. Any TTL, CMOS, or HNIL device may be used, from a simple ÷10 unit (such as the TTL 54/74 90A), to a programmable divider (such as the CMOS CD4059), which can divide by any number from 3 to 15,999.

If the V-to-F output is set at its nominal full scale, the output of the counter (shown in Figure 7) will be 1 kHz (4731) or 10 kHz (4733). Likewise, the minimum output frequency will be 1 MHz or 10 MHz, respectively.

Full-Scale Input Currents Greater Than +100 μA

If the full-scale input current is greater than nominal, the "current splitter" circuit of Figure 8 can be used. As noted in Figure 3, the voltage developed at the wiper of potentiometer RA must be less than the compliance voltage of the

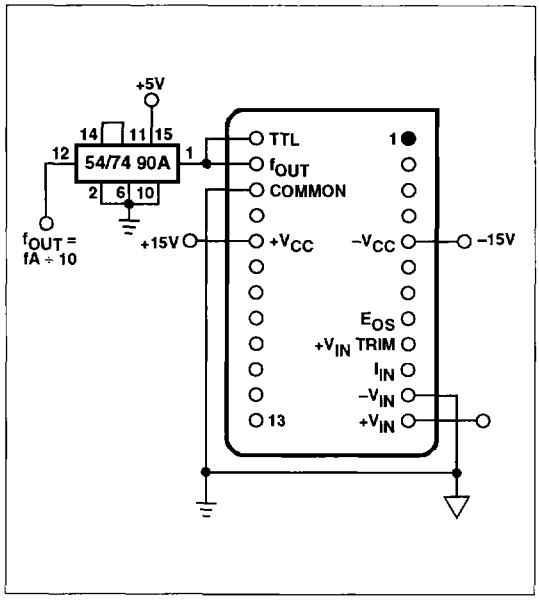


Figure 7. Reduced Full-Scale Output for $V_{IN} \geq 10V$

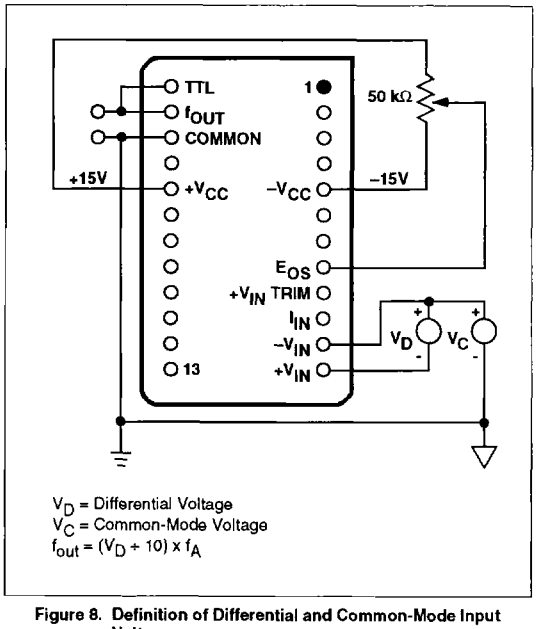


Figure 8. Definition of Differential and Common-Mode Input Voltages

current source. A negative-input current can be conditioned by passing it through a resistor connected between $-V_{IN}$ and signal common, thereby producing a negative voltage. The compliance voltage of the current source must be greater than the maximum voltage developed across the resistor.

The best way to condition current signals is with the classic op-amp current-to-voltage converter circuit. With this circuit and the "right" amplifier, virtually any current (even femtoamps) will provide a positive or negative 10V full-scale input to the V-to-F without compliance voltage problems.

Differential Inputs

The $+V_{IN}$ and $-V_{IN}$ terminals represent true differential inputs capable of accepting signals from a balanced line, a thermistor bridge or a signal source sitting at a common-mode voltage. The device's differential input eliminates the need for a differential preamplifier.

To use the voltage inputs differentially, some simple conventions (definitions) must be observed. Illustrated in Figure 8, they are:

1. Common-mode voltage (CMV) is defined as the voltage between $\pm V_{CC}$ common and $-V_{IN}$.
2. $+V_{IN}$ must always be positive with respect to $-V_{IN}$.
3. CMV range is typically between $+V_{CC}-4V$ and $-V_{CC}+5V$.
4. The differential (floating, balanced) signal source must be returned to $\pm V_{CC}$ common and must not create voltages exceeding the limits set in (1), (2) or (3).
5. f_{OUT} $= (+V_{IN}) - (-V_{IN}) \times fA/10V\ fA$
   $= 10$ kHz (4731)
   $= 100$ kHz (4733)

Operation With Bipolar Input Signals

The V-to-F converter cannot operate with bipolar (i.e., –5V to +5V) input signals when connected as shown in Figures 1 and 2. To handle bipolar inputs it is necessary to offset the zero (i.e., produce a pulse train out for "zero" volts in).

For example, if $+V_{IN}$ is connected to 0V and $-V_{IN}$ is connected to a fixed –5V, the device's output will be "offset" to either 5 kHz (4731) or 50 kHz (4733) for a 0V input. If $+V_{IN}$ is –5V, f_{OUT} will be 0 Hz; if $+V_{IN}$ is 0V, f_{OUT} is 5 kHz or 50 kHz; if $+V_{IN}$ is +5V, f_{OUT} is 10 kHz or 100 kHz.

The offset may be performed at $+V_{IN}$ (pin 12) and the signal applied to either $-V_{IN}$ (pin 11) or I_{IN} (pin 10); or I_{IN} may be used to inject the fixed offset. Offsetting may be combined with all of the adjustment techniques, shown in Figures 1 through 10, to provide signal conditioning for almost any practical input signal.

Eliminating Common-Mode Signals

An input signal is often a small voltage change impressed on a larger fixed voltage. This situation is handled by nulling (offsetting) the DC or unchanging component of the input signal at one input and adjusting the full-scale gain factor at another, so the variable portion of the input signal causes f_{OUT} to cover the full excursion from 0 Hz to full scale; i.e., an input signal that is a voltage varying between +4V and +6V. To implement offsetting, connect $+V_{IN}$ to −4V. Since the actual signal is 2V (6V–4V), connect it to $+I_{IN}$ in series with resistor and trim potentiometer chosen to generate 100 µA of input current from the 2V signal (see Figure 5).

When input varies between +5V and +15V (signal = 10V), implement offsetting by connecting $-V_{IN}$ to +5V and apply the signal to $+V_{IN}$. Trim the V-to-F per Figure 1. If the input varies between +30V and +50V (signal = 20V), implement offsetting by connecting −30V to $+I_{IN}$ through a 150 kΩ resistor and series potentiometer. Connect the 20V signal to $+V_{IN}$ or $+V_{IN}$ TRIM.

Operation With Fast Signals

A V-to-F application may require operation with rapidly changing input signals. For example, the output of a load cell may change from 0 to full scale (or full scale to 0) in 1 ms. To accurately handle this signal, the output of the V-to-F converter must be able to change faster than the input.

The basic response (or settling time) of the V-to-F converter for voltage inputs is one period of the new frequency +5 µs. Response time is either 1s (4731) or 0.1s (4733) +5 µs.

Using the 4731 as an example: When the input changes from 0V to 10V, the new frequency is 10 kHz, one period is 100 µs, and response time is 105 µs. However, if the signal changes from full scale to 0V, the new period is much longer than the required 1 ms (theoretically it is infinite).

If the V-to-F output is to change in 1 ms, the output frequency for 0V in must be offset to a new frequency, the period of which is less than the 1 ms required for the application described. The full-scale value of the input signal is adjusted so the V-to-F converter will operate between the chosen offset or zero frequency and the maximum full-scale frequency.

In Figure 9 a 4731 is offset so that a 0V to +1V signal produces an output which varies between 9 kHz and 10 kHz with a response time of 116 µs (maximum) in either direction. Offsetting the V-to-F output range in this manner has the effect of reducing the settling/response time to the required level.

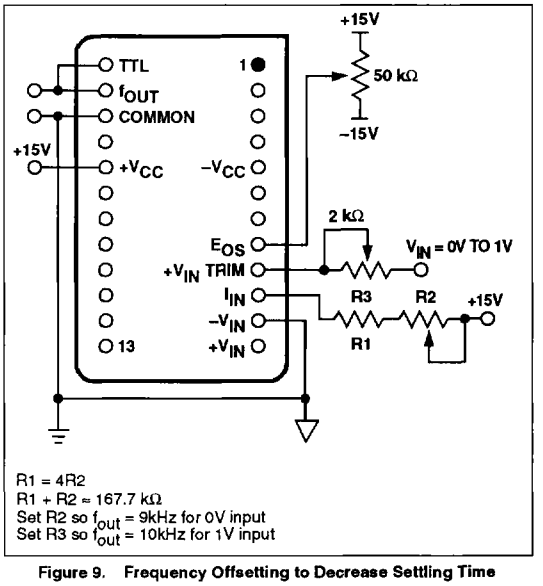


Figure 9. Frequency Offsetting to Decrease Settling Time

TTL Output Characteristics

The TTL-level pulse train from the V-to-F converter is designed to drive at least one TTL load over the power supply range +9V to +18V. At +15V, it can drive 10 TTL loads. The output circuit (see block diagram) is a single transistor (Q2) connected as a saturated switch with pull-up resistor (R5). When Q2 is on, the output is at "zero" volts. When Q2 is off, the output voltage is $(+V_{CC}+3)$, assuming pins 23 and 24 are connected together. (If pin 23 is not connected to pin 24, an external divider must be provided which will determine the high output voltage.)

CMOS or HNIL Logic

The 4731 and 4733 output circuits are easily adapted to drive CMOS or HNIL. It is only necessary to parallel R5 (see block diagram) with a 1 kΩ resistor. This additional pull-up resistor also decreases pulse rise time, enabling these devices to drive larger capacitive loads. If pin 23 is not connected to pin 24, an external divider must be provided.

Output Protection

The V-to-F output (collector of Q2) may be shorted to ground indefinitely without damage; however, since Q2 is ON most of the time, a short to $+V_{CC}$ will cause certain catastrophic failure in about 5s. A short to TTL (pin 24) and $-V_{CC}$ (pin 5) simultaneously will cause instant catastrophic failure.

Square-Wave Output

The outputs of the 4731 and 4733 are a train of pulses 20 µs or 2 µs wide, respectively (see Figure 11). A symmetrical (square wave) output for driving highly capacitive or noisy transmission lines can be obtained with a D-type or JK flip-flop, as shown in Figure 10. The square-wave output has a frequency equal to 1/2 the V-to-F output frequency.

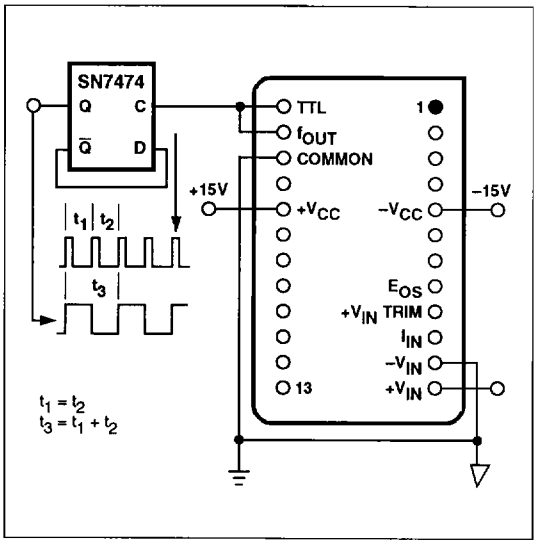
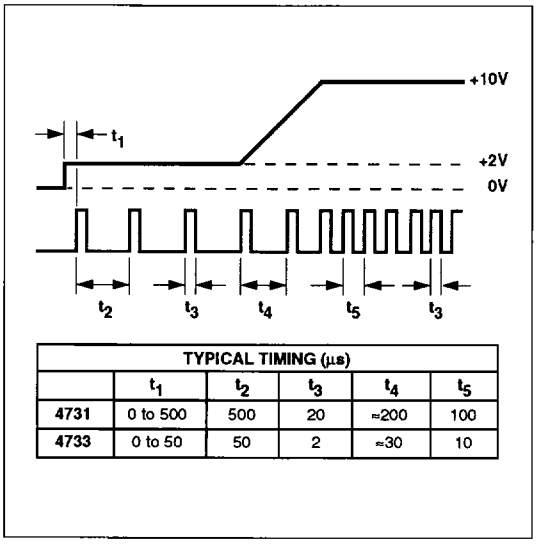


Figure 10. Square-Wave Output Using D-Type Flip-Flop



TYPICAL TIMING (µs)					
	t_1	t_2	t_3	t_4	t_5
4731	0 to 500	500	20	≈200	100
4733	0 to 50	50	2	≈30	10

Figure 11. Typical Timing Relationships