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FPD750SOT343E

LOW-NOISE HIGH-LINEARITY PACKAGED pHEMT

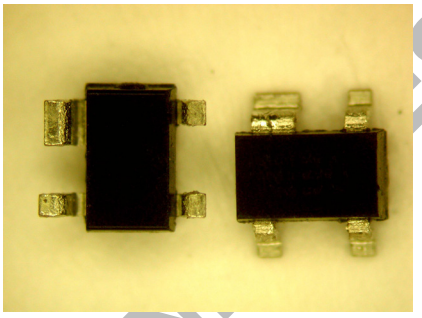
Package: SOT343

Product Description

The FPD750SOT343CE is a packaged depletion mode pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a 0.25µmx750µm Schottky barrier gate. RFMD's 0.25µm process ensures class-leading noise performance. The use of a small footprint plastic package allows for cost effective system implementation.

Optimum Technology Matching® Applied

- ☐ GaAs HBT
- ☐ GaAs MESFET
- ☐ InGaP HBT
- ☐ SiGe BiCMOS
- ☐ Si BiCMOS
- ☐ SiGe HBT
- ☑ GaAs pHEMT
- ☐ Si CMOS
- ☐ Si BJT
- ☐ GaN HEMT
- ☐ InP HBT
- ☐ RF MEMS
- ☐ LDMOS



Features

(at 1850MHz)

- 0.5dB NF Min
- 20dBm Output Power (P1dB)
- 16.5dB Small-Signal Gain (SSG)
- 37dBm Output IP_3
- RoHS-compliant (Directive 2002/95/EC)

Applications

- 802.11a, b, g and WiMAX LNAs
- PCS/Cellular High Linearity LNAs
- Other Types of Wireless Infrastructure Systems.

RF Parameter	Typical Performance				Unit	Condition
	0.9GHz	1.85GHz	2.6GHz	3.5GHz		
OP_{1dB} at Gain Compression	20	19	20	20.5	dBm	V_{DS}=3.3V, I_{DS}=40mA
Small-Signal Gain (SSG)	22	16.5	14	11	dB	V_{DS}=3.3V, I_{DS}=40mA
PAE	50	45	45	50	%	V_{DS}=3.3V, I_{DS}=40mA, $P_{OUT}=P_{1dB}$
Maximum Stable Gain (|S21/S12|)	24	20	18	16	dB	V_{DS}=3.3V, I_{DS}=40mA
Noise Figure (NF)	0.5	0.6	0.7	0.8	dB	V_{DS}=3.3V, I_{DS}=40mA
OIP_3 (15dB to 5dB below P_{1dB})	32	31	31	32	dBm	V_{DS}=3.3V, I_{DS}=40mA
	35	37	35	38	dBm	V_{DS}=3.3V, I_{DS}=80mA, P_{OUT}=9dBm per tone

*Note: Based on measured data taken on applications circuits.

RF/DC Parameter	Electrical Specification			Unit	Condition
	Min.	Typ.	Max.		
Frequency		2.0		GHz	
OP_{1dB} at Gain Compression	17			dBm	V_{DS}=3.3V, I_{DS}=40mA
Small-Signal Gain (SSG)	16			dB	V_{DS}=3.3V, I_{DS}=40mA
Saturated Drain-Source Current (I_{DSS})	185	230	280	mA	V_{DS}=1.3V, V_{GS}=0V
Transconductance (GM)		200		ms	V_{DS}=1.3V, V_{GS}=0V
Pinch-Off Voltage (V_P)	|0.7|	|1.0|	|1.3|	V	V_{DS}=1.3V, I_{DS}=0.75mA
Gate-Source Breakdown Vltg (V_{BDGS})	|13|	|16|		V	I_{GS}=0.75mA
Gate-Drain Breakdown Vltg (V_{BDGD})	|13|	|18|		V	I_{DS}=0.75mA
Thermal Resistivity (θJC) *		143		°C/W	V_{DS}>3V

*Note: All devices are 100% RF and DC tested at 2GHz with $Z_S=Z_L=50\Omega$. $T_{AMBIENT}$=22°C.

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Absolute Maximum Ratings[1]

Parameter	Rating	Unit
Drain-Source Voltage (V_{DS}) ($-3V<V_{GS}<-0.5V$)	6	V
Gate-Source Voltage (V_{GS}) ($0V<V_{DS}<+8V$)	-3	V
Drain-Source Current (I_{DS}) (For $V_{DS}>2V$)	I_{DSS}	
Gate Current (I_G) (Forward or reverse)	7.5	mA
RF Input Power (P_{IN})[2] (Under any acceptable bias state)	22	dBm
Channel Operating Temperature (T_{CH}) (Under any acceptable bias state)	175	°C
Storage Temperature (T_{STG}) (Non-Operating Storage)	-55 to 150	°C
Total Power Dissipation (P_{TOT})[3, 4, 5]	1.1	W
Gain Compression (Under any bias conditions)	5	dB
Simultaneous Combination of Limits[6] (2 or more max. limits)	80	%

Notes:
[1] $T_{AMBIENT}$ = 22 °C unless otherwise noted; exceeding any one of these absolute maximum ratings may cause permanent damage to the device.
[2] Max. RF input limit must be further limited if input VSWR > 2.5:1.
[3] Users should avoid exceeding 80% of 2 or more Limits simultaneously.
[4] Total Power Dissipation (P_{TOT}) defined as $(P_{DC}+P_{IN})-P_{OUT}$, where P_{DC}: DC Bias Power, P_{IN}: RF Input Power, P_{OUT}: RF Output Power.
Total Power Dissipation to be de-rated as follows above 22 °C:
$P_{TOT} = 1.1-(1/\theta JC) \times T_{PACK}$, where T_{PACK} = source tab lead temperature above 22 °C and θJC = 143 °C/W.

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

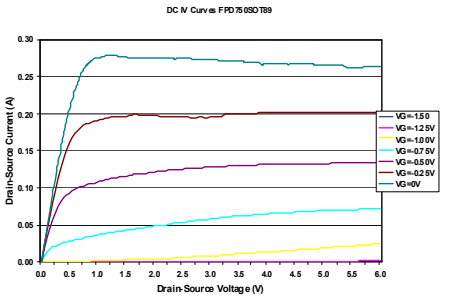
RoHS status based on EUDirective2002/95/EC (at time of this document revision).

Biasing Guidelines

Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that gate bias is applied before drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional Information.

Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices.

For standard Class A operation, a 50% of I_{DSS} bias point is recommended. A small amount of RF gain expansion prior to onset of compression is normal for this operating point. A class A/B bias of 25% to 33% offers an optimized solution for NF and OIP_3.



Note: The recommended method for measuring I_{DSS}, or any particular I_{DS}, is to set the drain-source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented). Setting the $V_{DS} > 1.3V$ will generally cause errors in the current measurements, even in stabilized circuits.

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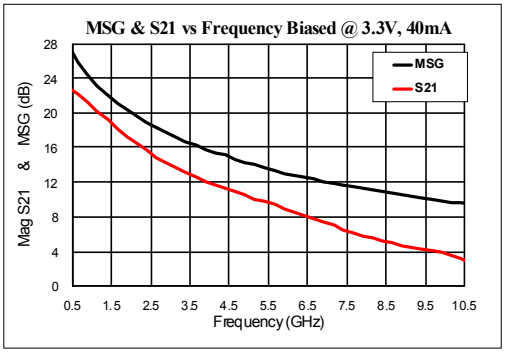
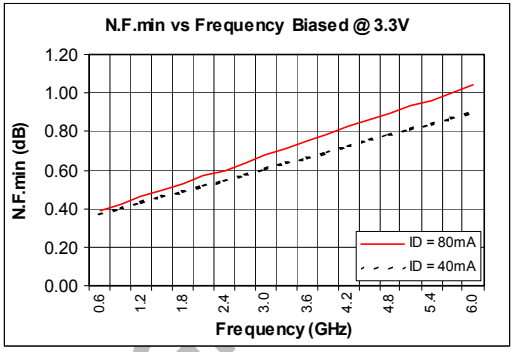
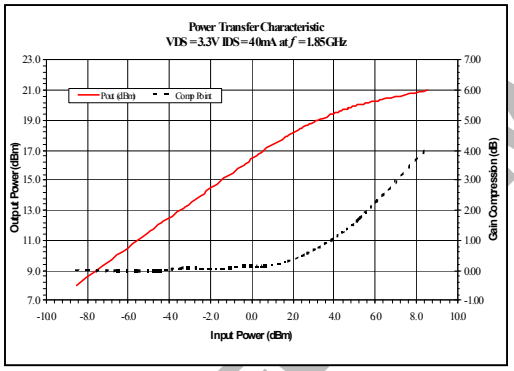
Typical Frequency Response

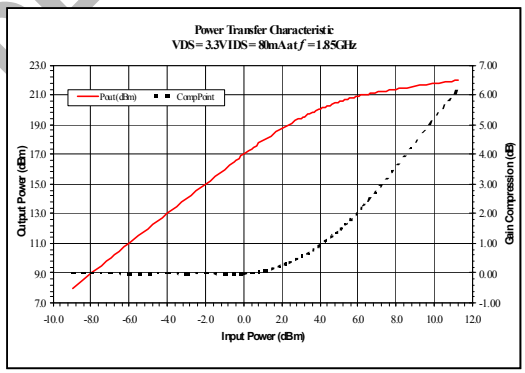




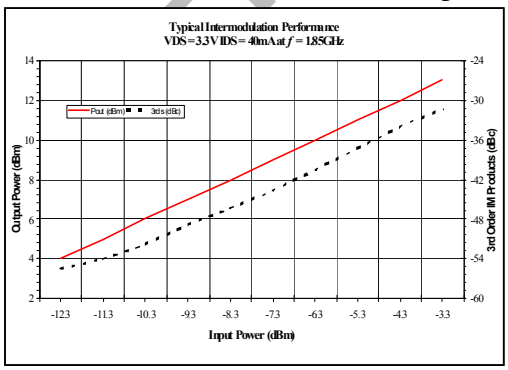
Note: Typical gain and noise figure variation against frequency is shown above. The devices were biased nominally at V_{DS}=3.3V, I_{DS}=40mA. The test devices were tuned for minimum noise figure and maximum gain using tuners at the device input and output ports.

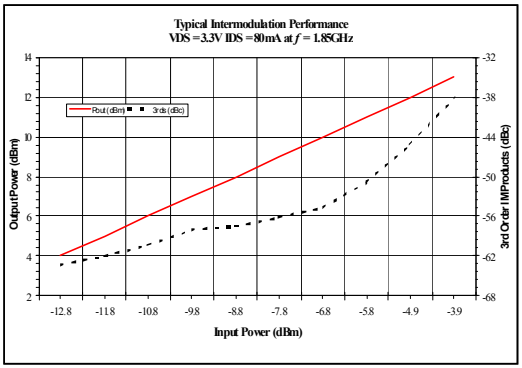
Typical RF Performance at 1.85GHz





Note: Typical power transfer curves at two bias conditions are shown above. The data is taken with the device mounted on evaluation board tuned at 1.85GHz for low noise and gain as shown in the reference design included in this document.





Note: Typical intermodulation performance is shown above. The data is taken with the device mounted on evaluation board tuned at 1.85GHz for low noise and gain as shown in the 1.85GHz reference design in this document. The FPD750SOT343CE

has enhanced Intermodulation performance with an OIP_3 value of up to P1dB+16dBm. This effect can be seen when the device is biased at I_D=80mA by the bough in the 3rd order product plot line.

Noise Parameters

Biased at V_{DS}=3.3V, I_{DS}=40mA

Freq. (GHz)	N.F.min (dB)	Γopt		Rn/50
		Mag	Angle	
0.60	0.37	0.770	12.2	0.108
0.90	0.40	0.689	21.2	0.100
1.20	0.43	0.614	30.6	0.092
1.50	0.46	0.546	40.4	0.084
1.80	0.49	0.485	50.6	0.077
2.10	0.52	0.431	61.1	0.069
2.40	0.55	0.383	72.1	0.063
2.70	0.58	0.342	83.4	0.057
3.00	0.61	0.307	95.1	0.053
3.30	0.64	0.280	107.2	0.049
3.60	0.67	0.258	119.8	0.046
3.90	0.70	0.244	132.7	0.043
4.20	0.73	0.236	146.0	0.042
4.50	0.76	0.236	159.6	0.040
4.80	0.78	0.242	173.7	0.040
5.10	0.81	0.254	-171.9	0.041
5.40	0.84	0.273	-157.0	0.044
5.70	0.87	0.299	-141.8	0.050
6.00	0.90	0.332	-126.1	0.061

Biased at V_{DS}=3.3V, I_{DS}=80mA

Freq. (GHz)	N.F.min (dB)	Γopt		Rn/50
		Mag.	Angle	
0.60	0.39	0.732	11.5	0.129
0.90	0.42	0.644	22.1	0.115
1.20	0.46	0.564	33.0	0.102
1.50	0.50	0.492	44.2	0.090
1.80	0.53	0.428	55.9	0.079
2.10	0.57	0.372	67.9	0.070
2.40	0.60	0.324	80.2	0.063
2.70	0.64	0.283	93.0	0.057
3.00	0.68	0.251	106.2	0.053
3.30	0.71	0.227	119.7	0.050
3.60	0.75	0.210	133.6	0.049
3.90	0.79	0.202	147.9	0.048
4.20	0.83	0.201	162.5	0.048
4.50	0.86	0.208	177.5	0.049
4.80	0.90	0.223	-167.1	0.051
5.10	0.94	0.247	-151.4	0.056
5.40	0.97	0.277	-135.2	0.065
5.70	1.01	0.317	-118.7	0.080
6.00	1.05	0.364	-101.8	0.106

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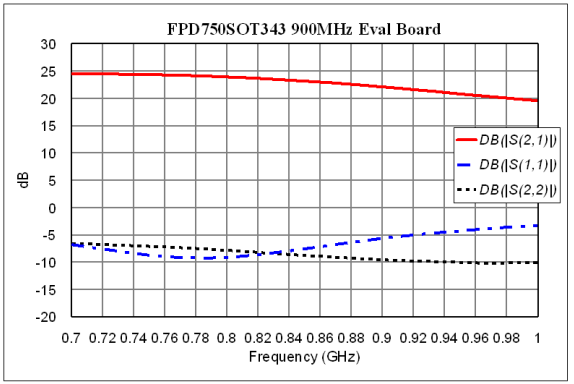
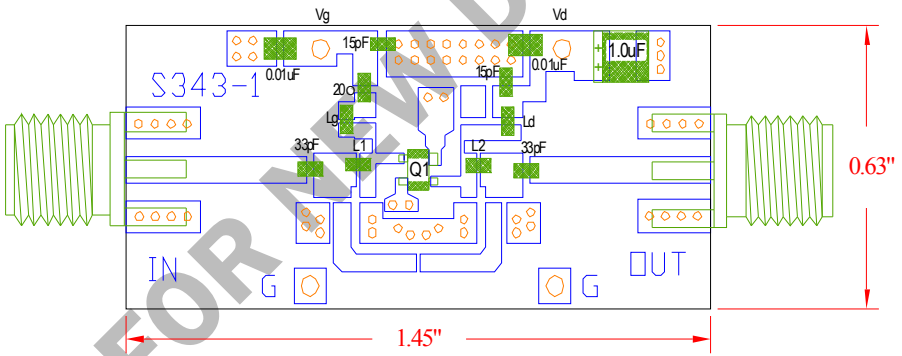
Reference Design (0.9 GHz)

Parameter	Typical	Unit
Gain	22	dB
P1dB	20	dBm
OIP_3	32	dBm
NF	0.5	dB
S11	-5	dB
S22	-10	dB
V_D	3.3	V
V_G	-0.4 to -0.6	V
I_D	40	mA



Note: OIP_3 measured at P_{OUT} of 9dBm per tone.

Evaluation Board Layout

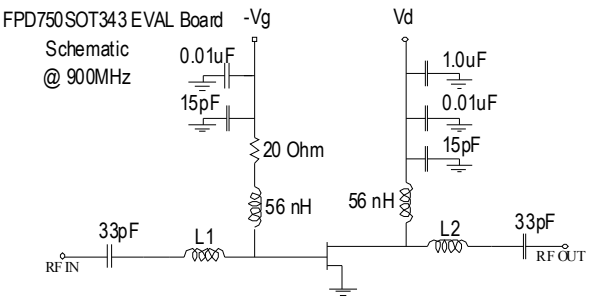


Component Values

Component	Value	Description
Lg	56nH	LL 1608 Toko chip inductor
Ld	56nH	LL 1608 Toko chip inductor
L1	15nH	LL 1608 Toko chip inductor
L2	4.7nH	LL 1608 Toko chip inductor

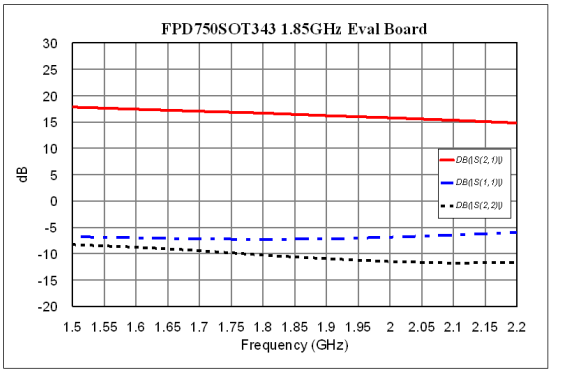
Evaluation board material: 31mil thick FR4 with 1/2oz. Cu on both sides.

DC blocking capacitors are ATC series 600S. A tantalum 1.0µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20Ω chip resistor from Vishay is used on the gate DC bias line for stability.



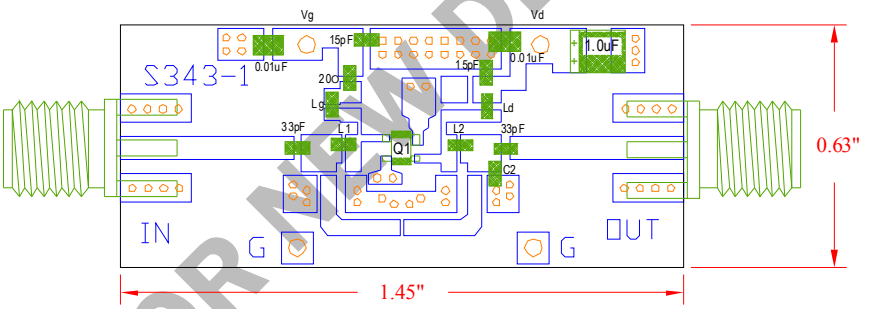
Reference Design (1.85GHz)

Parameter	Typical	Unit
Gain	16.5	dB
P1dB	19	dBm
OIP_3	31	dBm
NF	0.6	dB
S11	-6	dB
S22	-10	dB
V_D	3.3	V
V_G	-0.4 to -0.6	V
I_D	40	mA



Note: OIP_3 measured at P_{OUT} of 9dBm per tone.

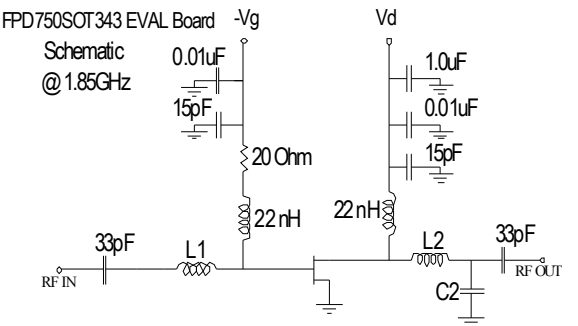
Evaluation Board Layout



Component Values

Component	Value	Description
Lg	22nH	LL 1608 Toko chip inductor
Ld	22nH	LL 1608 Toko chip inductor
L1	2.2nH	LL 1005 Toko chip inductor
L2	1.8nH	LL 1005 Toko chip inductor
C2	1.0pF	ATC 600S chip inductor

Evaluation board material: 31mil thick FR4 with 1/2oz. Cu on both sides.



DC blocking capacitors are ATC series 600S. A tantalum 1.0µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20Ω chip resistor from Vishay is used on the gate DC bias line for stability.

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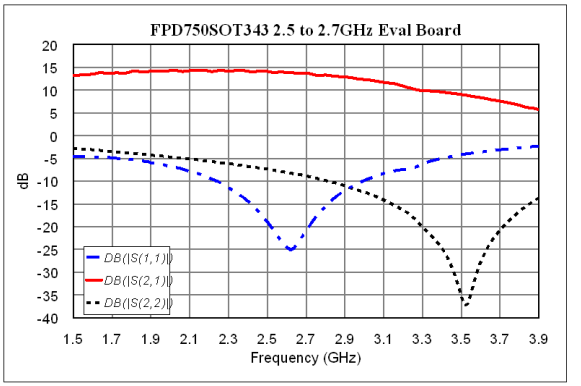
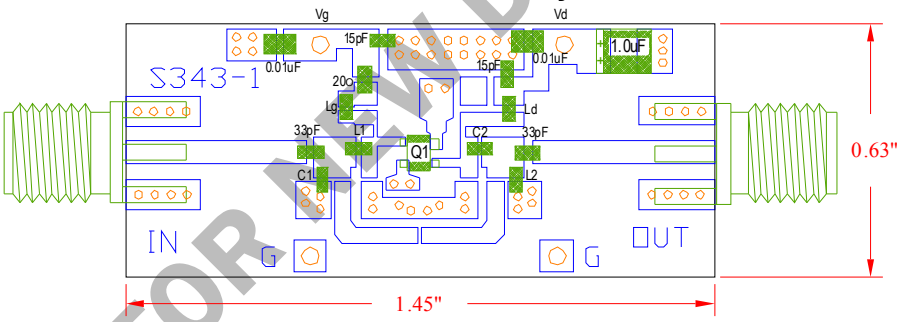
Reference Design (2.6GHz)

Parameter	2.5	2.6	2.7	Unit
Gain	14.2	14	13.5	dB
P1dB	20	21	21	dBm
OIP_3	30.5	31	31	dBm
NF	0.8	0.7	0.75	dB
S11	-20	-25	-20	dB
S22	-7	-8	-10	dB
V_D	3.3			V
V_G	-0.4 to -0.6			V
I_D	40			mA



Note: OIP_3 measured at P_{OUT} of 9dBm per tone.

Evaluation Board Layout

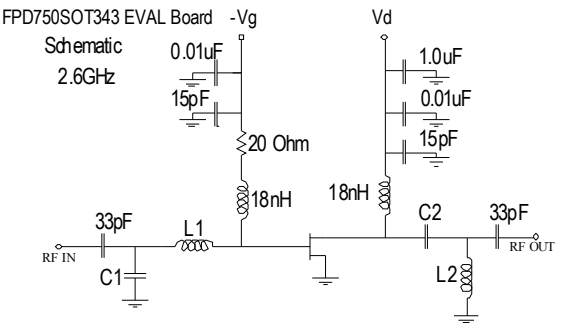


Component Values

Component	Value	Description
Lg	18nH	LL 1608 Toko chip inductor
Ld	18nH	LL 1608 Toko chip inductor
L1	1.2nH	LL 1005 Toko chip inductor
L2	2.7nH	LL 1005 Toko chip inductor
C1	1.0pF	ATC 600S chip inductor
C2	1.8pF	ATC 600S chip inductor

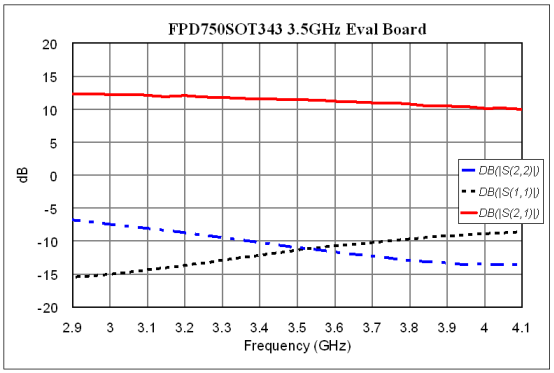
Evaluation board material: 31mil thick FR4 with 1/2oz. Cu on both sides.

DC blocking capacitors are ATC series 600S. A tantalum 1.0µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20Ω chip resistor from Vishay is used on the gate DC bias line for stability.



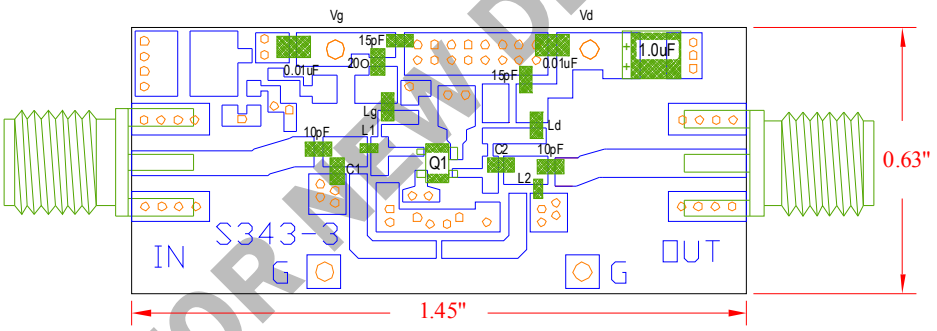
Reference Design (3.5GHz)

Parameter	3.5	Unit
Gain	11	dB
P1dB	20.5	dBm
OIP_3	32	dBm
NF	0.75	dB
S11	-11	dB
S22	-11	dB
V_D	3.3	V
V_G	-0.4 to -0.6	V
I_D	40	mA



Note: OIP_3 measured at P_{OUT} of 9dBm per tone.

Evaluation Board Layout

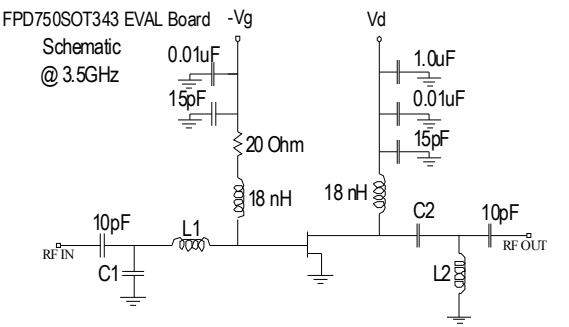


Component Values

Component	Value	Description
Lg	18nH	LL 1608 Toko chip inductor
Ld	18nH	LL 1608 Toko chip inductor
L1	1.0nH	0402CS Coil Cr. inductor
L2	2.7nH	0402CS Coil Cr. inductor
C1	0.3pF	ATC 600S chip inductor
C2	0.8pF	ATC 600S chip inductor

Evaluation board material: 31mil thick Rogers 4003 with 1/2oz. Cu on both sides.

DC blocking capacitors are ATC series 600S. A tantalum 1.0µF is used at the drain terminal. All other capacitors are 0603 and 0805 standard chip capacitors. A 0603 size 20Ω chip resistor from Vishay is used on the gate DC bias line for stability.



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S-Parameters

(Biased at 3V, 40mA)

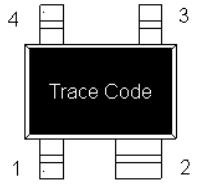
Freq	S11		S21		S12		S22	
(GHz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
0.60	0.875	-51.0	12.561	139.4	0.034	67.2	0.294	-40.8
0.90	0.788	-72.8	11.024	123.3	0.046	59.0	0.248	-59.5
1.20	0.707	-92.2	9.608	110.0	0.057	53.0	0.216	-76.2
1.50	0.641	-109.4	8.377	98.5	0.065	48.1	0.186	-91.7
1.80	0.590	-124.7	7.354	88.5	0.072	44.2	0.162	-106.8
2.10	0.557	-138.4	6.547	79.6	0.079	40.6	0.150	-121.3
2.40	0.532	-151.0	5.881	71.5	0.086	37.5	0.138	-133.8
2.70	0.515	-162.2	5.341	64.0	0.092	34.3	0.132	-145.4
3.00	0.501	-172.8	4.886	56.9	0.099	31.2	0.126	-155.7
3.30	0.491	178.2	4.519	50.2	0.105	28.2	0.119	-164.8
3.60	0.484	169.6	4.202	43.6	0.112	24.9	0.116	-175.0
3.90	0.484	161.3	3.950	37.2	0.118	21.5	0.110	176.0
4.20	0.483	153.4	3.728	30.7	0.125	17.9	0.107	165.7
4.50	0.489	145.3	3.525	24.1	0.131	14.0	0.110	153.9
4.80	0.494	136.9	3.340	17.5	0.137	9.8	0.115	142.7
5.10	0.503	128.7	3.173	11.1	0.143	5.6	0.125	129.9
5.40	0.515	120.5	3.020	4.5	0.148	1.2	0.141	119.8
5.70	0.528	112.3	2.874	-2.2	0.153	-3.4	0.161	110.4
6.00	0.545	104.4	2.725	-8.8	0.156	-8.0	0.185	101.6

S-Parameters

(Biased at 3V, 80mA)

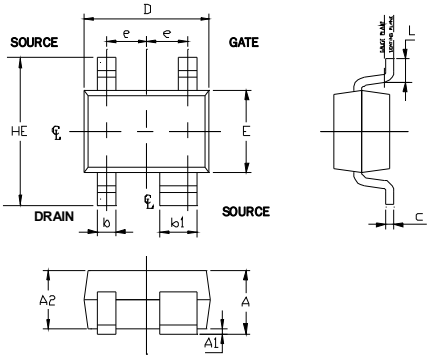
Freq	S11		S21		S12		S22	
(GHz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
0.60	0.852	-53.8	14.400	137.0	0.029	69.0	0.256	-38.6
0.90	0.755	-76.0	12.398	120.7	0.039	62.1	0.210	-55.1
1.20	0.671	-95.6	10.653	107.5	0.048	57.1	0.180	-69.8
1.50	0.605	-112.6	9.200	96.4	0.056	53.2	0.151	-82.8
1.80	0.556	-127.8	8.027	86.7	0.063	49.8	0.128	-96.3
2.10	0.525	-141.4	7.115	78.1	0.071	46.5	0.115	-109.7
2.40	0.502	-153.7	6.372	70.3	0.078	43.5	0.104	-121.0
2.70	0.487	-164.7	5.773	63.0	0.085	40.5	0.097	-132.3
3.00	0.475	-175.1	5.272	56.2	0.091	37.3	0.090	-141.3
3.30	0.465	176.1	4.868	49.6	0.098	34.3	0.083	-149.7
3.60	0.459	167.8	4.522	43.2	0.105	30.9	0.079	-159.5
3.90	0.458	159.6	4.246	37.0	0.112	27.5	0.073	-167.0
4.20	0.459	152.1	4.006	30.6	0.119	23.9	0.068	-177.9
4.50	0.464	144.2	3.787	24.2	0.126	19.9	0.069	169.0
4.80	0.469	136.1	3.588	17.8	0.132	15.7	0.071	154.1
5.10	0.479	128.2	3.408	11.5	0.138	11.5	0.079	137.9
5.40	0.492	120.1	3.246	5.1	0.144	7.0	0.094	125.7
5.70	0.506	112.2	3.094	-1.5	0.149	2.3	0.113	114.4
6.00	0.524	104.4	2.937	-8.0	0.153	-2.3	0.138	105.2

Branding Diagram



Package Outline

Dimensions in Millimeters

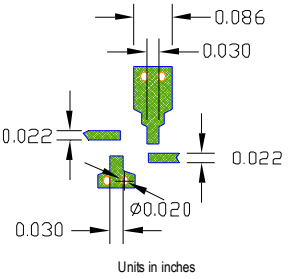


SYMBOL	MIN	MAX
E	1.15	1.35
D	1.85	2.25
HE	1.80	2.40
A	0.80	1.10
A2	0.80	1.00
A1	0.00	0.10
e	0.65 BSC	
b	0.25	0.40
b1	0.55	0.70
c	0.10	0.18
L	0.26	0.46

Tape Dimensions and Part Orientation

Tape and reel for this material are in accordance with EIA-481-1 except where exceptions are identified.

PCB Footprint



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Preferred Assembly Instructions

This package is compatible with both lead free and leaded solder reflow processes as defined within IPC/JEDEC J-STD-020C. The maximum package temperature should not exceed 260 °C.

Handling Precautions

To avoid damage to the devices, care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. storage, handling, assembly, and testing.

ESD Rating

These devices should be treated as Class 0 (0V to 250V) using the human body model as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

MSL Rating

The device has an MSL rating of Level 1. To determine this rating, preconditioning was performed to the device per the Pb-free solder profile defined within IPC/JEDEC J-STD-020C, moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices.

Application Notes and Design Data

Application Notes and design data including S-parameters, noise parameters, and device model are available on request and from www.rfmd.com.

Reliability

An MTTF of 4.2 million hours at a channel temperature of 150 °C is achieved for the process used to manufacture this device.

Disclaimers

This product is not designed for use in any space-based or life-sustaining/supporting equipment.

Ordering Information

Description	Ordering Code
Lead-Free Packaged pHEMT	FPD750SOT343E
RoHS-Compliant Packaged pHEMT with enhanced passivation (recommended for new designs)	EB750SOT343CE
2.0GHz Evaluation Board	EB750SOT343CE-BC

Quantity	Ordering Code
Reel of 1000	FPD750SOT343E
Reel of 100	FPD750SOT343ESR
Bag of 25	FPD750SOT343ESQ
Bag of 5	FPD750SOT343ESB

Note: To order RoHS-compliant packaged pHEMT with enhanced passivation parts, replace the E suffix with CE.