LG Semicon Co.,Ltd.

GM0810

VOICE BAND CODEC

Description

The GM0810 contains A/D and D/A conversion functions integrated on a single chip. The GM0810 is an ideal analog front end device for high performance fax and data modems as well as low cost digital audio applications.

The GM0810 includes 16-bit Sigma Delta A/D converter. Simple digital decimation filters with frequency response equalization are provided for A/D converter.

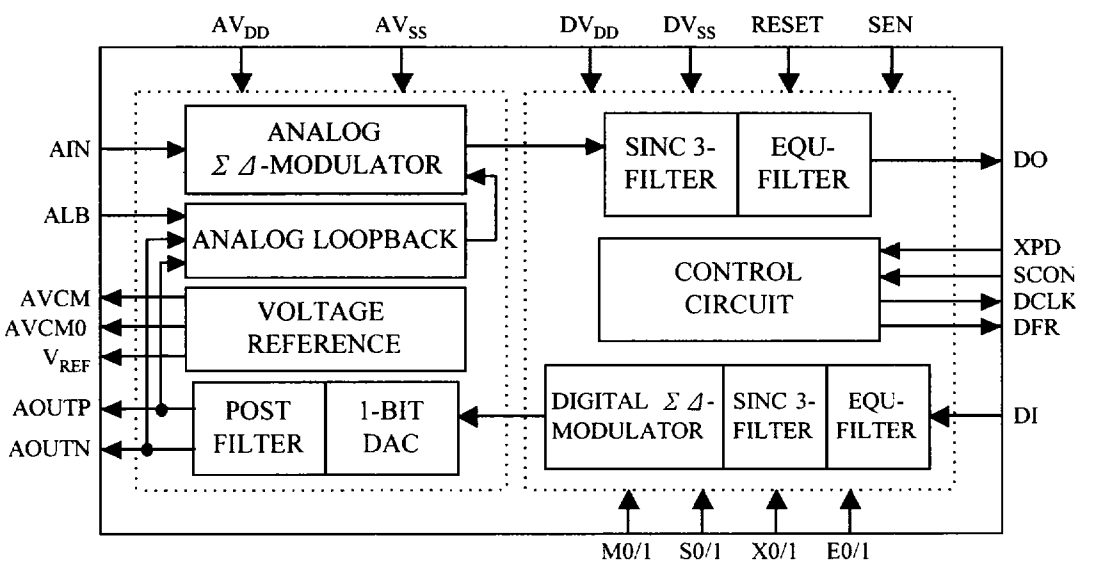
An interpolation filter together with equalization and analog post filtering are provided for D/A converter. On-chip voltage reference ensures a highly integrated solution.

Serial DSP interfaces for transmit and receive paths support directly industry standard DSP processors. The GM0810 supports versatile sampling frequencies including V.34 and V.34bis.

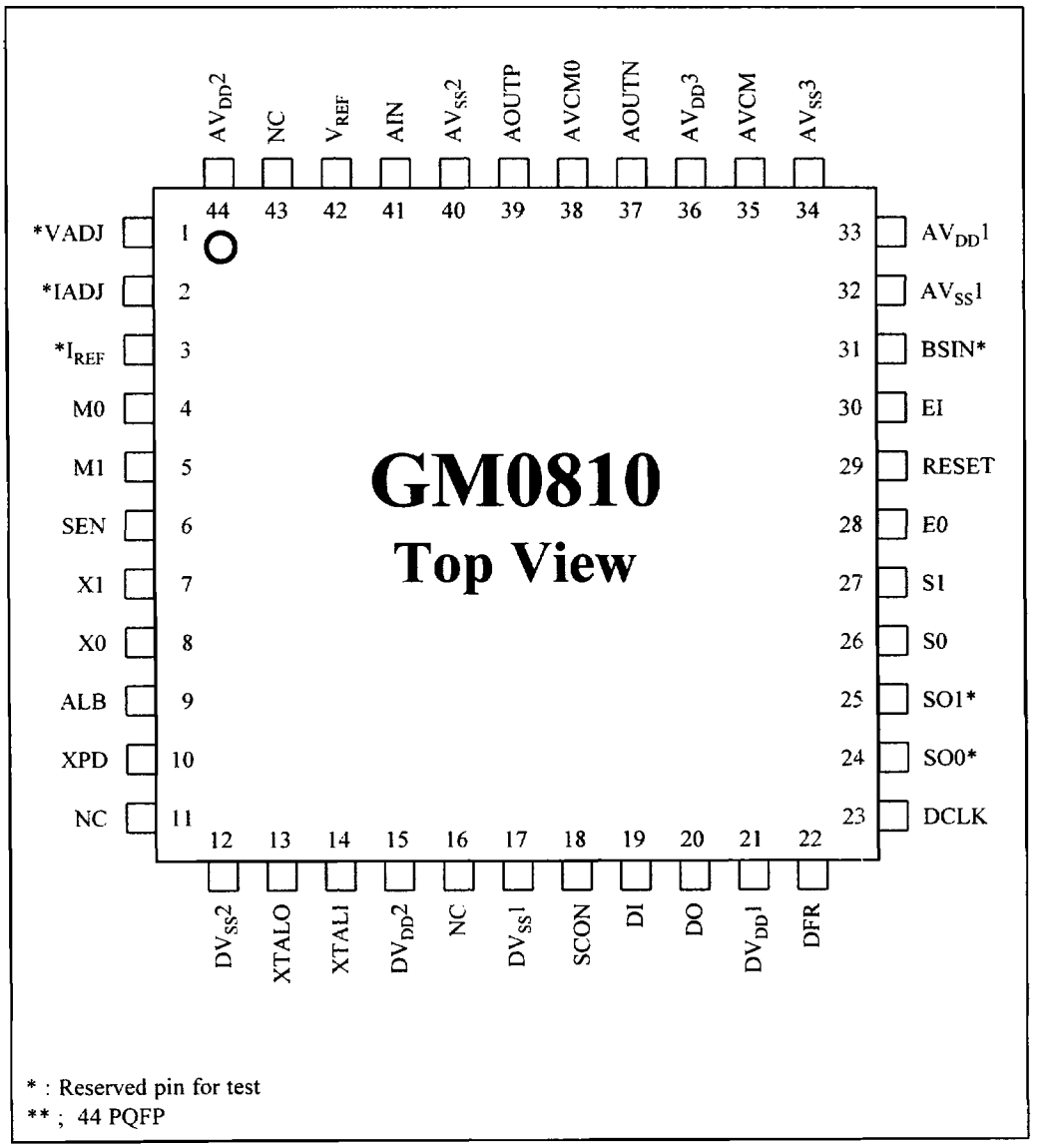
Features

- Low cost single chip A/D and D/A converter
- Supports for V.34 and V.34bis
- 2x and 4x oversampled data available
- Over 80dB dynamic range
- Single +5V power supply
- On-chip voltage reference
- Flexible serial DSP interface
- Available in 44 QFP or library module

Block Diagram



Pin Configuration



* : Reserved pin for test
** ; 44 PQFP

Pin Description

ANALOG SIGNALS

SYMBOL	PIN	I/O	DESCRIPTION
AVCM	35	O	Buffered anlaog ground (2.5V)
AVCM0	38	O	Unbeffered analog ground
AIN	41	I	Single end analog input
AOUTN	37	O	Negative analog output
AOUTP	39	O	Positive analog output
V_{REF}	42	O	Voltage reference (1.2116V at 50 ° C)
AV_{DD}	33,36,44	P	Analog power (+5V)
AV_{SS}	32,34,40	P	Analog ground

DIGITAL SIGNALS

SYMBOL	PIN	I/O	DESCRIPTION
DCLK	23	O	Serial data clock (864 kHz)
DFR	22	O	Serial data frame
DI	19	I	Serial data input
DO	20	O	Serial data output
EI	30	I	Mode select for D/A equalization (1=OFF, 0=ON)
EO	28	I	Mode select for D/A equalization (1=OFF, 0=ON)
XTAL1	14	I	Crystal input
XTAL0	13	I	Crystal output (13.824MHz)
RESET	29	I	Master reset (active low)

DIGITAL SIGNALS

SYMBOL	PIN	I/O	DESCRIPTION
M0, M1	4,5	I	Mode select (interface)
S0, S1	26,27	I	Mode select (sampling rate)
X0, X1	8,7	I	Mode select (oversampling ratio)
DV_{DD}	15,21		Digital power (+5V)
DV_{SS}	12,17		Digital ground
XPD	10	I	Power down (active low)
ALB	9	I	Analog loopback (active high)
SEN	6	I	Serial control enable (active high)
SCON	18	I	Serial control input
NC	18		No connection

External control pins are EI, EO, M0, M1, S0, S1, X0, X1, XPD and ALB.

Functional Description

The GM0810 utilizes the Sigma Delta modulation technique to achieve high resolution converters.
In the analog modulator a different signal between input signal and either $+V_{REF}$ or $-V_{REF}$ is integrated. The selection of either $+V_{REF}$ or $-V_{REF}$ for the different calculation is determined for every oversampling cycle by the output of the modulator at the same instant.
The output from the second integrator is quantized to single bit value, +1 or -1 that represents actually the polarity of the output. This one bit data is used to control the selection of feedback value, $+V_{REF}$ or $-V_{REF}$. In this way a negative feedback loop established around the integrators. The quantized one bit data is output from the modulator to the decimation filter.

In the digital modulator the operation is similar in nature containing also integrators accumulating different signals. The arithmetic operations are performed by digital devices and the signals are represented by digital codes instead of analog voltages.

In both cases second order modulator provide a transfer function that passes the signal band but shapes quantization noise energy then removed by digital decimation filter (A/D) or analog low pass filter (D/A).

OPERATING MODES

The GM0810 operates from external master clock which is 13.824 MHz. Sample rates from 7.2 KHz via 8 KHz and 9 KHz to 9.6 KHz are readily available. Also 2x and 4x oversampled data rates are available. Other sample rates can be generated by simply changing the system clock rate. All digital and the first analog post filter is a continuous time filter with corner frequency (-3dB) of 50 KHz.

TABLE 1. Sample rate selection control (f_{ext} = *13.824 MHZ*, f_{os} = *0.864MHz*)

X1	X0	S1	S0	OSR	fs (KHz)	Remark
0	0	0	0	45	38.4	
0	0	0	1	48	36	
0	0	1	0	54	32	
0	0	1	1	60	28.8	
0	1	0	0	168	10.286	3429 Hz×3 -1
0	1	0	1	206	8.388	2796 Hz×3 (2.8KHz×3)
0	1	1	0	210	8.229	2743 Hz×3
0	1	1	1	120	14.4	
1	0	0	0	180	9.6	3.2 KHz×3
1	0	0	1	192	9	3.0 KHz×3
1	0	1	0	216	8	
1	0	1	1	240	7.2	2.4 KHz×3
1	1	x	x	Test Modes		

TABLE 2. Equalization filter selection

EI	EO	EQUALIZATION
1	x	A/D equalization OFF
0	x	A/D equalization ON
x	1	D/A equalization OFF
x	0	D/A equalization ON

DSP INTERFACE

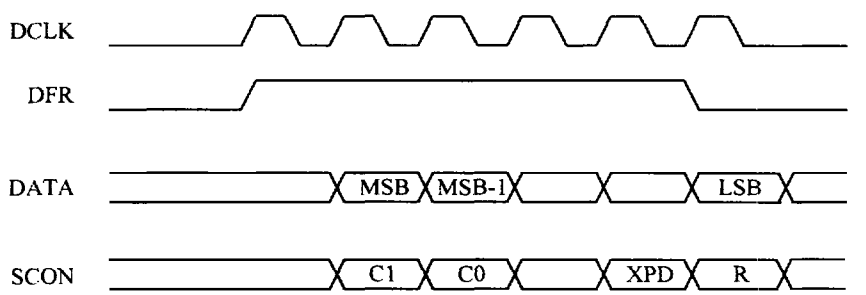
The GM0810 provides digital input and output samples in four different bus formats supporting direct connection to several popular DSP processors. Mode is selected by control pins M0 and M1.

TABLE 3. Interface selection

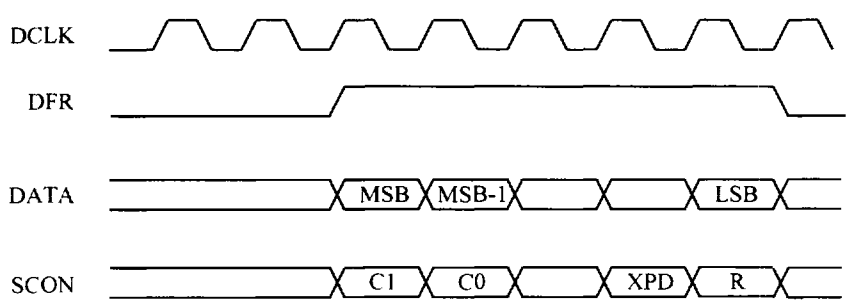
M1	M0	INTERFACE
0	0	MODE 0
0	1	MODE 1
1	0	MODE 2
1	1	MODE 3

INTERFACE TIMING

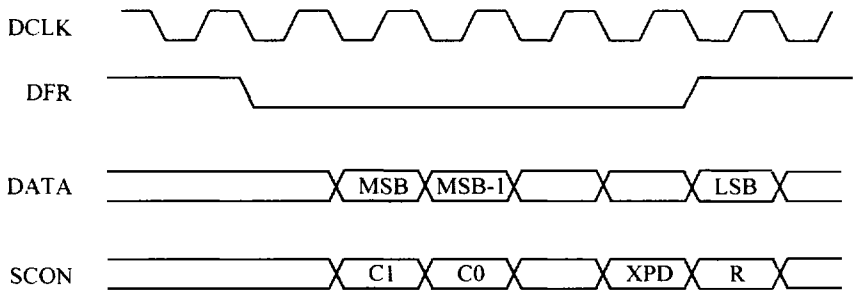
MODE 1



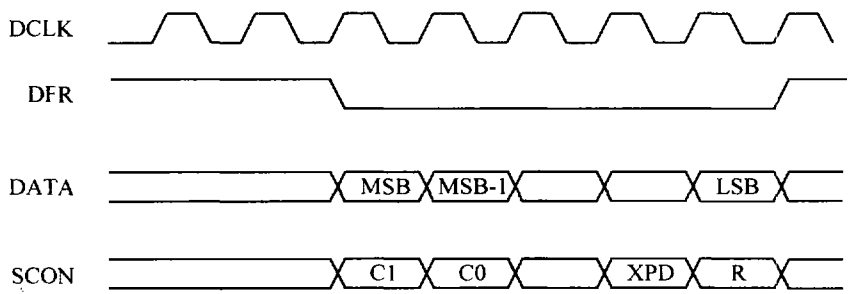
MODE 0



MODE 2



MODE 3



The GM0810 is controlled by external pin or serial control input pin. When SEN set 0, the GM0810 is controlled only by external pins. When SEN sets 1, the GM0810 is controlled only by programmed serial control as TABLE 4.

Serial Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
C1	C0	R	R	R	ALB	EI	EO	M1	M0	X1	X0	S1	S0	XPD	R	
0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	Reset Value

TABLE 4. Serial Control Register

Register	Value	Description
C1 C0	1 0	Indicate Serial Control Data
	0 0	Discard
	0 1	Discard
	1 1	Discard
ALB	0	Analog Loopback Disable
	1	Analog Loopback Enable
EI EO	1 x	A/D equalization OFF
	0 x	A/D equalization ON
	x 1	D/A equalization OFF
	x 0	D/A equalization ON
M1 M0	0 0	MODE 0
	0 1	MODE 1
	1 0	MODE 2
	1 1	MODE 3
X1 X0 S1 S0		fs (KHz) at fext=13.824MHz
	0 0 0 0	38.4
	0 0 0 1	36.0
	0 0 1 0	32.0
	0 0 1 1	28.8
	0 1 0 0	10.286
	0 1 0 1	8.388
	0 1 1 0	8.229
	0 1 1 1	14.4
	1 0 0 0	9.6
	1 0 0 1	9.0
	1 0 1 0	8.0
	1 0 1 1	7.2
	1 1 x x	Test Modes
XPD	0	Powerdown Enable
	1	Powerdown Disable
R		Reserved

Electrical Characteristics

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	DV_{DD}, AV_{DD}			6.5	V
Digital Input Voltage	V_{ind}	- 0.3		DV_{DD} + 0.3	V
Analog Input Voltage	V_{ina}	- 0.3		AV_{DD} + 0.3	V
Input Current	I_{in}	- 10		10	mA
Power Dissipation				500	mW
Storage temperature	T_{sto}	- 65		150	℃

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	DV_{DD}, AV_{DD}	4.75	5.0	5.25	V
Input Voltage	V_{in}		1.4		Vpp
Operating Temperature	T_{opr}	0		70	℃

Analog Characteristics (T_{opr} = 0 ~ 70℃, DV_{DD} = AV_{DD} = 5V, fs = 9.6 KHz)

A/D Converter

PARAMETER	MIN	TYP	MAX	UNIT
Oversampling Ratio	45		240	
Resolution		16		bit
Dynamic Range	84	88		dB
S/(N+THD) - extrapolated from - 20dB input level	74	80		dB
Input Impedance (f_{in} = 1 KHz)		80		kΩ
Input Capacitance			10	pF
Input Voltage Range			1.4	Vpp
Output Sample Rate			66.7	KHz

D/A Converter

PARAMETER	MIN	TYP	MAX	UNIT
Oversampling Ratio	45		240	
Resolution		16		bit
Dynamic Range		84		dB
S/(N+THD) - extrapolated from - 20dB input level	74	80		dB
Offset Error (T_{opr} = 25℃)		TBD		mV
Group Delay (digital filter)		TBD		μs
Group Delay (converter, fout = 1KHz)		TBD		μs
Load Impedance	600			Ω
Output Range		1.4		Vpp

Digital Characteristics (T_{opr} = 0 ~ 70℃, DV_{DD} = AV_{DD} = 5V)

PARAMETER	MIN	TYP	MAX	UNIT
Low-level Input Voltage			1.0	V
High-level Input Voltage	4.0			V
Input Capacitance			10	pF
Input Leakage Current	- 10		10	μA
Low-level Input Voltage (I_{sink} = 3.2mA)			0.4	V
High-level Input Voltage (I_{source} = -0.4mA)	2.4			V

Power Supply Characteristics (T_{opr} = 0 ~ 70℃, f_s = 9.6KHz)

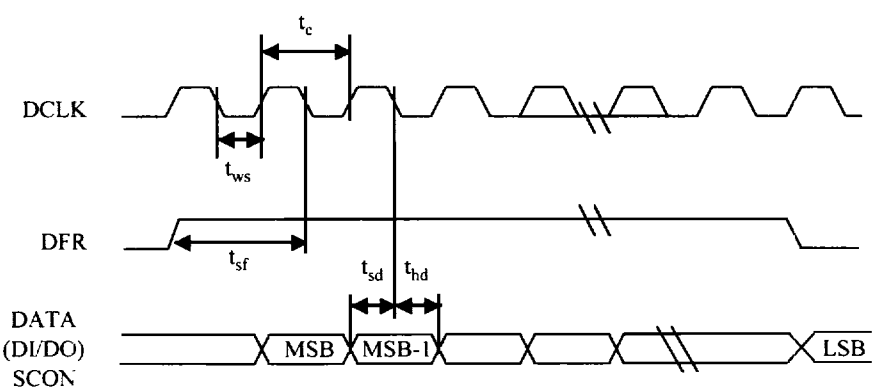
PARAMETER	MIN	TYP	MAX	UNIT
Power Dissipation		50	75	mW
Recommended Supply Voltages	4.75		5.25	V

Timing (T_{opr} = 0 ~ 70℃, DV_{DD} = AV_{DD} = 5V)

PARAMETER	MIN	TYP	MAX	UNIT
EXTCLK Frequency		13.824	24	MHz
Sampling Rate			66.7	KHz
DFR, DI Setup Time	20			ns
DFR, DI Hold Time	30			ns
DO Delay from CLK			40	ns
DFR Delay from CLK			40	ns
DFR Hold after CLK	0			ns

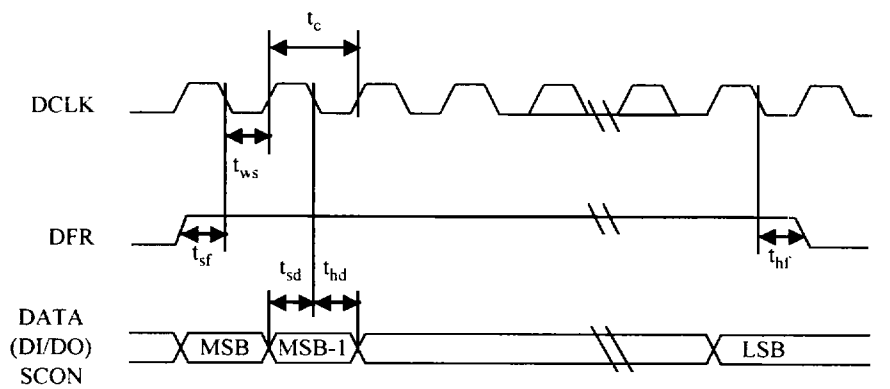
Serial Interface Timing Diagram

Serial Interface MODE 0



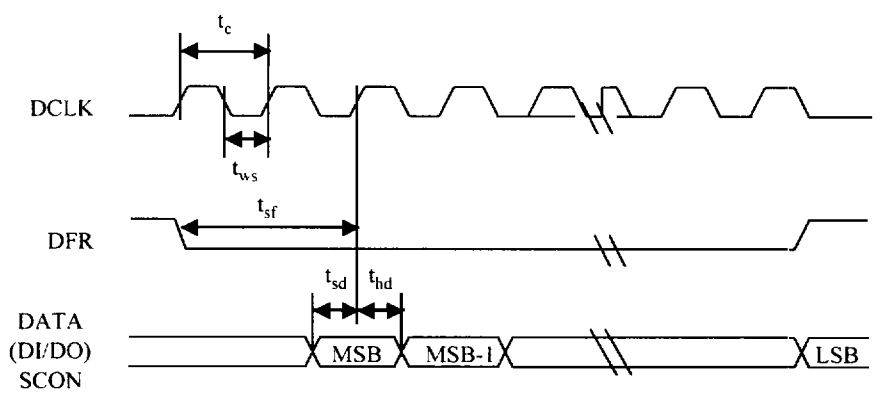
DI and DO change on the rising edge of DCLK. They should be captured on the falling edge.

Serial Interface MODE 1



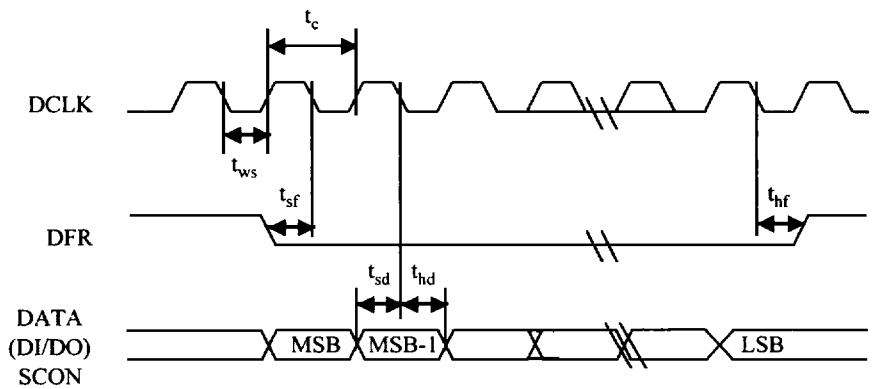
DI and DO change on the rising edge of DCLK. They should be captured on the falling edge.

Serial Interface MODE 2



DI and DO change on the falling edge of DCLK. They should be captured on the rising edge.

Serial Interface MODE 3



DI and DO change on the falling edge of DCLK. They should be captured on the rising edge.

t_{sf} : setup time for DFR before DCLK falling edge
t_{hf} : hold time for DFR after DCLK falling edge
t_{sd} : setup time for DATA before DCLK falling edge
t_{hd} : setup time for DATA after DCLK falling edge

t_{sf} , t_{hf}, t_{hd} = 250 ns min. (*EXTCLK = 13.82 MHz)
t_c = 579 ns
t_{ws} = 231 ns min.

44 PQFP Package Dimension

Unit : mm
M : MAX
m : MIN