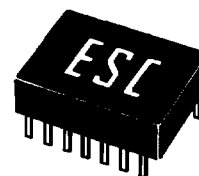
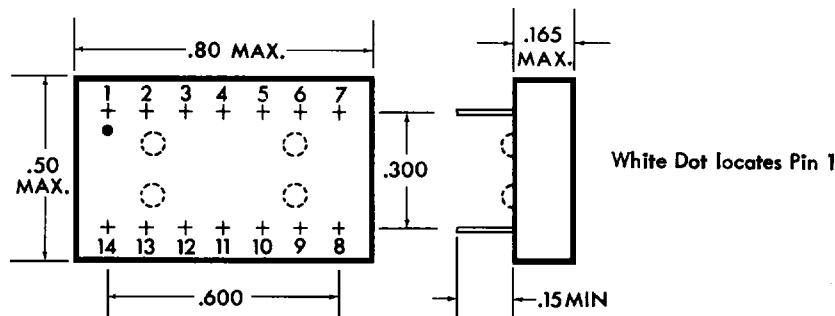




LOW PROFILE DIGITAL DELAY LINES 14 PIN PACKAGE TTL COMPATIBLE 5 TAPS • SINGLE • DUAL • TRIPLE FOR MILITARY APPLICATIONS

SERIES 9T, 9G, 9D AND 9P



ONLY ACTIVE PINS ARE SUPPLIED

Available with .015 standoffs. Add suffix S to part number when ordering.
The height of the 9P series is .200, with standoffs it is .215 max.

Intermediate delay values
available upon request.

SERIES 9T (5 TAP)		
Model No. (Fig. 1)	Delay ns	Delay/Tap ns
9T25	25	5
9T30	30	6
9T35	35	7
9T40	40	8
9T45	45	9
9T50	50	10
9T75	75	15
9T100	100	20
9T150	150	30
9T200	200	40
9T250	250	50
9T300	300	60
9T400	400	80
9T500	500	100

Delay/ Line(ns)	MODEL NUMBERS		
	Series 9G One output (Fig. 2)	Series 9D Dual output (Fig. 3)	Series 9P Triple output (Fig. 4)
5	9G5	9D5	9P5
10	9G10	9D10	9P10
15	9G15	9D15	9P15
20	9G20	9D20	9P20
25	9G25	9D25	9P25
30	9G30	9D30	9P30
35	9G35	9D35	9P35
40	9G40	9D40	9P40
45	9G45	9D45	9P45
50	9G50	9D50	9P50
60	9G60	9D60	—
75	9G75	9D75	—
100	9G100	9D100	—
125	9G125	—	—
150	9G150	—	—
200	9G200	—	—
250	9G250	—	—
300	9G300	—	—
400	9G400	—	—
500	9G500	—	—

DC PARAMETERS		LIMITS	
		Min.	Max.
V_{oh}	$V_{cc} = \min$ $I_{oh} = 1.0 \text{ mA}$	2.5V	—
V_{ol}	$V_{cc} = \min$ $I_{ol} = 20 \text{ mA}$	—	0.5V
I_{th}	$V_{cc} = \max$ $V_{ih} = 2.7V$	—	50 μA
I_{il}	$V_{cc} = \max$ $V_{il} = 0.5V$	-2.0 mA	—
I_i	$V_{cc} = \max$ $V_i = 5.5V$	—	1.0 mA
V_i	$V_{cc} = \min$ $I_{in} = -18 \text{ mADC}$	-1.2Vdc	—
I_{cc}	$V_{cc} = \max$ outputs low	Series 9T 70mA Series 9G 55mA Series 9D 100mA Series 9P 120mA	

For variations in delay from above listing, modify part number by changing delay.
Example: 125ns, 9T series becomes 9T125.

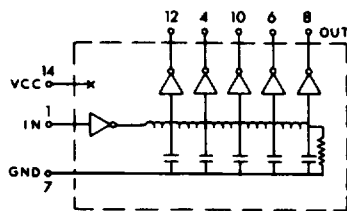


FIG. 1

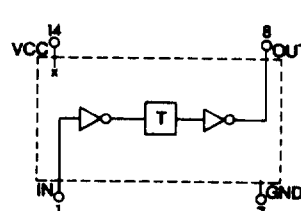


FIG. 2

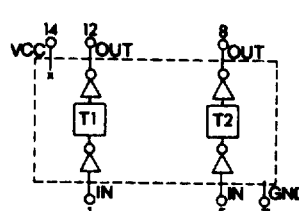


FIG. 3

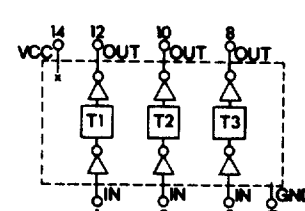


FIG. 4

SPECIFICATIONS:

- Supply voltage (V_{cc}): 5.0VDC $\pm 10\%$
- Delay tolerances: $\pm 2\text{ns}$ or $\pm 5\%$ wig
- Rise time: 4ns max
- Minimum pulse width: 40% of Total delay
- Maximum duty cycle: 50%
- Operating temp. range: -55°C to $+125^\circ\text{C}$
- Temp. coeff. of delay: 1.0ns + 500ppm/ $^\circ\text{C}$
- Terminals: Electro tin plated alloy 42
.020w x .010th.

TEST CONDITIONS:

- Temperature: $25^\circ \pm 5^\circ\text{C}$; $V_{cc}=5.0\text{VDC}$
- Input pulse width: 1.2 times the total delay time
- Pulse spacing: 5 times the total delay time
- Input rise time: 2ns; input pulse amplitude 3.0VDC
- All outputs loaded with 15pf
- Time delays measured at the 1.5 volts level on the leading edges
- Rise time measured from .75 to 2.4V

These devices are supplied with ceramic packaged IC's that have been screened to MIL-STD-883.