

KS54AHCT 192
KS74AHCT

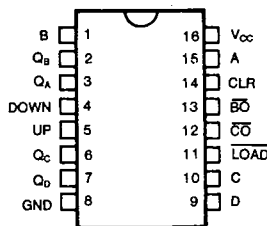
Synchronous 4-Bit Up/Down
Decade Counters with Dual Clock

T-45-23-09

FEATURES

- Look-ahead circuit enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- Function, pin-out, speed and drive compatibility with 54/74ALS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
I_{OL} = 8 mA @ V_{OL} = 0.5V
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
KS74AHCT: -40°C to +85°C
KS54AHCT: -55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	CLR	LOAD	UP	DOWN	A	B	C	D	Q _A	Q _B	Q _C	Q _D	C _O	B _O
reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	X	X	H	A	B	C	D	L	H
count up	L	H	↑	H	X	X	X	X	count up				H*	H
count down	L	H	H	↑	X	X	X		count down				H	H**

* C_O = Up at terminal count up (HHHH)
** B_O = Down at terminal count down (LLLL)
H = HIGH voltage level

L = LOW voltage level
X = don't care
↑ = LOW to HIGH clock transition

DESCRIPTION

These are high-speed synchronous reversible 4-bit decade counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidentally with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered by a low-to-high-level transition of either count (clock) input (Up or Down). The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

These counters were designed to be cascaded without the need for external circuitry. The borrow output (B_O) produces a low-level pulse while the count is zero (all outputs low) and the count-down input is low. Similarly, the carry output (C_O) produces a low-level pulse while the count is maximum (9 or 15) and the count-up input is low. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs, respectively, of the succeeding counter.

These devices provide speeds and drive capability equivalent to their ALSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

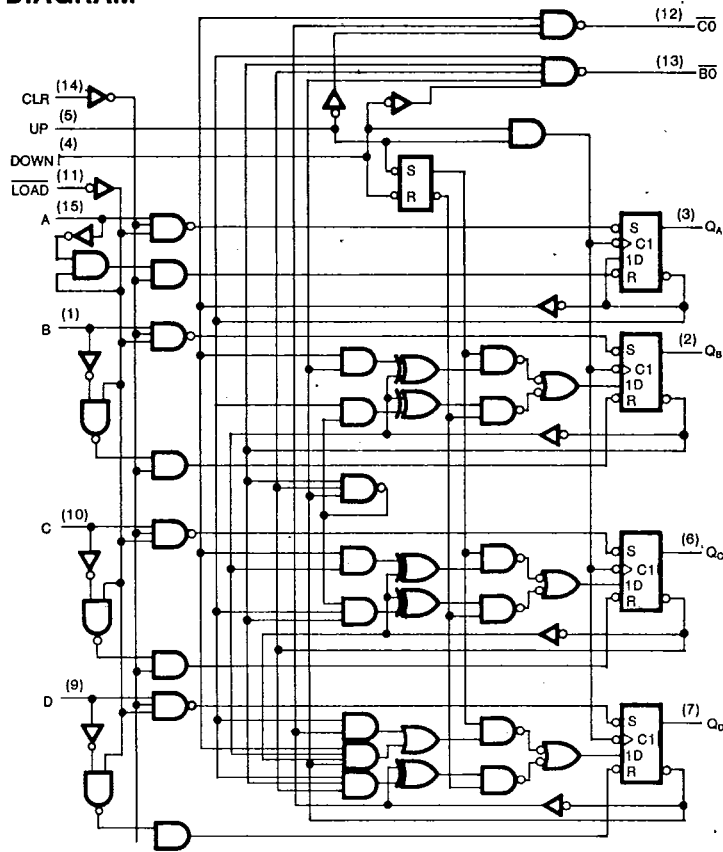
All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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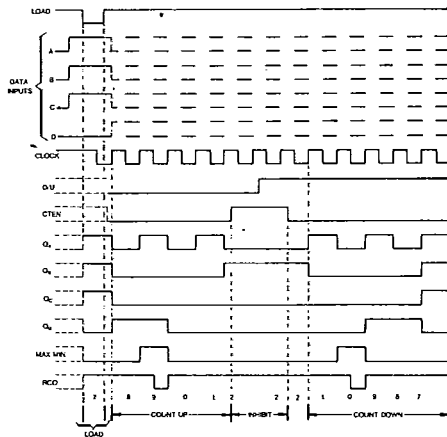
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LOGIC DIAGRAM



Typical load, count, and inhibit sequences



Sequence;

- (1) Load (preset) to BCD seven.
- (2) Count up to eight, nine (maximum) zero, one, and two.
- (3) Inhibit
- (4) Count down to one, zero (minimum), nine, eight, and seven

NOTE A: Clear overrides load data, and count inputs.
Note B: When count up, count-down input must be high; when counting down, countup input must be high.

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Absolute Maximum Ratings*

Supply Voltage Range V_{CC} , -0.5V to +7V
 DC Input Diode Current, I_{IK}
 ($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ± 20 mA
 Continuous Output Current Per Pin, I_O
 ($-0.5V < V_O < V_{CC} + 0.5V$) ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins ± 125 mA
 Storage Temperature Range, T_{stg} -85°C to $+150^\circ\text{C}$
 Power Dissipation Per Package, P_{df} 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
 Plastic Package (N): $-12\text{mW}/^\circ\text{C}$ from 85°C to 85°C
 Ceramic Package (J): $-12\text{mW}/^\circ\text{C}$ from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} ... 0V to V_{CC}
 Operating Temperature
 Range KS74AHCT: -40°C to $+85^\circ\text{C}$
 KS54AHCT: -55°C to $+125^\circ\text{C}$
 Input Rise & Fall Times, t_r , t_f Max 500 ns
 * Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$ Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	$T_a = 25^\circ\text{C}$		KS74AHCT		KS54AHCT		Unit
			Typ		Guaranteed Limits		$T_a = -55^\circ\text{C}$ to $+125^\circ\text{C}$		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	2.0	V	
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	0.8	V	
Minimum High-Level Output Voltage	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = -20\mu\text{A}$ $I_O = -4\text{mA}$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	$V_{CC} - 0.1$ 3.7	V	
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O = 20\mu\text{A}$ $I_O = 4\text{mA}$ $I_O = 8\text{mA}$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	0.1 0.4	V	
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	± 1.0	μA	
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu\text{A}$		8.0	80.0	160.0	160.0	μA	
Additional Worst Case Supply Current	ΔI_{CC}	per input in $V_I = 2.4V$ other inputs: at V_{CC} or GND $I_{OUT}=0\mu\text{A}$		2.7	2.9	3.0	3.0	mA	

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AC ELECTRICAL CHARACTERISTICS (Input t_r , $t_f \leq 2$ ns), AHCT192

Characteristic	Symbol	Conditions†	$T_a = 25^\circ\text{C}$	KS74AHCT		KS54AHCT		Unit
			$V_{CC} = 5.0\text{V}$	$T_a = -40^\circ\text{C to } +85^\circ\text{C}$	$T_a = -55^\circ\text{C to } +125^\circ\text{C}$	$V_{CC} = 5.0\text{V} \pm 10\%$		
			Typ	Min	Max	Min	Max	
Maximum Clock Frequency	f_{max}		50	30		25		MHz
Propagation Delay, UP to CO	t_{PLH}	$C_L = 50\text{pF}$	11		18		22	ns
	t_{PHL}		11		18		22	
Propagation Delay, DOWN to any Q	t_{PLH}		11		18		22	ns
	t_{PHL}		11		18		22	
Propagation Delay, UP or DOWN to any Q	t_{PLH}		11		19		23	ns
	t_{PHL}		11		19		23	
Propagation Delay, LOAD to any Q	t_{PLH}		17		29		35	ns
	t_{PHL}		17		29		35	
Propagation Delay, CLR to any Q	t_{PLH}		10		17		20	ns
Pulse Width	CLR High		t_w	6	10		15	
	LOAD Low	10		17		20		
	UP or DOWN High or Low	10		17		20		
Setup Time	Data before LOAD†	t_{su}	10	17		29		ns
	CLR Inactive before UP† or DOWN†		10	17		20		
	LOAD Inactive before UP† or DOWN†		10	17		20		
	UP high before DOWN†		10	17		17		
	Down high before UP†		8	15		15		
Hold Time	Data after LOAD†	t_h	-3	0		0		ns
	UP High after DOWN†		-3	0		0		
	DOWN High after UP†		3	8		6		
Input Capacitance	C_{IN}		5				pF	
Power Dissipation Capacitance*	C_{PD}		80				pF	

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

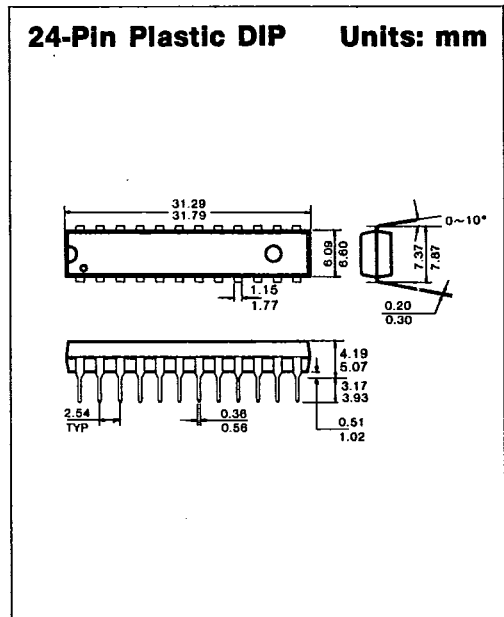
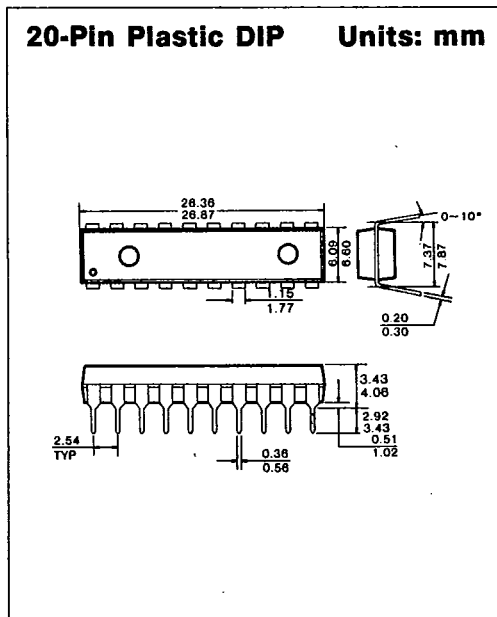
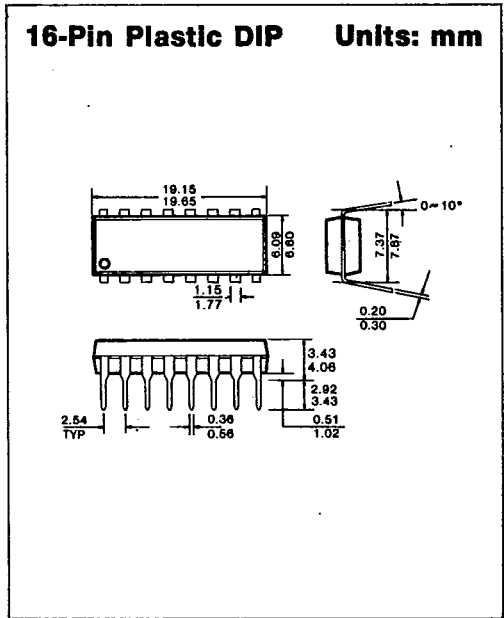
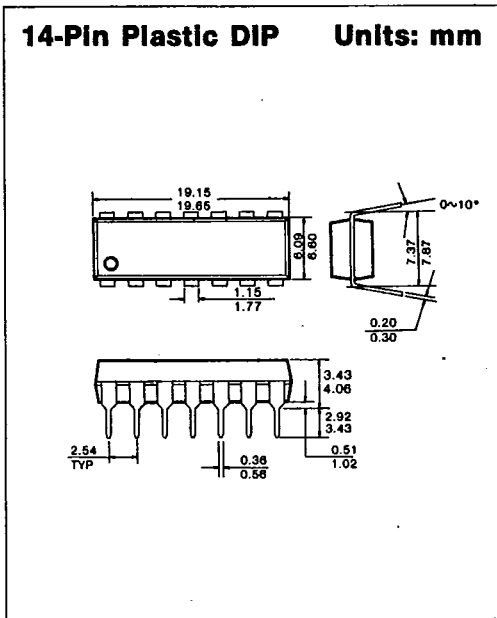
† For AC switching test circuits and timing waveforms see section 2.



PACKAGE DIMENSIONS

T-90-20

1. PLASTIC PACKAGES



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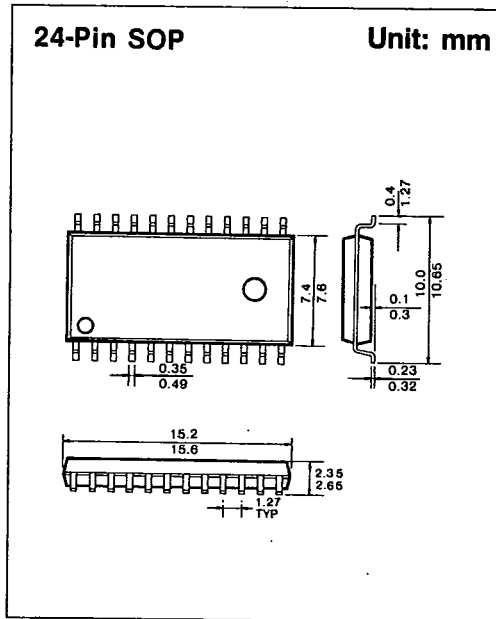
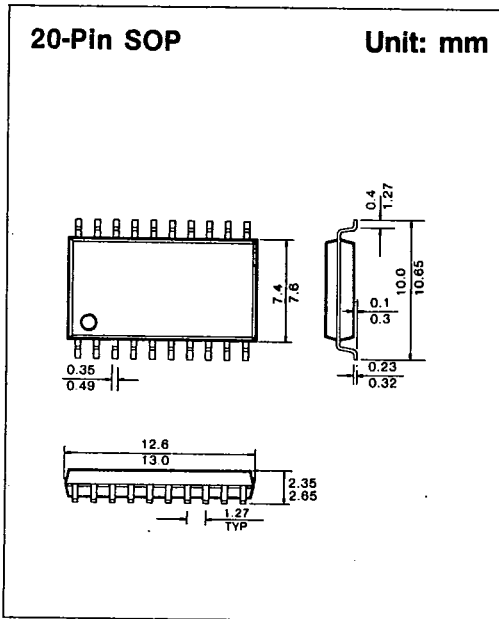
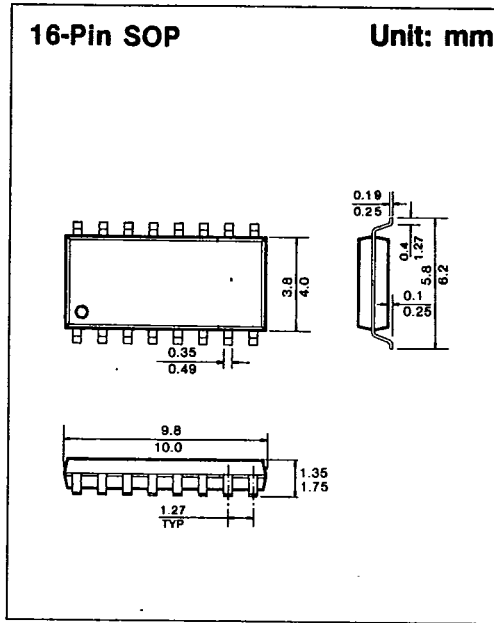
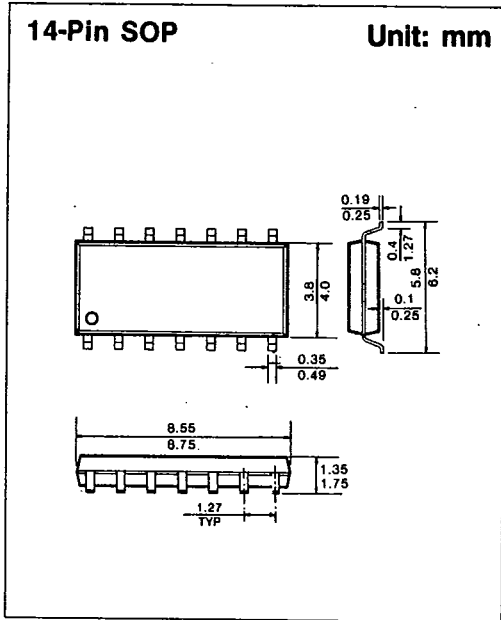
SAMSUNG SEMICONDUCTOR

1675

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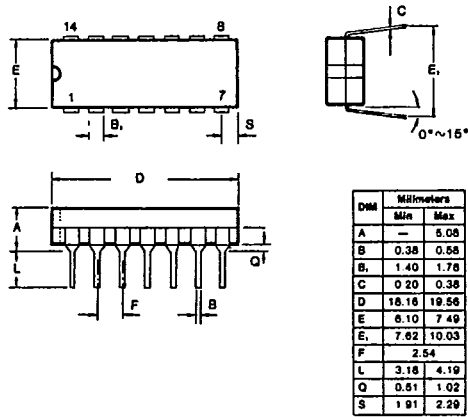


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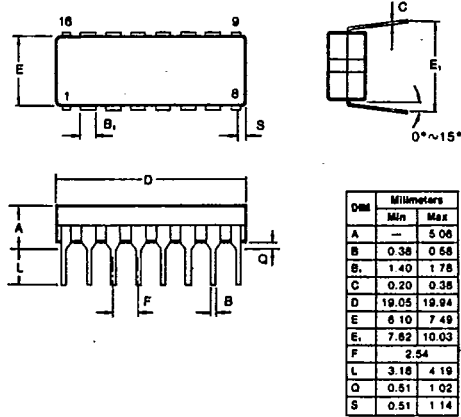
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2. CERAMIC PACKAGES

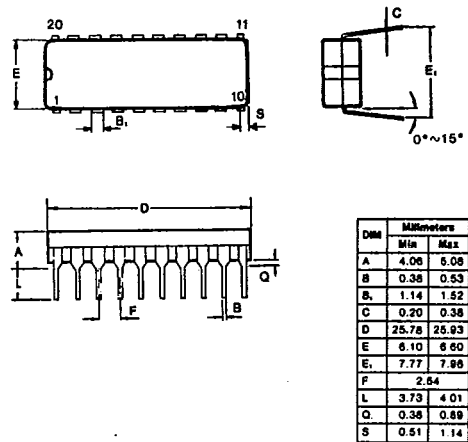
14-Pin Ceramic DIP Units: mm



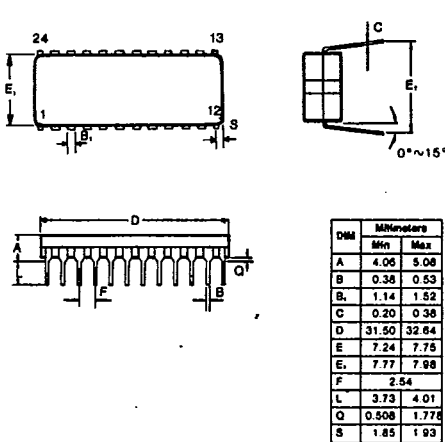
16-Pin Ceramic DIP Units: mm



20-Pin Ceramic DIP Units: mm



24-Pin Ceramic DIP Units: mm



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