Floppy Disk Write Amplifier

GENERAL DESCRIPTION

The XR-3471 is a write amplifier designed to provide the complete interface between write data signals and tunnel and straddle erase magnetic heads. Although primarily intended for floppy disk drive systems, the XR-3471 can also be used in other magnetic media systems such as tape drives. Write and erase currents are each externally resistor programmable. Also included is circuitry for inner track write current compensation.

The XR-3471, available in a 20 pin DIP or small outline package, provides TTL compatible inputs. Tunnel erase delays are determined by external reistors and capacitors.

FEATURES

Fully Programmable Write & Erase Currents
Fully Programmable Erase Turn-on/Turn-off Times
(Tunnel and Straddle Erase Compatibility)
Inhibit Output
TTL Compatible Inputs
Direct Replacement for Motorola MC3471

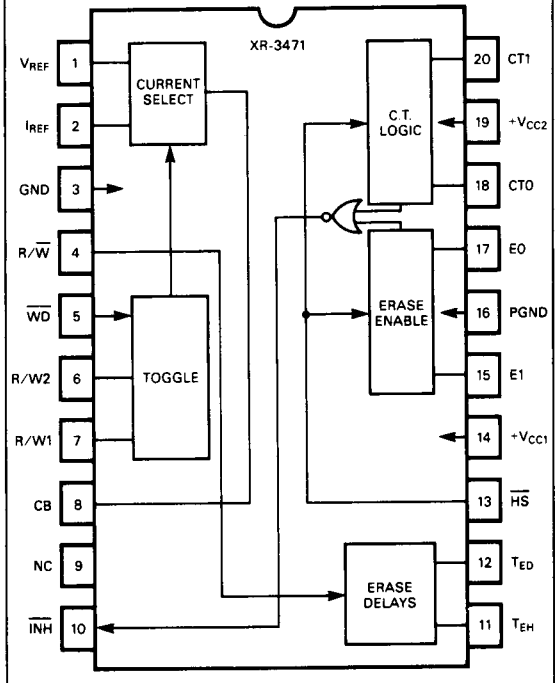
APPLICATIONS

Floppy Disk Drives
Magnetic Tape Write Amplifier

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_{CC} 2	30 V dc
V_{CC} 1	7.0 V dc
Input Voltage (All Digital Inputs)	−0.2 V to +5.75 V dc
Output Current	100 mA dc
Storage Temperature	-55°C to +150°C
Power Dissipation	
Plastic Package	650 mW
Derate Above 25°C	5.0 mW/°C
Ceramic Package	1 W
Derate Above 25°C	8.0 mW/°C

FUNCTIONAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-3471CN	Ceramic	0°C to +70°C
XR-3471CP	Plastic	0°C to +70°C
XR-3471MD	Small Outline	0°C to +70°C

SYSTEM DESCRIPTION

The XR-3471 accepts a serial binary data stream input. With the write mode selected, negative transitions of this input signal will alternately provide write current to each half of the head. The write current is externally programmed with a resistor between the internal voltage reference and the current setting input. A high-current open collector output provides the erase coil drive. Turn-on and turn-off delay circuitry is provided, with the delay externally programmed.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 10.8 to 26.4 V, unless specified otherwise. Typicals given for V_{CC1} = 5.0 V, V_{CC2} = 12 V and T_A = 25°C, unless noted otherwise.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
DIGITAL INPUT VOLTAGES							
I_{CC2} I_{CC2}	Power Supply Current			17 7.5	60 30	mA	V_{CC1} V_{CC2}
V_{IH}	High Level Input Voltage	4,8,13	2.0			V	V_{CC1} = 4.5 V
V_{IL}	Low Level Input Voltage	4,8,13			0.8	V	V_{CC1} = 5.5 V
V_{IK}	Input Clamp Voltage	4,5,8,13		−0.87	−1.5	V	I_{IK} = −12 mA
$V_{T(+)}$	Positive Threshold	5	1.5	1.75	2.0	V	V_{CC1} = 5.0 V
$V_{T(-)}$	Negative Threshold	5	0.7	0.98	1.3	V	V_{CC1} = 5.0 V
V_{HTS}	Hysteresis		0.4	0.76		V	$V_{T(+)} - V_{T(-)}$
DIGITAL INPUT CURRENTS							
I_{IH}	High Level Input Current	4,5,8,13		0.1	40	μA	V_{CC1} = 5.5 V, V_{CC2} = 26.4 V, V_I = 2.4 V
I_{IL}	Low Level Input Current	4,5,8,13 4 4 5 8,13		 0.36 0.76 0.46 0.39	−1.6	mA	V_{CC1} = 5.5 V, V_{CC2} = 26.4 V V_{CC2} = 12 V V_{CC2} = 24 V V_{CC1} = 5.0 V V_{CC1} = 5.0 V
DIGITAL OUTPUT LEVEL ($\overline{\text{INHIBIT}}$)							
I_{OH}	High Level Output Current	10			100	μA	V_{OH} = 7.0 V, V_{CC1} = 4.5 V
V_{OL}	Low Level Output Voltage	10			0.5	V	I_{OL} = 4.0 mA, V_{CC1} = 4.5 V
CENTER-TAP and ERASE OUTPUTS							
V_{OH}	Output High Voltage	18,20	V_{CC2} −1.5 V	V_{CC2} −1.0		V	I_{OH} = −100 mA V_{CC1} = 4.5 V_{CC2} = 10.8 to 26.4 V
V_{OL}	Output Low Voltage	18,20		 70 70	 150 150	mV	I_{OL} = 1.0 mA V_{CC2} = 12 V V_{CC2} = 24 V
I_{OH}	Output High Leakage	15,17		0.01	100	μA	V_{OH} = 24 V, V_{CC1} = 4.5 V, V_{CC2} = 24 V
V_{OL}	Output Low Voltage			 0.27 0.27	 0.60 0.60	 V V	I_{OL} = 90 mA, V_{CC1} = 4.5 V V_{CC2} = 12 V V_{CC2} = 24 V

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC1} = 4.5 to 5.5 V, V_{CC2} = 10.8 to 26.4 V, unless specified otherwise. Typicals given for V_{CC1} = 5.0 V, V_{CC2} = 12 V and T_A = 25°C, unless noted otherwise.

SYMBOL	PARAMETERS	PINS	MIN	TYP	MAX	UNIT	CONDITIONS
CURRENT SOURCE							
V_{REF}	Reference Voltage	1		5.7		V	
V_{DEG}	Degauss Voltage	1		1.0		V	Voltage Pin 1—Voltage Pin 2
V_F	Bias Voltage	2		0.7		V	
I_{OH}	Write Current Off Leakage	6,7		0.03	15	µA	V_{OH} = 30 V
V_{SAT}	Saturation Voltage	6,7		0.85	2.7	V	V_{CC2} = 12 V
ΔI_{RW}	Current Sink Compliance	6,7		15	40	µA	$V_{6,7}$ = 4.0 V to 24 V
I_{RA}	Average Value Write Current	6,7					Note 2
			2.91	3.0	3.09	mA	R_W = 10k, CB = Low
			5.64	5.89	6.14	mA	R_W = 5.0k, CB = Low
CB	Current Boost		31.3	33.3	35.5	%	R_W = 10k, CB = High
ΔI_{RW}	Difference in Write Current $I_{R/W2} - I_{R/W1}$	6,7					
				0.003	0.015	mA	R = 10k, IWRS = Low
				0.005	0.030	mA	R = 5.0k, IWRS = Low

Note 2 $I_{AVG} = \frac{I_{R/W1} + I_{R/W2}}{2}$

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AC SWITCHING CHARACTERISTICS

Test Conditions: V_{CC1} = 5.0 V, T_A = 25°C, V_{CC2} = 24 V, I_{RWS} = 0.4 and $I_{R/W}$ = 3.0 mA, unless specified otherwise (refer to Figure 1).

PARAMETERS	F_{IN} Note 4	MIN	TYP	MAX	UNIT
1. Delay from Head Select going through 0.8 V to CT0 going high through 20 V.	HS, Pin 13		1.6	4.0	µs
2. Delay from Head Select going low through 0.8 V to CT1 going low through 1.0 V.	HS		2.1	4.0	µs
3. Delay from Head Select going high through 2.4 V to CT0 going low through 1.0 V.	HS		1.7	4.0	µs
4. Delay from Head Select going high through 2.4 V to CT1 going high through 20 V.	HS		1.4	4.0	µs
5. Delay from R/W going low through 0.8 V to CT0 going low through 1.0 V.	R/W, Pin 4		1.3	4.0	µs
6. Delay from R/W going low through 0.8 V to CT1 going high through 20 V.	R/W, Pin 4		0.8	4.0	µs
7. Delay from R/W going low through 0.8 V to CT0 going high through 20 V.	R/W, Pin 4		0.75	4.0	µs
8. Delay from R/W going low through 0.8 V to CT1 going low through 1.0 V.	R/W, Pin 4		1.2	4.0	µs
9. After R/W goes high, delay from R/W1 turning off through 10% to CT0 going high through 20 V.	R/W, Pin 4	20	750		ns
10. After R/W goes high, delay from R/W1 turning off through 10% to CT1 going low through 1.0 V.	R/W, Pin 4	20	1200		ns
11. After R/W goes high, delay from R/W2 turning off through 10% to CT0 going low through 2.0 V.	R/W, Pin 4	20	1200		ns
12. After R/W goes high, delay from R/W2 turning off through 10% to CT1 going high through 20 V.	R/W, Pin 4	20	600		ns
13. After R/W goes low, delay from CT0 going low through 1.0 V to R/W1 turning on through 10%.	R/W, Pin 4	20	750		ns
14. After R/W goes low, delay from CT1 going low through 1.0 V to R/W2 turning on through 10%.	R/W, Pin 4	20	750		ns
15. After R/W goes low, fall time (10-90%) of R/W1.	R/W, Pin 4		5.0	200	ns
16. After R/W goes low, fall time (10-90%) of R/W2	R/W, Pin 4		5.0	200	ns
17 Set-up time, HS going low before R/W going low.	R/W, Pin 4	4.0			µs
18. Write Data low Hold Time.	WD, Pin 5	200			ns
19. Write Data high Hold Time.	WD, Pin 5	500			ns
20. Delay from R/W going high through 2.0 V to R/W1 turning off through 10% of on value.	R/W, Pin 4		3.9		µs
21. Delay from R/W going low through 0.8 V to inhibit going low 0.5 V (Note 5).	R/W, Pin 4		0.08	4.0	µs
22. After R/W goes high, delay from R/W1 turning off through 10% to inhibit going high, through 1.5 V (10k pull-up on inhibit) (Note 5)	R/W, Pin 4	20	750		ns
23. After R/W goes high, delay from E1 going high through 23 V to inhibit going through 1.5 V (10k pull-up on inhibit) (Note 5).	R/W, Pin 4	20	750		ns

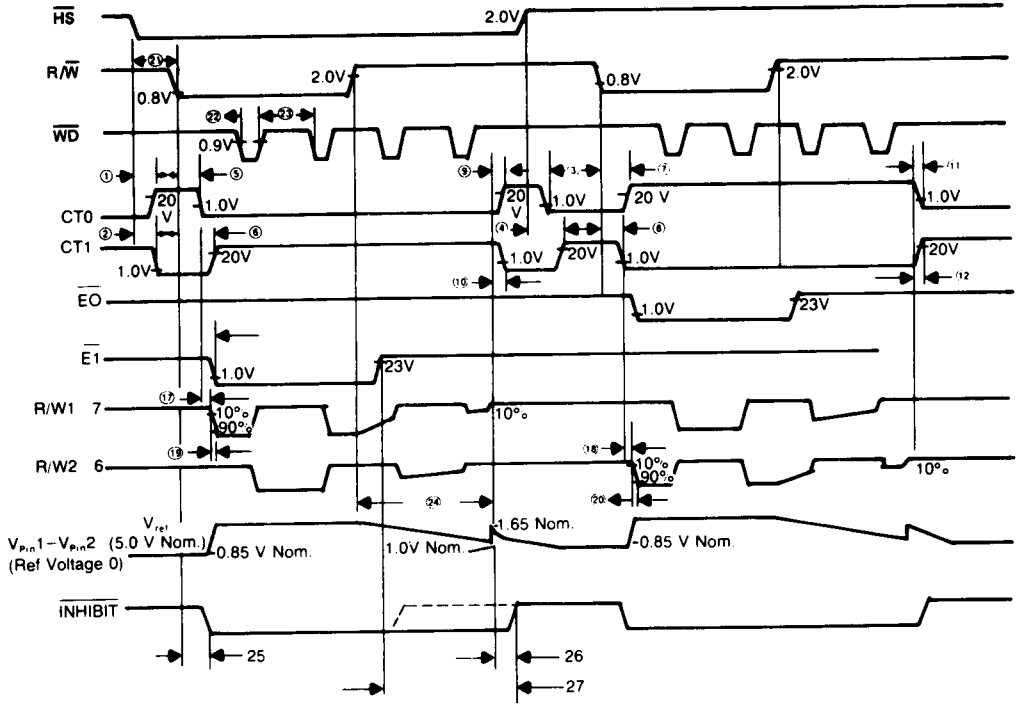

Figure 1. AC Timing Diagram

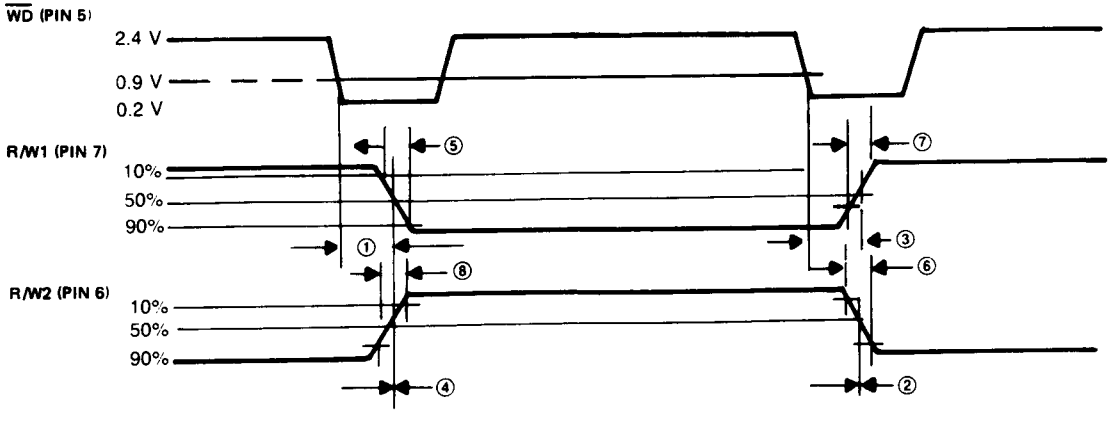

Figure 2. R/W1 and R/W2 Relationship

AC CHARACTERISTICS Continued

Test Conditions: V_{CC1} = 5.0 V, T_A = 25°C, V_{CC2} = 24 V, R/W = 0.4 V, unless specified otherwise (refer to Figure 2).

	PARAMETERS (Note 6)	MIN	TYP	MAX	UNIT
1.	Delay from Write Data going low through 0.9 V to R/W1 turning on through 50%.		85		ns
2.	Delay skew difference of R/W1 turning off and R/W2 turning on through 50% after Write Data going low through 0.9 V.	−40	1.0	40	ns
3.	Delay from Write Data going low through 0.9 V to R/W1 turning off through 50%.		80		ns
4.	Delay skew, difference of R/W1 turning on and R/W2 turning off 50% after WD going low through 0.9 V.	−40	1.0	40	ns
5.	Rise time, 10 to 90% of R/W1.		1.7	200	ns
6.	Rise time, 10 to 90% of R/W2		1.7	200	ns
7.	Fall time, 90 to 10% of R/W1		12	200	ns
8.	Fall Time, 90 to 10% of R/W2.		12	200	ns

Note 3 Test numbers refer to encircled number in Figure 1.

Note 4 AC test waveforms applied to the designated pins as follows:

Pin	f_{in}	Amplitude	Duty Cycle
HS, Pin 13	50 kHz	0.4 to 2.4 V	50%
R/W, Pin 4	50 kHz	0.4 to 2.4 V	50%
WD, Pin 5	1.0 MHz	0.2 to 2.4 V	50%

Note 5 26 or 27, whichever produces the longer delay, will control inhibit.

Note 6 Test numbers refer to encircled numbers in Figure 2. f_{in} = 1.0 MHz, 50% Duty Cycle and Amplitude of 0.2 V to 2.4 V.

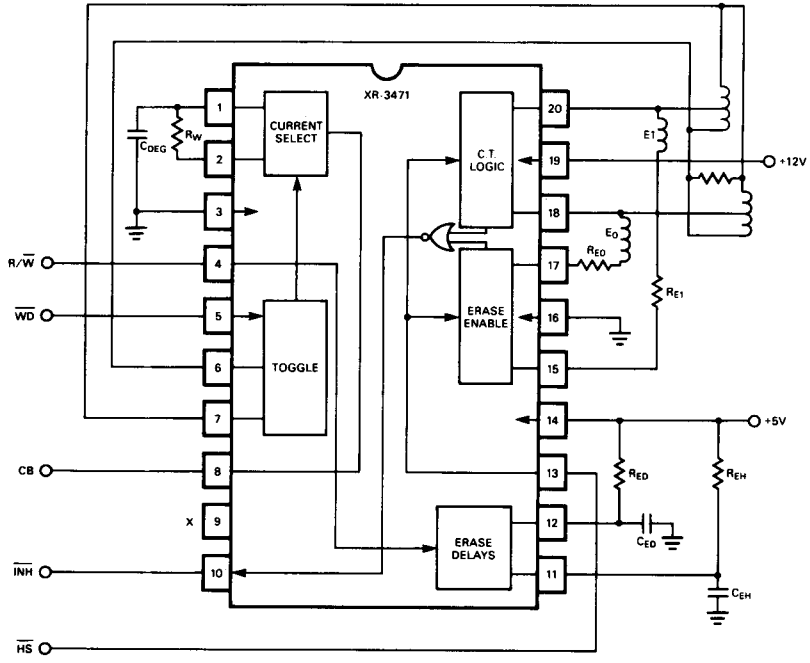

Figure 3. XR-3471 Typical Application Schematic

PIN DESCRIPTION TABLE

NAME	SYMBOL	PIN	DESCRIPTION
Head Select	HS	13	Head Select input selects between head I/O pins center-tap, erase, and read write. A HIGH selects Head 0 and a LOW selects Head 1.
Read/Write Select	R/W	4	This input selects the write mode when LOW, the read mode when HIGH.
Write Data	W/D	5	Write Data input controls the turn on/off of the write current. The internal divide-by-two flip-flop toggles on the negative going edge of this input to direct the current alternately to the two halves of the head coils.
Current Boost	CB	8	Current Boost selects the amount of write current used. When LOW, the current equals the value according to the external resistor. When HIGH, the current equals the low current +33%.
V_{ref} I_{ref}	V_{ref} I_{ref}	1 2	A resistor between these pins sets the write current. A 10 k resistor produces 3 mA of write current.
Center-tap 0	CT0	18	Center-tap 0 output is connected to the center tap Head 0. It will be pulled to GND or V_{CC2} (+12 or +24) depending on mode and head selection.
Erase 0	E0	17	Erase 0 will be LOW for writing on Head 0, and floating for other conditions.
Center-tap 1	CT1	20	Center-tap 1 output is connected to the center tap of Head 1. It will be pulled to GND or V_{CC2} (+12 or +24) depending on mode and head selection.
Erase 1	E1	15	Erase 1 will be LOW for writing on Head 1, and floating for other conditions.
R/W1 R/W2	R/W1 R/W2	7 6	These pins are the differential outputs, connected directly to the magnetic heads.
	V_{CC1}	14	+5 V Power
	V_{CC2}	19	+12 V or +24 V Power
	PGND	16	Coil grounds
	GND	3	Reference and logic ground
T_{ED} ON	T_{ED}	12	Erase turn on delay control (RC or logic).
T_{EH} OFF	T_{EH}	11	Erase Hold (turn off delay) control (RC or logic).
INHIBIT	INH	10	Inhibit is an open collector output pulled low whenever the leads are in the write, degauss, or erase mode. Inhibit is used for step or read inhibit.

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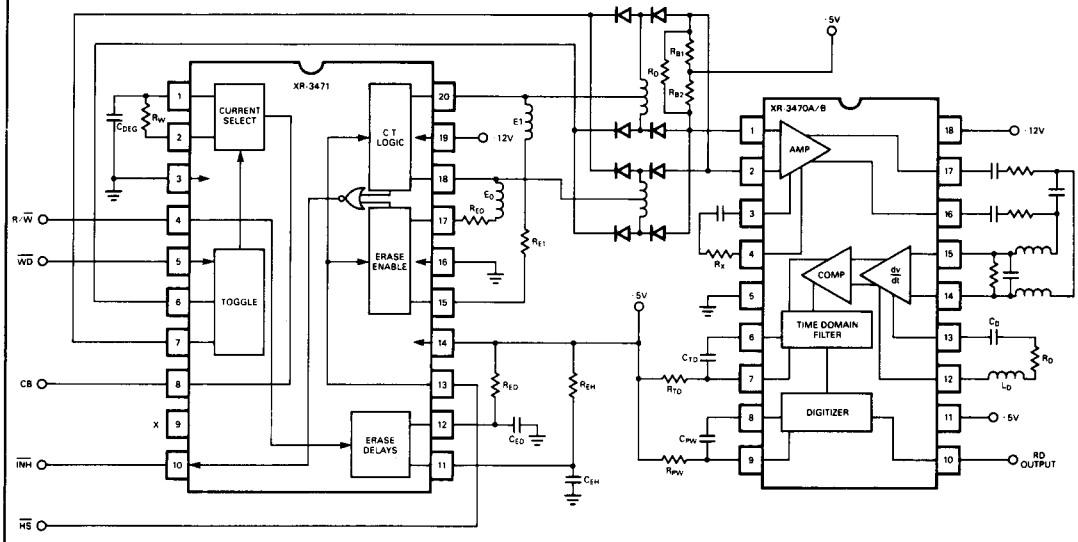


Figure 4. Dual Head Floppy Drive Using the XR-3470 and XR-3471

TYPICAL APPLICATIONS

The XR-3471 is designed for use with the XR-3470 Read Amplifier. A complete dual head floppy disk signal processing chain includes the XR-3470, XR-3471, and a head selection switching matrix. Figure 3 shows the XR-3471 in a typical application. Figure 4 shows the XR-3470 and the XR-3471 in a complete floppy drive.

Component Selection

Write current is set by R_W. Figure 5 shows the relationship between I_W and R_W.

Erase current is limited by external resistors, R_{E0} and R_{E1}.

$$I_E \approx \frac{V_{CC2} - 1.5\ V}{R_E}$$

Tunnel erase delay times are determined by external resistors and capacitors. Erase delay, the time between the write mode is selected and erase current flows equals

$$T_{ED} = R_{ED}\, C_{ED}$$

Erase Hold, the time between the end of writing and cessation of erasure is found as

$$T_{EH} = R_{EH}\, C_{EH}$$

In Figure 4, the head selection is performed by standard switching diodes. C_{DEG} controls degaussing times and may be omitted in systems not requiring degaussing. The reader is directed to the XR-3470 data sheet for a discussion of read circuit component selection.

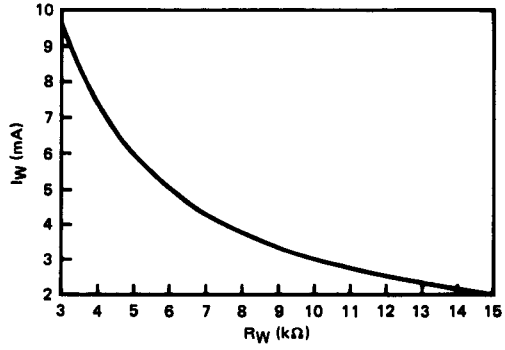


Figure 5. Write Current Dependence on R_W

EXAR

XR-1488/1489A

Quad Line Driver/Receiver

GENERAL DESCRIPTION

The XR-1488 is a monolithic quad line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard No. RS232C. This extremely versatile integrated circuit can be used to perform a wide range of applications. Features such as output current limiting, independent positive and negative power supply driving elements, and compatibility with all DTL and TTL logic families greatly enhance the versatility of the circuit.

The XR-1489A is a monolithic quad line receiver designed to interface data terminal equipment with data communications equipment. the XR-1489A quad receiver along with its companion circuit, the XR-1488 quad driver, provide a complete interface system between DTL or TTL logic levels and the RS232C defined voltage and impedance levels.

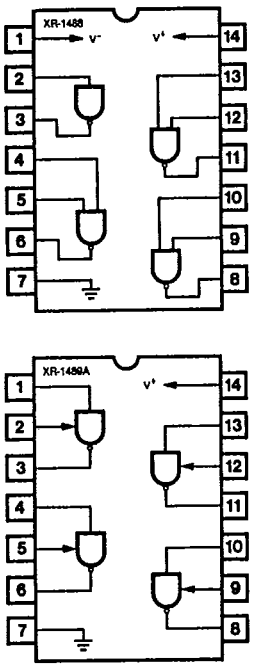
ABSOLUTE MAXIMUM RATINGS

Power Supply	
XR-1488	±15 Vdc
XR-1489A	+10 Vdc
Power Dissipation	
Ceramic Package	1000 mW
Derate above +25°C	6.7 mW/°C
Plastic Package	650 mW/°C
Derate above +25°C	5 mW/°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-1488N	Ceramic	0°C to +70°C
XR-1488P	Plastic	0°C to +70°C
XR-1489AN	Ceramic	0°C to +70°C
XR-1489AP	Plastic	0°C to +70°C

FUNCTIONAL BLOCK DIAGRAMS



SYSTEM DESCRIPTION

The XR-1488 and XR-1489A are a matched set of quad line drivers and line receivers designed for interfacing between TTL/DTL and RS232C data communication lines.

The XR-1488 contains four independent split supply line drivers, each with a ±10 mA current limited output. For RS232C applications, the slew rate can be reduced to the 30 V/μS limit by shunting the output to ground with a 410 pF capacitor. The XR-1489A contains four independent line receivers, designed for interfacing RS232C to TTL/DTL. Each receiver features independently programmable switching thresholds with hysteresis, and input protection to ±30 V. The output can typically source 3 mA and sink 20 mA.