HARRIS

HM-8832-8

32K x 8 Asynchronous CMOS Static RAM Module

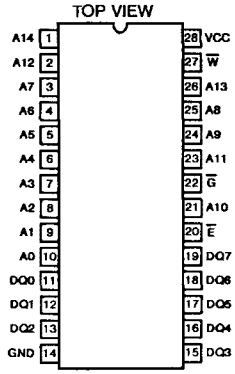
June 1989

Features

- Full CMOS Six Transistor Memory Cell
- Low Standby Supply Current 250µA
- Low Operating Supply Current 15mA
- Fast Address Access Time..... 180ns
- Low Data Retention Supply Voltage 2.0V
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Times
- No Clocks or Strobes Required
- Single 5V Power Supply
- Easy Microprocessor Interfacing
- Operating Temperature Range ... -55°C to +125°C
- Standard DIP Size - 0.6" x 1.4"

Pinout

TOP VIEW

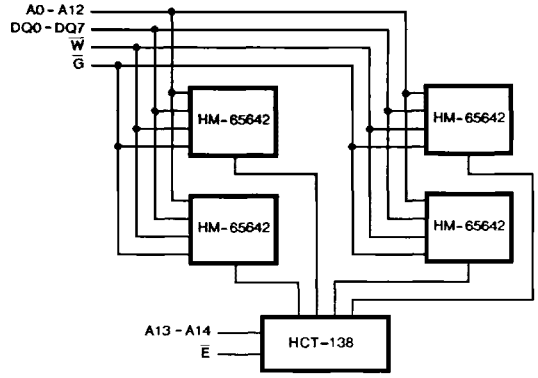


Description

The HM-8832-8 is a 32K x 8 Bit Asynchronous CMOS Static RAM Module based on a multi-layered, co-fired, dual-in-line ceramic substrate, four HM-65642 CMOS Asynchronous Static RAMs, and an HCT-138 high-speed CMOS decoder, all mounted in ceramic leadless chip carriers. In addition to this, each module is equipped with a ceramic capacitor to minimize power supply noise and reduce the need for external decoupling. Furthermore, this capacitor is sealed in a ceramic leadless carrier for maximum reliability, even in extreme environments. All inputs on the HM-8832-8 are gated by the $\overline{E}$ input to simplify system design requirements to obtain the minimum standby and data retention supply current. The pinout of the HM-8832-8 conforms with the JEDEC standard for eight-bit wide, 28 pin RAMs, which allows the module to be pin compatible with future generations of high density RAMs and EPROMs.

The HM-65642 RAMs used on the HM-8832-8 module are full CMOS devices, utilizing arrays of six-transistor (6T) memory cells for the most stable and lowest possible standby and data retention supply current over the full military operating temperature range. In addition to this, the high stability of the 6T cell provides excellent protection against soft errors due to power supply noise and alpha particles. This stability also improves the radiation tolerance of the module over that of RAMs utilizing four transistor (4T) Mix-MOS memory cells.

Functional Diagram



TRUTH TABLE

MODE	$\overline{E}$	$\overline{W}$	$\overline{G}$
Standby (CMOS)	VCC	X	X
Standby (TTL)	VIH	X	X
Enabled (High Z)	VIL	VIH	VIH
Read	VIL	VIH	VIL
Write	VIL	VIL	X

PIN DESCRIPTION

PIN	FUNCTION
A0-A14	Address Inputs
DQ0-DQ7	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
VCC	Power (+5V)
GND	Ground

3 CMOS MEMORY

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3V to VCC +0.3V
Storage Temperature Range ..... -65°C to +150°C
Gate Count ..... 405,230 Gates
Junction Temperature ..... +175°C
Lead Temperature (Soldering, Ten Seconds) ..... +300°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C

D.C. Electrical Specifications (Note 4) VCC = 5V ± 10%; T_A = -55°C to +125°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSBI	Standby Supply Current (CMOS)	-	900	µA	IO = 0, $\overline{E}$ = VCC -0.3V
ICCSB	Standby Supply Current (TTL)	-	10	mA	IO = 0, $\overline{E}$ = VIH
ICCEN	Enable Supply Current	-	10	mA	IO = 0, $\overline{E}$ = VIL
ICCOP	Operating Supply Current (Note 3)	-	15	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	750	µA	VCC = 2.0V, $\overline{E}$ = VCC -0.3V
VCCDR	Data Retention Supply Voltage	2.0	-	V	$\overline{E}$ = VCC
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	VIO = VCC or GND
VIL	Input Low Voltage	0	0.8	V	
VIH	Input High Voltage	2.4	VCC	V	
VOL	Output Low Voltage	-	0.4	V	IOL = 4.0mA
VOH1	Output High Voltage	2.4	-	V	IO = -1.0mA
VOH2	Output High Voltage (Note 2)	VCC-0.4	-	V	IO = -100µA

Capacitance (Note 2)

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CA	Address Input Capacitance	40	pF	VA = VCC or GND, f = 1MHz
CDQ, CG	Data, Output Enable Capacitance	45	pF	VDQ, VG = VCC or GND, f = 1MHz
CEN	Chip Enable Capacitance	15	pF	VEN = VCC or GND, f = 1MHz
CW	Write Enable Capacitance	60	pF	VW = VCC or GND, f = 1MHz

NOTES:
1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent CL = 100pF (min) including scope and jig - for CL greater than 100pF, access time is derated by 0.15ns per pF.
2. Guaranteed but not tested.
3. Typical derating 5mA/MHz increase in ICCOP.
4. All devices tested at worst case temperature and supply voltage limits.

A. C. Electrical Specifications (Notes 1, 4) VCC = 5V ± 10%; T_A = -55°C to +125°C

PIN NO.	SYMBOL		PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE								
(1)	TAVAX	tRC	Read Cycle Time		180	-	ns	
(2)	TAVQV	tAA	Address Access Time		-	180	ns	
(3)	TELQV	tCE	Chip Enable Access Time		-	180	ns	
(4)	TGLQV	tOE	Output Enable Access Time		-	75	ns	
(5)	TELQX	tLZ	Chip Enable Output Enable Time		10	-	ns	(Note 2)
(6)	TGLQX	tOLZ	Output Enable Time		5	-	ns	(Note 2)
(7)	TAXQX	tOH	Address Output Hold Time		10	-	ns	(Note 2)
(8)	TEHQZ	tHZ	Chip Disable Output Disable Time		0	80	ns	(Note 2)
(9)	TGHQZ	tOZ	Output Disable Time		0	55	ns	(Note 2)
WRITE CYCLE								
(10)	TAVAX	tWC	Write Cycle Time		180	-	ns	
(11)	TWLWH	tWP	Write Pulse Width		95	-	ns	
(12)	TELWH	tCW	Chip Enable to End of Write	$\overline{W}$ Controlled	95	-	ns	
(13)	TELEH	tCW	Chip Enable to End of Write	$\overline{E}$ Controlled	90	-	ns	(Note 2)
(14)	TAVWL	tAS	Address Setup Time	$\overline{W}$ Controlled	30	-	ns	
(15)	TAVEL	tAS	Address Setup Time	$\overline{E}$ Controlled	30	-	ns	(Note 2)
(16)	TWHAX	tWR	Write Recovery Time	$\overline{W}$ Controlled	10	-	ns	
(17)	TEHAX	tWR	Write Recovery Time	$\overline{E}$ Controlled	40	-	ns	(Note 2)
(18)	TDVWH	tDW	Data Setup Time	$\overline{W}$ Controlled	65	-	ns	
(19)	TDVEH	tDW	Data Setup Time	$\overline{E}$ Controlled	65	-	ns	(Note 2)
(20)	TWHDX	tDH	Data Hold Time	$\overline{W}$ Controlled	10	-	ns	
(21)	TEHDX	tDH	Data Hold Time	$\overline{E}$ Controlled	40	-	ns	(Note 2)
(22)	TWLQZ	tWZ	Write Enable Output Disable Time		-	55	ns	(Note 2)
(23)	TWHQX	tOW	Write Disable Output Enable Time		5	-	ns	(Note 2)

NOTES:

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ICCEN	Enable Supply Current	-	10	mA	IO = 0, $\overline{E}$ = VIL
ICCOP	Operating Supply Current (Note 3)	-	15	mA	IO = 0, f = 1MHz, $\overline{E}$ = VIL, VI = VCC or GND
ICCDR	Data Retention Supply Current	-	200	µA	VCC = 2.0V, $\overline{E}$ = VCC -0.3V
VCCDR	Data Retention Supply Voltage	2.0	-	V	$\overline{E}$ = VCC
II	Input Leakage Current	-1.0	+1.0	µA	VI = VCC or GND
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(22)	TWLQZ	tWZ	Write Enable Output Disable Time		-	55	ns	(Note 2)
(23)	TWHQX	tOW	Write Disable Output Enable Time		5	-	ns	(Note 2)

NOTES:
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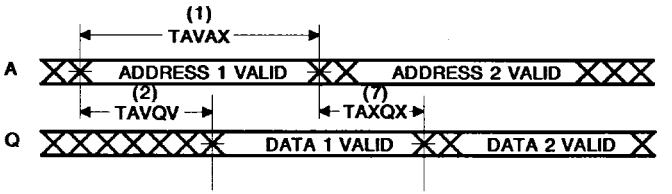
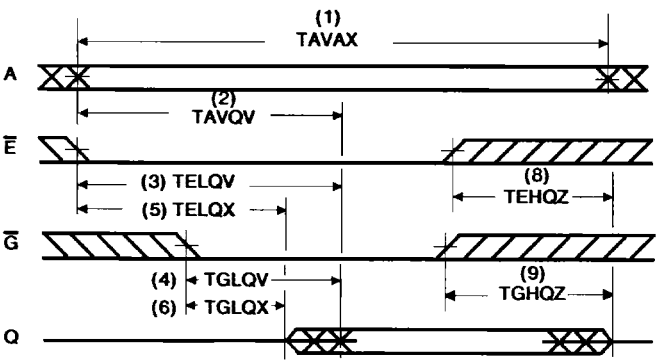
Timing Diagrams

READ CYCLE I: ADDRESS CONTROLLED (Notes 1, 2)



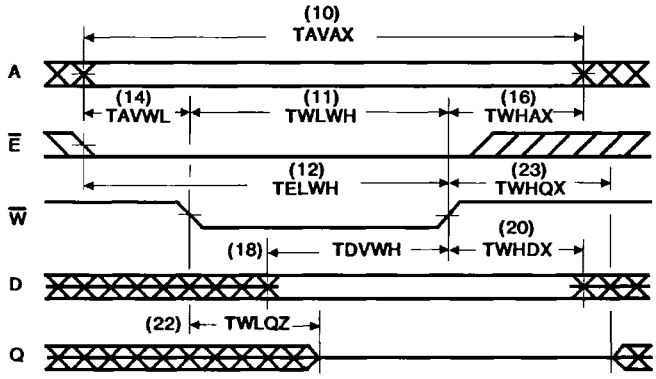
READ CYCLE II: $\overline{E}$ OR $\overline{G}$ CONTROLLED (Note 1)



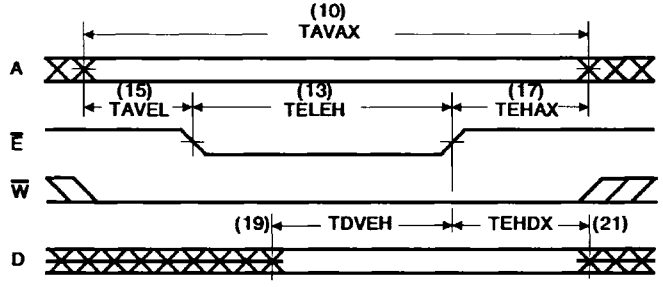
READ CYCLE NOTES:
1. In a read cycle, $\overline{W}$ is held high.
2. In read cycle 1, the module is kept continuously enabled: $\overline{E}$ and $\overline{G}$ are held low.

Timing Diagrams

WRITE CYCLE I: $\overline{W}$ CONTROLLED (Note 1)



WRITE CYCLE II: $\overline{E}$ CONTROLLED (Note 2)



WRITE CYCLE NOTES:

1. In Write Cycle I, the module is first enabled, and then data is strobed into the RAM with a pulse on $\overline{W}$. If $\overline{G}$ is held high for the entire cycle, the outputs will remain in the high impedance state. If $\overline{G}$ is held low, it may be necessary to lengthen the cycle to prevent bus contention. This would occur if TWLQZ and TDVWH overlapped.
2. In Write Cycle II, Address (A) and Write Enable ($\overline{W}$) are first set up and then data is strobed into the RAM with a pulse on $\overline{E}$.