T-46-13-27

MODULES M28C010

Timer E²

1024K Electrically Erasable PROM

October 1989

Features

- CMOS Technology
- Military Temperature Range
- Low Power Operation
  - 70 mA Active Curent
  - 2 mA Standby Current
- On-Chip Timer
  - Automatic Erase Before Write
- 64 Byte Page Mode . . . Fast Effective Write Time
  - 80 µsec Average Byte Write Time
- Write Cycle Completion Indication
  - Data Polling
- 5V ± 10% Power Supply
- Power Up/Power Down Protection Circuitry
- JEDEC Approved Byte Wide Pinout

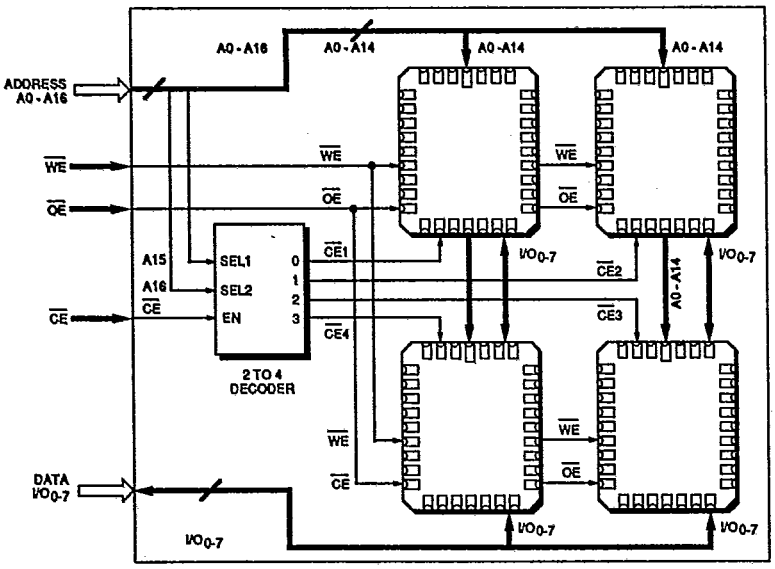
Description

SEEQ's MM28C010 is a CMOS 5V only, 128K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). The MM28C010 consists of 4 28C256 (32K x 8) CMOS EEPROMs and a 2 to 4 line decoder in LCC packages, mounted on and interconnected on a ceramic substrate. The MM28C010 is available in a 32 pin module package and is ideal for applications which require low power consumption, non-volatility and in-system reprogrammability.

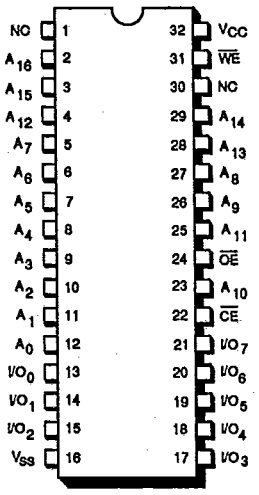
Pin Names

A_0-A_{16}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/DATA OUTPUT (READ)

Block Diagram



Pin Configuration



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The MM28C010 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches, frees the microprocessor for other tasks during the write time. The MM28C010's write cycle time is 10 ms maximum. An automatic erase is performed before a write. The Data Polling feature of the MM28C010 can be used to determine the end of a write cycle. Data retention is greater than 10 years.

Device Operation

Operational Modes

There are four operational modes (see Table 1); only TTL inputs are required. Write can only be initiated under the conditions shown. Any other conditions for $\overline{CE}$, $\overline{OE}$, and $\overline{WE}$ will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of the forementioned three input lines.

Mode Selection (Table 1)

Mode Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Standby	V_{IH}	X	X	High Z
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Write Inhibit	X	X	V_{IH}	High Z or D_{OUT}
	V_{IH}	X	X	High Z
	X	V_{IL}	X	High Z or D_{OUT}

X: any CMOS/TTL level

Reads

A read is typically accomplished by presenting the addresses of the desired byte to the address inputs. Once the address is stable, $\overline{CE}$ is brought to a TTL low in order to enable the chip. The $\overline{WE}$ pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ($\overline{OE}$) to a TTL low. During read, the addresses, $\overline{CE}$, $\overline{OE}$, and input data latches are transparent.

Writes

To write into a particular location, the addresses must be valid and a TTL low is applied to the write enable ($\overline{WE}$) pin of a selected ($\overline{CE}$ low) device. This combined with output enable ($\overline{OE}$) being high, initiates a write cycle. During a byte write cycle, all inputs except data are latched on the falling edge of $\overline{WE}$ (or $\overline{CE}$, whichever one occurred last). Write enable needs to be at a TTL low only for the specified t_{WP} time. Data is latched on the rising edge of $\overline{WE}$ (or $\overline{CE}$ whichever occurred first). An automatic erase is performed before data is written.

The MM28C010 can write both bytes and blocks of up to 64 bytes. The write mode is discussed below.

Write Cycle Control Pins

For system design simplification, the MM28C010 is designed such that either the $\overline{CE}$ or $\overline{WE}$ pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either $\overline{CE}$ or $\overline{WE}$ signal to latch the data. Address and $\overline{OE}$ set up and hold are with respect to the later of $\overline{CE}$ or $\overline{WE}$; data setup and hold is with respect to the earlier of $\overline{WE}$ or $\overline{CE}$.

To simplify the following discussion, the $\overline{WE}$ pin is used as the control pin throughout the rest of this document. Timing diagrams of both write cycles are included in the AC characteristics.

Write Mode

One to 64 bytes of data can be loaded randomly into the MM28C010. Address lines A15 and A16 must be held valid during the entire page load cycle. The part latches row addresses, A6-A14 during the first byte write. These addresses are latched on the falling edge of $\overline{WE}$ signal (assuming $\overline{WE}$ control write cycle) and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to write into different locations of the page, are latched every time a new write is initiated. These addresses along with $\overline{OE}$ state (high) are latched on the falling edge of $\overline{WE}$ signal. For proper write initiation and latching, the $\overline{WE}$ pin has to stay low for a minimum of t_{WP} ns. Data is latched on the rising edge of $\overline{WE}$, allowing easy microprocessor interface.

Upon a low to high $\overline{WE}$ transition, the MM28C010 latches data and starts the internal page loader timer. The timer is reset on the falling edge of the $\overline{WE}$ signal if a write is initiated before the timer has timed out. The timer stays reset while the $\overline{WE}$ pin is kept low. If no more write cycles have been initiated in (t_{BLC}) after the last $\overline{WE}$ low to high transition, the part terminates the page load cycle and starts the internal write. During this time, which takes a

maximum of 10 ms, the device ignores any additional load attempts. The part can be now read to determine the end of write cycle (DATA polling). A 160 µs maximum effective byte write time can be achieved if the page is fully utilized.

Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time, (t_{BLC}). Since some applications may not be able to sustain transfers at this minimum rate, the MM28C010 permits an extended page load cycle. To do this, the write cycle must be 'stretched' by maintaining $\overline{WE}$ low, assuming a write enable controlled cycle, and leaving all other control inputs ($\overline{CE}$, $\overline{OE}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{WE}$, keeping this signal low will inhibit the page load timer. When $\overline{WE}$ returns high, the input data is latched and the page load cycle timer begins. In $\overline{CE}$ controlled write the same is true, with $\overline{CE}$ holding the timer reset instead of $\overline{WE}$.

$\overline{\text{Data}}$ Polling

The MM28C010 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. $\overline{DATA}$ polling is a method of minimizing write times by determining the actual end point of a write cycle. If a read is performed to any address while the MM28C010 is still writing, the device will present the Ones-complement of the last data byte written. When the MM28C010 has completed its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly. A $\overline{DATA}$ polling read should not be done until a minimum of t_{LP} microseconds after the last byte is written. Timing for a $\overline{DATA}$ polling read is the same as a normal read once the t_{LP} specification has been met.

Power Up/Down Considerations

There is internal circuitry to minimize a false write during V_{CC} power up or power down. This circuitry prevents writing under any one of the following conditions:

1. V_{CC} is less than V_{WI} V.
2. A high to low Write Enable ($\overline{WE}$) transition has not occurred when the V_{CC} supply is between V_{WI} V and V_{CC} with $\overline{CE}$ low and $\overline{OE}$ high.

Writing will also be inhibited when $\overline{WE}$, $\overline{CE}$, or $\overline{OE}$ are in TTL logical states other than that specified for a byte write in the Mode Selection table.

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Absolute Maximum Stress Range*

Temperature
Storage ..... –65°C to +150°C
Under Bias ..... –65°C to +135°C

All Input or Output Voltages with Respect to V_{SS} ..... + 6 V to – 0.5V

"COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

	MM28C010
Temperature Range	–55°C to +125°C (case temp.)
V_{CC} Power Supply	5V ± 10%

Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N K	Minimum Endurance[4]	10,000 1,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T_{DR}	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

DC Characteristics Read Operation (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I_{CC}	Active V_{CC} Current		70	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}; All I/O = 0 ma; Addr = 5 MHz
I_{SB_1}	Standby V_{CC} Current (TTL Inputs)		10	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL}; All I/O = 0 ma;
I_{SB_2}	Standby V_{CC} Current (CMOS Inputs)		2	mA	$\overline{CE}$ = V_{CC} –02; A15, A16 = V_{CC} –0.2 Other Inputs = V_{IH} All I/O = 0 ma
I_{IL}[2]	Input Leakage Current		5	µA	V_{IN} = V_{CC} Max.
I_{OL}[3]	Output Leakage Current		25	µA	V_{OUT} = V_{CC} Max.
V_{IL}	Input Low Voltage	–0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	6	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –400 µA
V_{WI} [1]	Write Inhibit Voltage	3.8		V	

NOTES:
1. Characterized. Not tested.
2. Inputs only. Does not include I/O.
3. For I/O only.
4. Endurance can be specified as an option to be 1000 or 10000 cycles/byte minimum.

Capacitance [1] T_A = 25°C, f = 1 MHz

Symbol	Parameter	Max.	Conditions
C_{IN}	Input Capacitance	30 pF	V_{IN} = OV
C_{OUT}	Data (I/O) Capacitance	40 pF	$V_{I/O}$ = OV

E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP} [2]	E.S.D. Tolerance	>1000 V.	M_{IL}-STD 883 Test Method 3015

A.C. Test Conditions

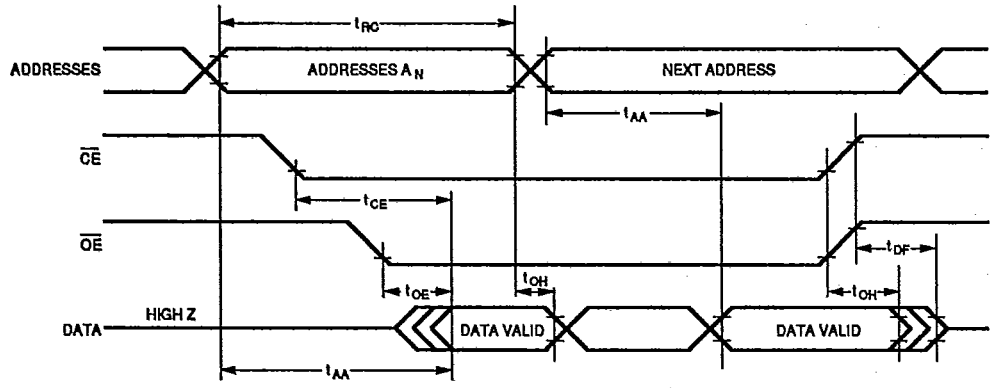
Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: < 10 ns
Input Pulse Levels: 0.45 V to 2.4 V
Timing Measurement Reference Level:
Inputs 0.8 V and 2 V
Outputs 0.8 V and 2 V

AC Characteristics

Read Operation (Over operating temperature and V_{CC} range, unless otherwise specified)

Symbol	Parameter	Limits						Units	Test Conditions
		MM28C010-250		MM28C010-300		MM28C010-350			
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	250		300		350		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{CE}	Chip Enable Access Time		250		300		350	ns	$\overline{OE}$ = V_{IL}
t_{AA}	Address Access Time		250		300		350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
t_{OE}	Output Enable Access Time		150		150		150	ns	$\overline{CE}$ = V_{IL}
t_{DF}	Output or Chip Enable High to Output in Hi-Z	0	60	0	80	0	80	ns	$\overline{CE}$ = V_{IL}
t_{OH}	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Read /$\overline{DATA}$ Polling Cycle



NOTES:
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

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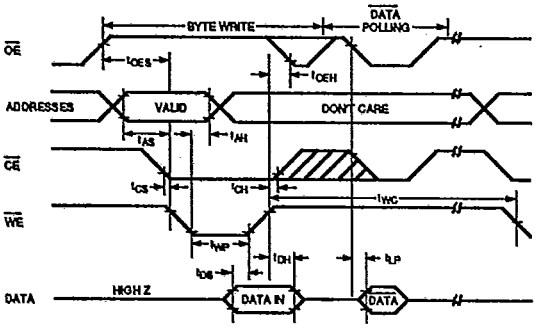
AC Characteristics

Write Operation (Over the operating temperature and V_{CC} range, unless otherwise specified)

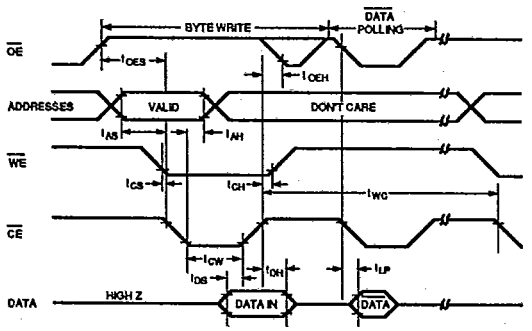
Symbol	Parameter	Limits						Units
		MM28C010-250		MM28C010-300		MM28C010-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10		10	ms
t_{AS}	Address Set-up Time	20		20		20		ns
t_{AH}	Address Hold Time (see note 1)	150		150		150		ns
t_{CS}	Write Set-up Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width (see note 2)	150		150		150		ns
t_{OES}	$\overline{OE}$ High Set-up Time	20		20		20		ns
t_{OEH}	$\overline{OE}$ High Hold Time	20		20		20		ns
t_{WP}	$\overline{WE}$ Pulse Width (see note 2)	150		150		150		ns
t_{DS}	Data Set-up Time	50		50		50		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{BLC}	Byte Load Timer Cycle (Page Mode Only) (see note 3)	0.2	200	0.2	200	0.2	200	µs
t_{LP}	Last Byte Loaded to $\overline{DATA}$ Polling		1		1		1	ms

Write Timing

$\overline{WE}$ CONTROLLED WRITE CYCLE

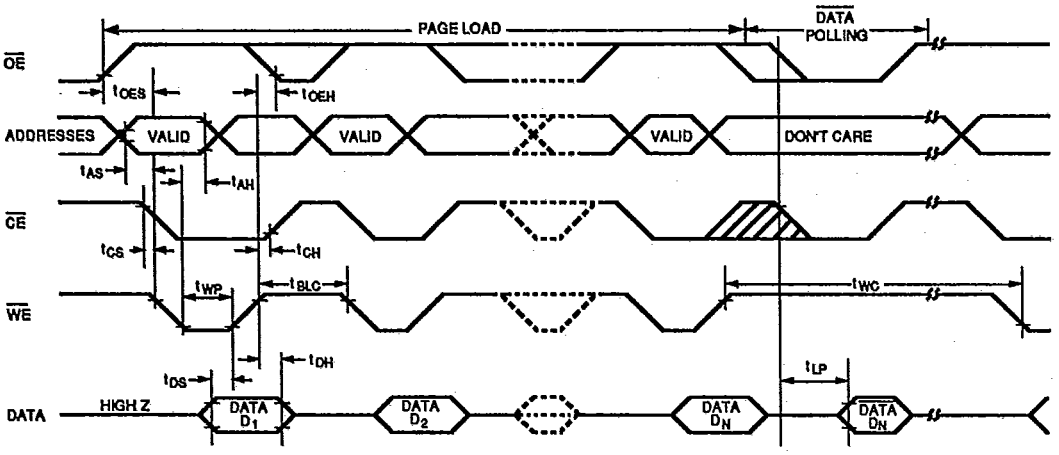


$\overline{CE}$ CONTROLLED WRITE CYCLE

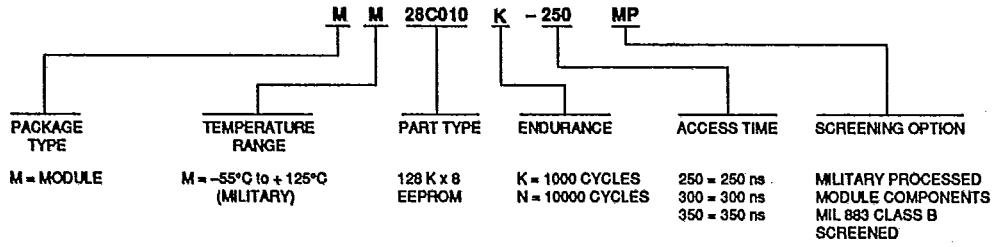


NOTES:
1. Address hold time is with respect to the falling edge of the control signal $\overline{WE}$ or $\overline{CE}$.
2. $\overline{WE}$ and $\overline{CE}$ are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t_{BLC} min. is the minimum time before the next byte can be loaded. t_{BLC} max. is the minimum time the byte load timer waits before initiating internal write cycle.

Page Write Timing



Ordering Information



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