Philips Components–Signetics

Document No.	
ECN No.	
Date of Issue	December 1988
Status	Preliminary Specification
Data Communication Products	

NE5080

High-speed FSK modem transmitter

DESCRIPTION

The NE5080 is the transmitter chip, of a two-chip set, designed to be the heart of an FSK modem. (The NE5081 is the receiver chip.) The chips are compatible with the IEEE 802.4 standard for a "Single-Channel" Phase-Continuous-FSK Token Bus." The specifications shown in this data sheet are those guaranteed when the transmitter is tuned for the frequencies given in the 802 standard. However, both the NE5080 and the NE5081 may be used at other frequencies. The ratio of logic high to logic low frequencies is normally at 1.67 to 1.00 at any center frequency; however, it can be varied externally. (See AN1950.)

FEATURES

- Meets IEEE 802.4 standard
- Data rates to several Megabaud
- Half- or full-duplex operation
- Jabber function on-chip

APPLICATIONS

- Local Area Networks
- Point-to-point communications
- Factory automation
- Process control
- Office automation

PIN CONFIGURATION

N Package

OSC 1	1	16	OSC 2
JABBER FLAG	2	15	REGULATOR BYPASS
JABBER CONTROL	3	14	DATA INPUT
V$_{CC1}$	4	13	GND 1
TRANSMIT GATE	5	12	OSC 3
FSK OUTPUT	6	11	GND 2
CABLE GND	7	10	N.C.
V$_{CC2}$	8	9	N.C.

TOP VIEW

ORDERING CODE

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
16-Pin Plastic DIP	0°C to +70°C	NE5080N
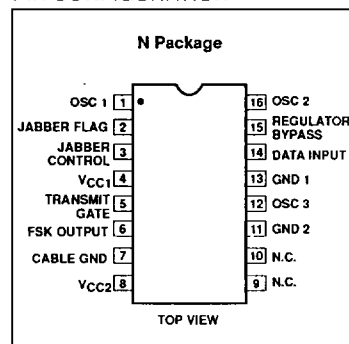
BLOCK DIAGRAM
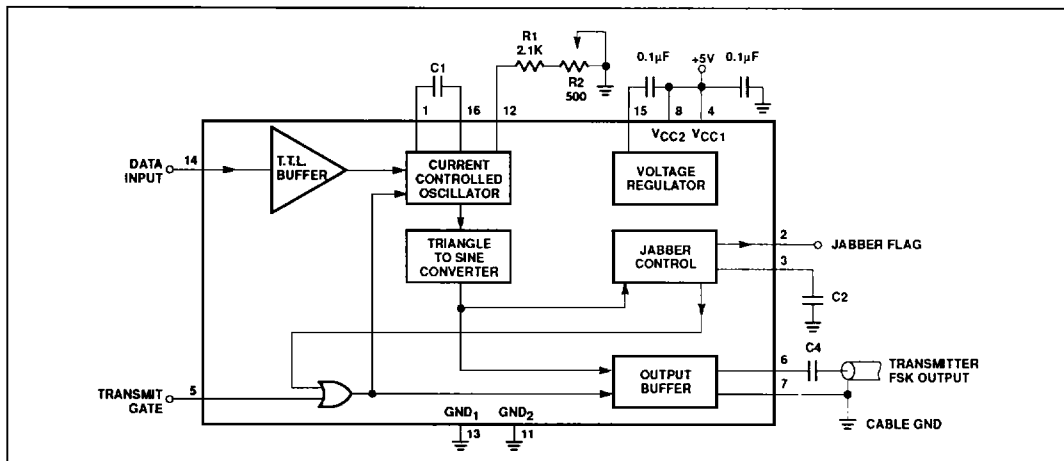
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GENERAL DESCRIPTION

The NE5080 is designed to transmit high fre-
quency asynchronous data on coaxial cable, at
rates from DC to 2M baud (see Note 1). The
chip accepts serial data and transmits it as a
periodic signal whose frequency depends on
whether the data is high or low.

The device is meant to operate at a frequency
of 6.25MHz for a logic high and 3.75MHz for a
logic low (see Note 2). The frequency is set up
by external trimming components; however,
the ratio of the high and low frequencies is set
internally and cannot be altered.

The FSK output can be turned off by use of the
transmit gate pin. When turned off, the trans-
mitter has a high output impedance and the os-
cillator is disabled.

The length of time a transmitter can transmit
can be controlled by the use of the Jabber con-
trol pin (see description of Jabber Control Pin).

Jabber Control Pin

During the time the transmitter is transmitting,
this pin sources a current. This current can be
used to set the maximum time that the transmit-
ter can be on. There are three options that can
be used:

   1. Use the current to charge a capacitor.
   When the voltage across the cap gets to
   approximately 1.4V, the transmitter will
   turn off. A logic low applied to Pin 3 will
   reset the Jabber function; an open collec-
   tor output should be used for this pur-
   pose. A logic high applied to the pin will
   disable the transmitter.

   2. Use to externally sense the current and
   have external circuitry to control the
   length of time the transmitter is on

   3. The pin can be tied to ground and is
   then not active. Transmission is then con-
   trolled solely by the signal at the transmit
   gate pin.

Jabber Flag Pin

This pin will go to a logic high when the Jabber
Control pin is used to shut off the transmitter. It
will latch and can be reset by applying a logic
low to the Jabber Control pin.

NOTES:
1. The NE5080 is capable of transmitting up
   to 1M baud of differential Manchester
   code at a center frequency of 5MHz.
2. Although the chip is designed to meet the
   requirements of IEEE standard 802.4 (To-
   ken-Passing Single-Channel Phase-Con-
   tinuous-FSK Bus), it can be used at other
   frequencies.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC1} V_{CC2}	Supply Voltage	+6	V
V_{IN}	Input voltage range (Data, Gate)	–0.3 to V_{CC}	V
P_D	Power dissipation	800	mW
T_A	Operating temperature range	0 to +70	°C
T_J	Maximum junction temperature	+150	°C
T_{STG}	Storage temperature range	–65 to +150	°C
T_{SOLD}	Lead temperature (soldering, 10sec)	300	°C

NE5080 PIN FUNCTION

PIN	FUNCTION
1	**OSC 1:** One end of the external capacitor used to set the carrier frequency.
2	**Jabber Flag:** This pin goes to a logic high if the transmitter attempts to transmit for a longer time than allowed by the Jabber control function.
3	**Jabber Control:** Used to control transmit time. See note on Jabber function.
4	V_{CC1}: Voltage supply
5	**Transmit Gate:** A logic flow on this pin will enable the transmitter, a logic high will disable it.
6	**Transmitter FSK Output**
7	**Cable Ground:** The shield of the coax cable should be connected to this pin and to Pin 11.
8	V_{CC2}: Connect to Pin 4 close to device.
9	**No Connection**
10	**No Connection**
11	**Ground 2:** Connect to Analog ground close to device
12	**OSC 3:** A variable resistor between this point and ground is used to set the carrier frequencies
13	**Ground 1:** Connect to Analog close to device
14	**Data Input**
15	**Regulator Bypass:** A bypass capacitor between this pin and V_{CC1} is required for the internal voltage regulator function.
16	**OSC 2:** One end of a capacitor that is between Pin 1 and Pin 16 and is used to set the carrier frequency.

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NE5080

DC ELECTRICAL CHARACTERISTICS $V_{CC1,2} = 4\ 75\text{–}5.25V$, $T_A = 0°C$ to $+70°C$.

SYMBOL	PARAMETER	TEST CONDITIONS	Min	Typ	Max	UNIT
				LIMITS		
f_1	Output frequency (Logic high)	Data input $\geq 2.0V$ (See Note 1)	6.17	6.25	6.33	MHz
f_0	Output frequency (Logic low)	Data input $\leq 0\ 8V$ (See Note 1)	3.67	3 75	3.83	MHz
V_O	Output amplitude	Data input $\geq 2.0V$ or $\leq 0.8V$ Output Load $= 37.5\Omega$	0.5		1 0	V_{RMS}
R_{OFF}	Output impedance (gated off)	Transmit gate $\geq 2.0V$	100			$k\Omega$
R_{ON}	Output impedance (gated on)	Transmit gate $\leq 0.8V$			37 5	Ω
C_O	Output capacitance	Transmit gate $\geq 2\ 0V$ or $\leq 0.8V$			10	pF
V_F	Feedthrough	Transmit gate $\geq 2.0V$ 2.0MHz sq wave (TTL levels) input			1	mV_{RMS}
I_J	Jabber current	Transmit gate $\leq 0.8V$ Input $\geq 2.0V$ or $\leq 0.8V$		1.25		μA
I_{CC}	Supply current	V_{CC1} connected to V_{CC2}		75	100	mA
Logic levels						
	Data Input					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	$V_{IN} = 2\ 4V$			40	μA
I_{IL}	Input current	$V_{IN} = 0.4V$			-1.6	mA
	Transmit gate					
V_{IH}	Logic high	Input high voltage	2.0			V
V_{IL}	Logic low	Input low voltage			0.8	V
I_{IH}	Input current	$VG = 2.4V$			40	μA
I_{IL}	Input current	$VG = 0.4V$			-1.6	mA
	Jabber flag					
V_{OH}	Logic high	$I_{OH} = -400\mu A$	2 4			V
V_{OL}	Logic low	$I_{OL} = 4.0mA$			0 4	V
	Jabber control					
V_{iH}	Logic high	Input high voltage	2 0			V
V_{iL}	Logic low	Input low voltage			0.8	V

NOTE:
1. Tuned per instructions in AN195.

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TO	FROM	TEST CONDITIONS	Min	Typ	Max	UNIT
						LIMITS		
t_S	Setup time	Data in	Gate on	Figure 1	2	0.1		μs
t_A	Delay time	Output freq. change	Data transition	Figure 2			150	ns
t_B	Delay time	Output disabled	Gate off	Figure 3		0.4	2	μs
t_C	Delay time	Output disabled	Jabber control	Figure 4			100	ns
t_D	Delay time	Jabber flag	Jabber control	Figure 5			100	ns
	Jabber control reset Pulse width (Logic low)				100			ns

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Figure 1. Setup Time, t_S

Figure 2. Delay Time, t_A

Figure 3. Delay Time, t_B

Figure 4. Delay Time, t_C

Figure 5. Delay Time, t_D