QT2025PxKD Data Sheet

Serial 10Gbps-to-XAUI Transceiver with Adaptive EDC

March 13, 2009

Features

- 10Gbps Operation: 10GbE LAN/WAN & 10GFC
- Advanced EDC Engine with Auto Tap Weight Adjustment & Advanced Tracking
- 10G High-Speed Interface with Integrated RX AGC, Adjustable TX Amplitude with Pre-Emphasis, and I/O Polarity Swap
- XAUI Interface with Selectable Lane Ordering, Polarity Swap, Input Equalization, Output Pre-Emphasis, Amplitude Adjust
- Ethernet Clock recovery for Synchronous Ethernet applications (125MHz and 156.25MHz)
- Integrated Loopback and Line Timing Functionality
- Integrated BER Tester, and PRBS, Packet, and Programmable Pattern Generation and Checking
- Tri-State Push/Pull 25MHz MDIO Operation with Two Additional I2C Compatible Interfaces for EEPROM External Device Configuration and External Module Status/ Control including NVR
- Compliant to Applicable IEEE & INCITS Specs
- 13mm x 13mm, 1mm Ball Pitch, BGA Package with Green/ RoHS Compliant Lead Free Option

Backplane Specific Features

- 1000BASE-KX and 10GBASE-KR Support
- Auto-Negotiation & In-Band FEC Capability
- KR Training for Channel Optimization

SFP+ Specific Features

- SFI-to-XAUI Operation for SFP+ Modules Supporting Limiting & Linear (-1 Only) Applications
- 1Gigabit Ethernet Operation for SFP Applications
- DFE/FFE Adaptive EQ for Pre/Post/Symmetric Stressors Compliant to IEEE 802.3aq
- Passive Direct Attach SFP+ Cable Support (Twinax)

XFP Module Specific Features

- Low Power XFI-to-XAUI Operation
- WIS (10GBASE-W) SONET/SDH Support with Overhead DCC Channel
- Automatic Line Timing Capability for Synchronous Operation in SONET Networks

Applications

QT2025:

- Backplane 10GBASE-KR /1000BASE-KX Support
- Hostboard Termination for SFP+/SFP Limiting Modules including 10GBASE-SR, -LR & 1000BASE-X and Passive Direct Attach SFP+ Cable
- Hostboard Termination for XFP Modules including 10GBASE-R & -W Protocols

QT2025-1:

- Hostboard Termination for SFP+/SFP Limiting & Linear Modules: 10GBASE-LRM/SR/LR/1000BASE-X and Passive Direct Attach SFP+ Cable
- On-board PHY inside XENPAK/X2 Modules for 10GBASE-LRM, -R & -W Protocols

General Description

The QT2025 is a fully integrated 9.95-10.52 Gbps transceiver with fully adaptive Electronic Dispersion Compensation (EDC) capabilities. The device provides a high performance interface between a MAC or switch device and copper media including Twinax Cable and 10GBASE-KR backplanes. The data rate is switchable to 1.25 Gbps, allowing dual 1000BASE-KX / 10GBASE-KR support on a single backplane design using Auto-negotiation for rate selection.

It can also interface to optical media including SFP+, SFP and XFP modules or reside inside a XENPAK or X2 module. When designing for SFP+ applications, customers can generate one dual-rate design that supports SFP+ modules (10GBASE-R) and SFP modules (1000BASE-X), as well as Twinax cable, providing maximum medium flexibility.

In the receive direction the device uses a sophisticated EDC engine that continuously adapts itself to the channel characteristics providing an optimum level of performance regardless of environmental conditions. The QT2025-1 was designed to exceed the performance specified in the 10GBASE-LRM Standard.

In the transmit direction, the 10Gbps driver utilizes signal equalization to compensate for degradation due to copper traces and connectors in the signal path.

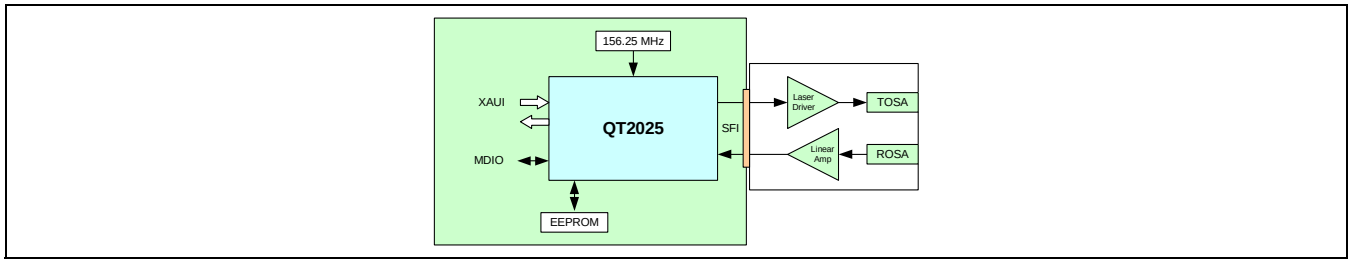
The QT2025 includes two standard two-wire interfaces (plus MDIO) for auto/manual initialization, firmware loading, NVR, & optical module status/control.

Firmware

The PHY is provided with a firmware program that runs on the built-in 8051 microprocessor. The firmware configures the PHY for different applications and works in conjunction with the silicon to provide the features and performance specified in this document.

Please consult the AMCC website for access to the production firmware.

Figure 1: System Block Diagram



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QT2025 Overview

The QT2025 implements the high speed interface for 10GbE LAN/WAN, 10GFC, 1GbE equipment and associated optical modules. The QT2025 devices may be used in diverse applications including:

QT2025: 10GBASE-KR, 1000BASE-KX Backplane Support

SFP+/SFP Limiting Module Applications

Passive Direct Attach SFP+ Cable Applications

XFP Module Applications

QT2025-1: SFP+/SFP Linear and Limiting Module and Passive Direct Attach SFP+ Cable Applications

XENPAK/X2 10GBASE-LRM Applications

The basic flow of operations is contained in lists below and the detailed descriptions of all of the features are contained in the applicable sections. An important feature of the device, the on-chip EDC engine, provides equalization for Multimode Fiber (to meet the IEEE 10GBASE-LRM spec in the QT2025-1), FR4 and connector effects. The EDC engine is fully adaptable to compensate for cable variations and the system is field programmable in order to support standards changes or emerging standards such as 10GBASE-VSRM (850 linear w/EDC). The 10G transmitter includes waveform reshaping capability, allowing the signal jitter content to be minimized. This enables low bit error rate and transmission over longer trace lengths.

Serial 10G (RX Channel) to XAUI Operations

1. FRXI Serial Data Input
2. AGC w/DC Offset Control
3. EDC & CDR; DeMultiplexer and Clock Divider
4. Receive WIS (Optional), Frame Sync, Descrambler
5. 66B/64B Decoder, Rate Adjust, 8B/10B Encoder
6. XDRV XAUI Data Output

XAUI (TX Channel) to Serial 10G Operations

1. XCDR XAUI Data Input
2. Phase Adjust & Demultiplexer
3. XAUI Code Synchronization & Lane Alignment
4. 8B/10B Decoding, Rate Adjust, 64/66B Encoding
5. Scrambler and Gear Box
6. Transmit WIS (Optional), Mux, & Clock Generation
7. 10G FTXI Serial Data Output

Table 1: Standard Compliance List

Standard	Revision	Date
Backplane Ethernet Standard 10GBASE-KR, 1000BASE-X: IEEE 802.3ap-2007	Released 2007	March 22, 2007
SFP+ Standard: SFF-8431 Specification for Enhanced 10 Gigabit Small Form Factor Pluggable Module “SFP+”	Revision 2.2	December 19, 2007
XFP Standard: INF-8077i 10 Gigabit Small Form Factor Plug-gable Module	Revision 4.5	August 31, 2005
SFP Standard: INF-8074i Specification for SFP (Small Form Factor Pluggable) Transceiver	Revision 1.0	May 12, 2001
IEEE Ethernet: Std. 802.3-2005	Released 2005	December 12, 2005
IEEE LRM: 802.3aq/D4.0	D4.0	May 2007
IEEE JTAG: IEEE Std. 1149.1-2001	Released 2001	
IEEE Std. 1149.6-2003	Released 2003	
10G Fibre Channel: INCITS T11/Project 1413-D	Revision 3.1	June 7, 2002
JEDEC Power Supply and Voltage Interface Standard: JEDEC JESD8-11		October, 2000
JEDEC ESD: JEDEC JESD22-A114-B		June, 2000
JEDEC/IPC Handling, Packaging, Shipping and Reflow of Sensitive SMD's: IPC/JEDEC J-STD-033A	Revision 1.0	July 2002
SONET: GR-253-CORE	Issue 3	September, 2000
XENPAK MSA	Issue 3.0	September 18, 2002
RoHS Directive		February 13, 2003

Note: Standards compliance only relates to applicable sections pertaining to this product type.

QT2025-1 Application: 10GE SFP+ Line Card

The QT2025-1 device supports the high-speed 10G serial SFI performance specifications. It is fully compatible with industry standard SFP+ modules and supports two reference clock rates as shown in Figure 2. Direct Attach SFP+ cable applications are also supported.

QT2025-1 Application: 1GE SFP on a 10GE Line Card

The QT2025-1 device supports the related 1GE protocol and is fully compatible with industry standard 1GE SFP modules. In this mode, the PHY supports a 1GE signal on XAUI Lane 0 and interfaces to the SFP module on the same pins used for 10GE.

All hardware configurations for the QT2025-1 are the same between the 1GE and 10GE applications. The host system must configure the device to operate with the installed module.

Figure 2: QT2025-1 SFP+ Application

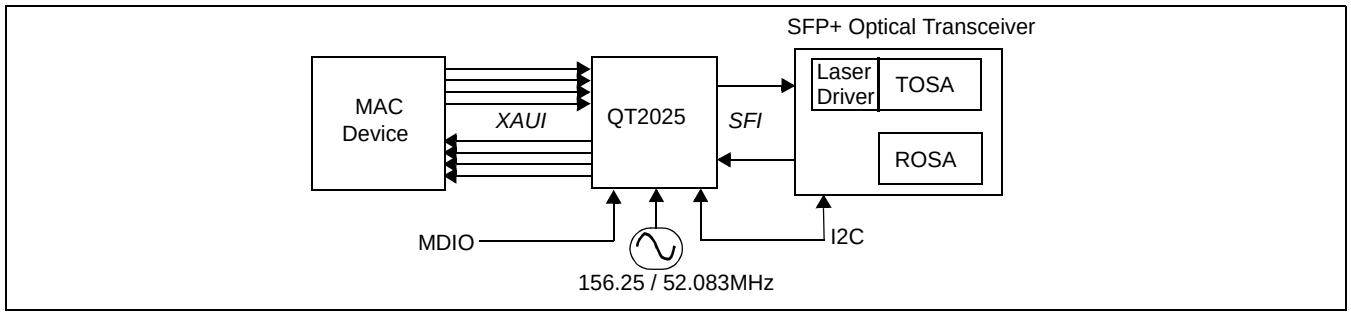
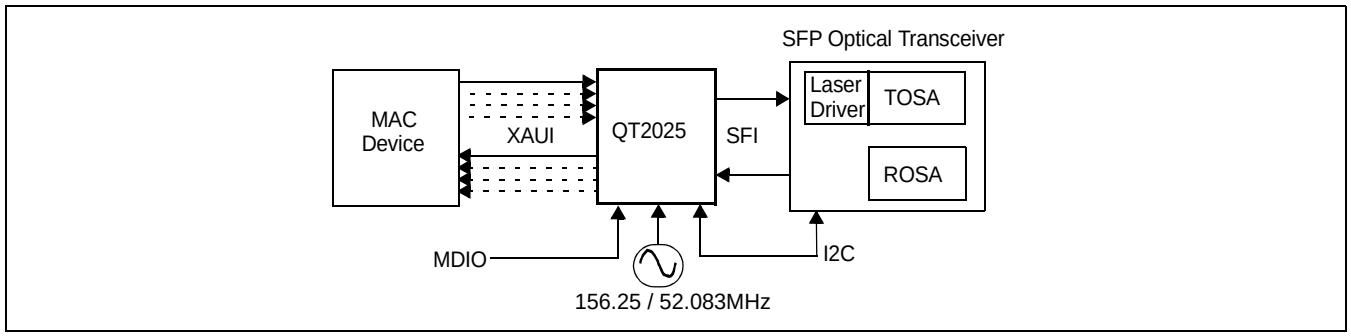


Figure 3: QT2025-1 1GE SFP Application



QT2025 Application: 10GbE XFP Line Cards

The QT2025 device supports the high-speed 10G serial XFI performance specifications. Figure 4, below, shows the QT2025 in a 10GbE LAN/PHY with optional WIS support. XFI Rx equalization and/or XFI Tx pre-emphasis can be activated to allow the designer to use longer FR-4 traces on the XFI interface or to compensate for marginal PCB performance.

QT2025 Application: 10GbE over Backplane

The QT2025 supports 10GBASE-KR applications and the device, when enabled in KR Mode, provides transmit pulse shaping that gets optimized for each backplane channel using link training specified in IEEE 802.3ap.

Figure 5, below, shows a typical blade server application. In this case, the QT2025 converts the XAUI signal from a 10G Ethernet MAC engine to 10GBASE-KR on a single differential signal pair. On the server blades themselves, there are typically two ports (for failover and/or increased bandwidth). Each server port must be matched by a port on the switch blade. ATCA backplane applications look very similar to the blade server application.

Figure 4: QT2025 XFP Application

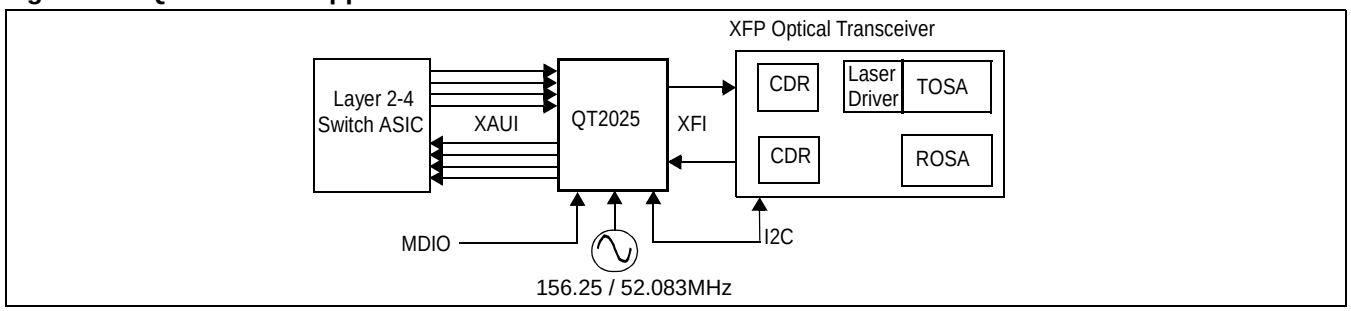
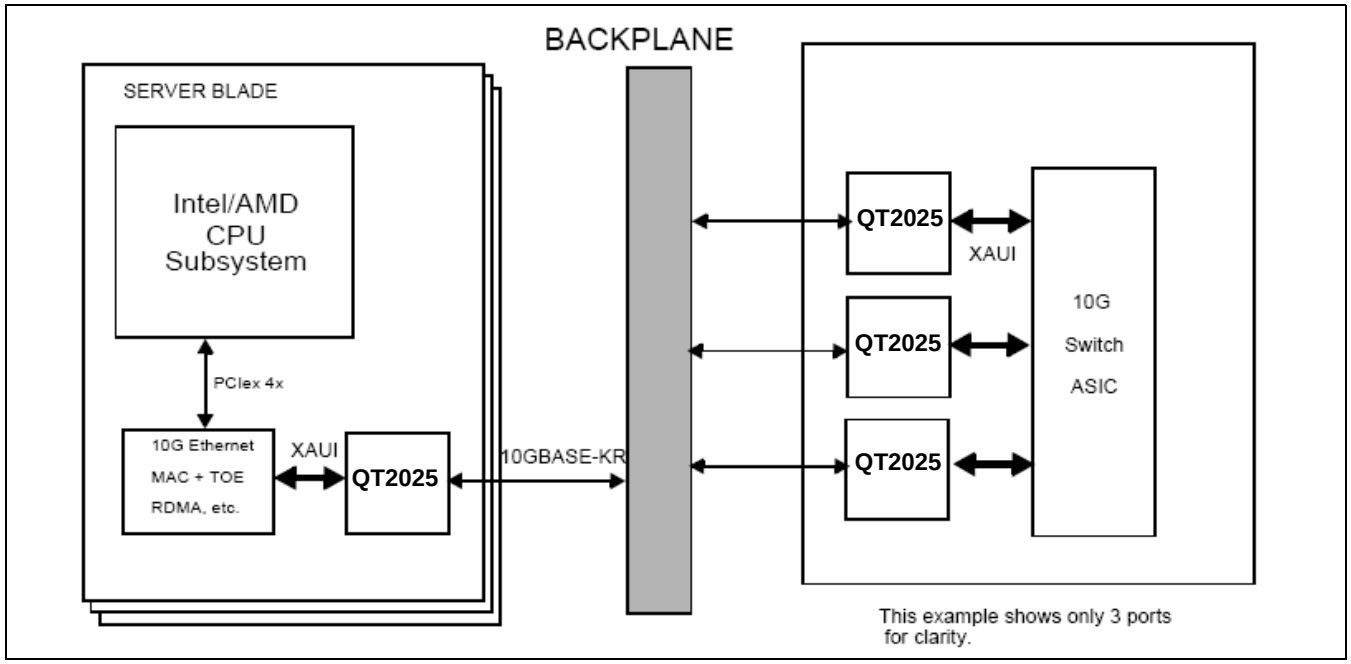
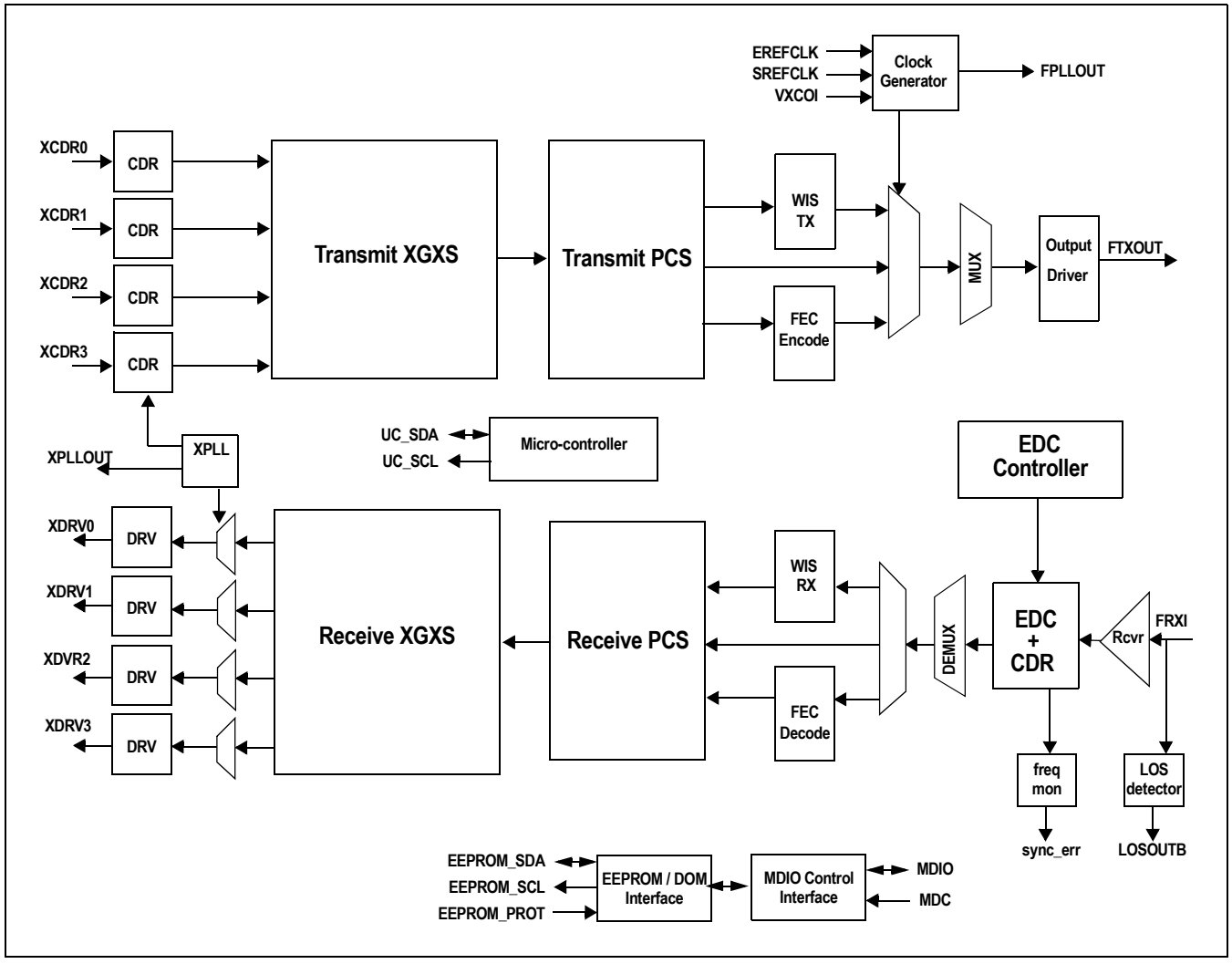


Figure 5: QT2025 10GBASE-KR Backplane Application



Functional Block Diagram

Figure 6: QT2025 – Functional Block Diagram



Functional Description

This section describes the functional blocks of the QT2025 illustrated below. Each block will be described in the following sections.

Transmit Data Path: XAUI Interface

The XAUI input accepts 4 differential 3.125Gbps data lanes on inputs XCDR0 - XCDR3. The data must be encoded as specified by IEEE 802.3 Clause 47. The XAUI signal is recovered, synchronized and deskewed. The data is then passed through a rate compensation block. Finally, the data is 10b/8b decoded and passed to the next block for 64b/66b encoding.

XAUI I/O & CDR

At the XAUI inputs, clock and data are recovered for each of the four 3.125Gbps input lanes. The differential receivers used at this interface have 100Ω differential input impedance and are intended to be AC coupled. The XAUI interface includes a passive equalization circuit to improve tolerance for sub-optimal XAUI interface design.

Transmit XGXS

Phase Adjust/Demux

The signal from each lane is phase adjusted to a single clock and then demultiplexed.

XAUI Code Synchronization

The Code Synchronization block delineates the 10 bit code word boundaries by identifying the comma character in the K28.5 Idle code. This is performed independently on each lane. The code synchronization status is displayed in Register bits 4.0018h[3:0].

If any single lane loses signal (no transitions detected), the code sync block will not attempt to achieve sync on the XAUI input lanes. The QT2025 will report ‘loss of sync’ on all 4 lanes. However, when transitions are received on all 4 lanes, the code sync block is fully active. If no K28.5 codes are detected on a given lane, the QT2025 will report ‘loss of sync’ independently for each lane.

XAUI Lane Alignment

The incoming XAUI data must be aligned due to varying off-chip transmission delays between the four lanes. The alignment operation is done by aligning /A/ codes on all four lanes. The /A/ codes appear randomly in the idle data stream and are transmitted simultaneously at the source on all four channels as a single column of data, ||A||.

The QT2025 can tolerate a skew of up to 40 bits between any two lanes at the XCDR input pins.

8B/10B Decoding

Each 10 bit code word is decoded into 8 data bits and 1 control bit. The 8 data bits and 1 control bit are then passed on to the rate adjust function.

8B/10B coding errors are counted on a per lane basis. For each lane, errors are reported in an 8 bit, non-rollover counter that is read cleared. The four counters for Lane 0 to Lane 3 are located in the lower byte of MDIO registers 4.C030h - 4.C033h.

Transmit Rate Adjust

Data is written into a rate compensation FIFO. The outgoing data is read out using a clock derived from the local reference clock. Idle codes or sequence ordered_sets from the data stream are added or dropped to compensate for the clock rate difference. The minimum inter-frame gap (IFG) of five characters and sequence ordered_sets are always maintained.

Proper rate compensation will always be performed when the clock rates are within 200ppm. In LAN mode, the QT2025 can tolerate a continuous input and output stream of back-to-back 9600 byte jumbo frames with minimum IFG. In WAN mode, this is limited to 2 jumbo frames with minimum IFG. If the clock rate difference exceeds 200ppm or multiple back-to-back jumbo frames are transmitted, one or more packets may be corrupted.

Transmit rate adjust operation is monitored in MDIO register 4.C002h. This register flags idle code removal and insertion in bits [15:14] (normal operation), as well as overflow/underflow in bits [9:8] (fault condition).

Transmit PCS

64B/66B Encoding

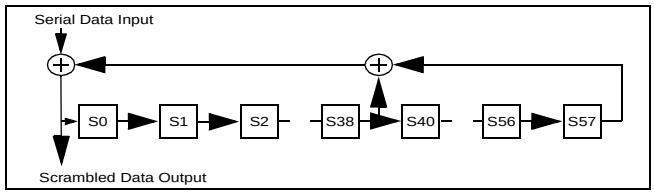
The encoder takes 64 bits of input data and the associated 8-bit control word from the XAUI block and creates a new 66 bit data bus. The 66 bits are composed of 2 sync bits followed by 64 bits of data. The sync bits are used to synchronize the data stream on a frame boundary. The sync bits [1:0] are 10 if 64 bit data bus is composed solely of data words. If the bus contains 1 or more control words, the sync bits [1:0] are set to 01 and are followed by a 8 bit type data. The type word indicates the content of the following 56 bits of data. The sync bit values of 00 or 11 are invalid.

Incoming control words are converted from 8 bits to 7 bits. Data words are not altered. When combinations of data and control words are used in a bus, extra bits are inserted if needed at the boundary between the data and control words to make the total number of bits 64. Ordered set control codes are encoded using a combination of the block's type field and a 4 bit O code for each ordered set.

Scrambler

The 66-encoded data is scrambled before transmission. The scrambler polynomial is $1+x^{39}+x^{58}$. Only the 64 data bits pass through the scrambler. The sync bits are not scrambled. The scrambler can be bypassed by setting the MDIO register bit 3.C000h[2]. The scrambler is depicted in Figure 7.

Figure 7: Transmit Scrambler



Gearbox

The gearbox converts the data from a 66 bit wide data bus at 156.25 Mb/s to a 64 bit wide bus at 161.1328 Mb/s. This step is required to prepare the data for serialization in the next functional block.

Transmit 10G Driver

Transmit WAN Interface Sublayer (WIS)

When enabled, via 2.0007h[0], the optional TX WIS block accepts data from the Gearbox and maps it into the payload of the transmitted STS-192C WIS frame stream. Fixed stuff octets are added, together with a set of Path Overhead octets, to create a Synchronous Payload Envelope (SPE). Line and Section Overhead octets are combined with the SPE and then scrambled using the frame-synchronous scrambler to produce the final transmitted WIS frame. The WIS continuously generates one WIS frame every 125µs.

The WIS function is not supported in 10GBASE-KR applications.

Transmit FEC

The QT2025 implements an optional FEC (Forward Error Correction) sublayer for 10GBASE-R applications to improve link performance. The chip uses an in-band FEC encoding that does not consume additional bandwidth, and so is compatible with currently supported PMD devices. It is optimized to handle short bursts of errors in the signal. The implementation is compliant to IEEE 802.3ap Clause 74 and is specifically intended for 10GBASE-KR applications.

The FEC sublayer acts on the scrambled 66b encoded data blocks from the PCS layer. The algorithm encodes FEC information across a group of 32 data blocks, forming a FEC frame that is 66 x 32 = 2112 bits long. The FEC Transmitter engine consists of a Transcoder, Encoder and Scrambler. An Error Injector is also available. The Transcoder shortens each block from 66 bits to 65 bits by reducing the sync header field from 2 bits to 1. The Encoder calculates a 32-bit parity-check field across the FEC frame that is appended to the frame end. The Scrambler is then applied to the frame before it is transmitted.

The FEC block is described in detail in "FEC Encoding/ Decoding" on page 41

Transmit Multiplexer and Clock Generation

A clock divider generates the clock frequencies required to multiplex the 64 bit wide bus coming from the previous block into a single 10Gbps output, from the locally generated 10GHz clock.

Output Data Driver

The output driver is a differential pair, FTXOUTN and FTXOUTP, which are both terminated on chip with 50Ω to 1.8V. The output level can be adjusted and output polarity inverted with a vendor specific MDIO register. The output driver has the ability to emphasize the output to overcome frequency dependent loss of FR4.

Receive Data Path: 10G Interface

Linear Equalizer/AGC

The QT2025 is configured with a front end Linear Equalizer/AGC with a DC Offset circuit which provides an equalized, fixed amplitude signal to the EDC engine input (Figure 8). The input must be externally AC-coupled.

EDC Engine

In 10GBASE-LRM applications (QT2025-1 Only), an adaptive Electronic Dispersion Compensation Engine is used to equalize signal impairments caused by the transmission channel response. The equalizer employs a linear AGC amplifier and both a Feed Forward Equalizer (FFE) and a Decision Feedback Equalizer (DFE). The values of the tap weights in the FFE and DFE are adapted automatically.

In backplane applications only the DFE is used to save power.

Adaptive Data Recovery

The clock and data recovery adapt both the phase and decision threshold of the sampling point for optimum BER.

Clock Recovery

The signal from EDC block is passed to a clock and data recovery (CDR) circuit. The clock recovery circuit recovers the clock from the received signal. The recovered clock is used to time the EDC engine and provides the frequency reference from the receiver. When the PLL is frequency locked to the incoming data the internal signal, frxlock, is asserted. When frxlock is low the receive data outputs XDRV<3:0> will transmit idle frames and error codes. The state of frxlock is reflected in the ‘PMA receive link status’ bit, 1.0001h.2 and 1.0008h.10, a latched low and latch high register bit respectively whose value is determined by the equation {frxlock AND RXLOSB_I}. The state of the RXLOSB_I input is available in Register bit 1.D002h.2.

Recovered Clock Frequency Monitoring

When the receive recovered clock is more than 500ppm from the transmit reference clock, a synchronization error is declared and the internal signal *sync_err* goes high. *sync_err* can be viewed at MDIO register 1.C001h.1. This is a latched high register bit that is cleared on read. On powerup or reset, the register must be read to clear it.

Demultiplexer and Clock Divider

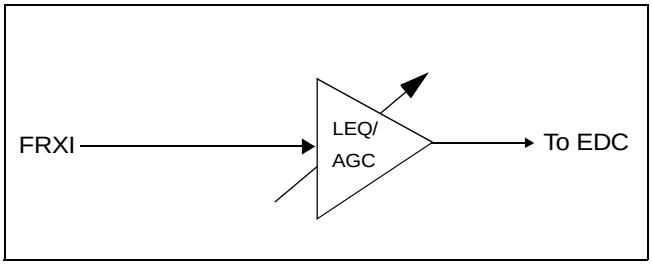
All clocks needed for the demultiplexer and the reset of the receive path are generated in this block by dividing down the 10GHz recovered clock. The demux converts the 10 Gbps serial incoming data into 64 parallel bits.

Receive WAN Interface Sublayer (WIS)

The RX WIS block receives data from a SONET link and extracts the Ethernet payload from the STS-192c SPE. It also monitors the integrity of data at the Section, Line and Path levels and monitors both near and far end faults. The WIS receive and transmit blocks are bypassed in 10GBASE-R applications.

The WIS function is not supported in 10GBASE-KR Backplane applications.

Figure 8: Receiver Input



Receive FEC

The QT2025 implements an optional FEC (Forward Error Correction) sublayer for 10GBASE-R applications to improve link performance. The chip uses an in-band FEC encoding that does not consume additional

bandwidth, and so is compatible with currently supported PMD devices. It is optimized to handle short bursts of errors in the signal. The implementation is compliant to the IEEE 802.3ap Standard and specifically intended for 10GBASE-KR applications.

The FEC sublayer acts on the scrambled 66b encoded data blocks from the PCS layer. The algorithm encodes FEC information across a group of 32 data blocks, forming a FEC frame that is 66 x 32 = 2112 bits long. The FEC Receiver Engine consists of a De-Scrambler, Block Synchronizer, Decoder and Reconstructor, along with an Error Monitor.

Receive PCS

Frame Synchronization

The frame synchronizer takes the 64 bit wide data bus output from the demultiplexer and converts it to a 66 bit wide data bus. The 66 bits are composed of 2 sync bits followed by 64 bits of data. The sync bits are used to synchronize the data stream on a frame boundary. The bus rate at each stage will depend on the selected protocol.

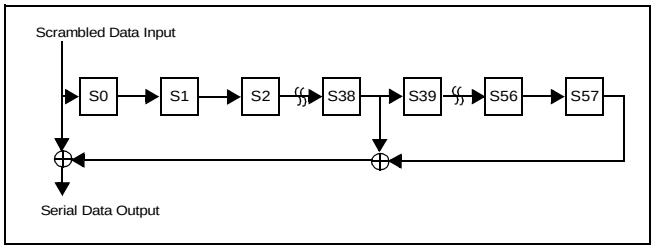
The chip also monitors invalid sync header bits. Valid sync bits include 01b and 10b. The combinations 11b and 00b are invalid. When an invalid sync header is detected, a 6-bit counter is incremented. This counter is located in MDIO register field 3.0021h[13:8]. This is a read only, non-rollover counter that is cleared when read. The counter will count a maximum of 16 sync header errors in a 125 µs window.

When there are 16 or more sync header errors in a 125µs window, the ‘hi_ber’ flag is set to 1b in MDIO register bit 3.0020h[1]. This is a read only register bit. The algorithm for counting sync header errors and detecting ‘hi_ber’ follows the ‘BER monitor state machine’ described in IEEE 802.3-2005 Figure 49-13.

Descrambler

The descrambler processes the payload to reverse the effect of the scrambler on the payload. The descrambler is self-synchronizing. It calculates the inverse of the scrambler function using the polynomial $1+x^{39}+x^{58}$. The descrambler is depicted in Figure 9. Only the 64 data bits are passed through the descrambler. The descrambler is bypassed when the scrambler bypass mode is enabled through MDIO register 3.C000h[1].

Figure 9: Receive Descrambler



66b/64b Decoder

The decoder performs the inverse function of the encoder. This block converts the 64 bit payload back into the original eight 8-bit codes. Valid code word formats are described in IEEE 802.3-2005 Figure 49-7.

Receive XGXS

Receive Rate Adjust

Data from the 66b/64b decoder is written into a rate compensation FIFO using the fiber recovered clock. The outgoing data is read out using the XAUI reference clock. Due to the fact that these clocks are derived from different sources, a rate adjust operation needs to be performed. The rate compensation block accomplishes this by either adding or dropping Idle ordered_sets, as required, from the data stream. The minimum inter packet gap of five characters and sequence ordered set messages are maintained.

Receive rate adjust operation is monitored in MDIO register 4.C002h. This register flags Idle code removal and insertion in bits [13:12] (normal operation), as well as overflow/underflow in bits [7:6] (fault condition).

8b/10b Encoder

The data bus is divided into four 8-bit wide data channels. Each of the four channels has independent 8b/10b encoders which will convert the 8 bit data lanes into 10 bit code words. Either a positive or negative disparity 10 bit code word will be selected, depending on the running disparity.

Receive XAUI Driver

Multiplexer and XAUI DRV

After 8b/10b encoding has been added, the receive multiplexer serializes data words to form four 3.125Gbps output data lanes.The XAUI output drivers

provide high-swing differential outputs with 100Ω differential output impedance and are intended to be AC coupled. The 3.125GHz timing is derived from the reference clock, EREFCLK.

The receive XAUI driver interface includes programmable pre-emphasis to compensate for sub-optimal host-side PCB design.

High Speed Interfaces

This section describes the high-speed XAUI and 10Gbps interfaces, with focus on configurable capabilities.

XAUI Interface

XAUI XCDR Input Equalization

The XAUI input includes an equalization circuit to compensate for FR4 channel loss. There are two equalization settings:

- Standard equalization (4.C05Eh[0] = 0b, default)
- Enhanced equalization (4.C05Eh[0] = 1b)

For FR4 channels that are compliant to 802.3-2005, the standard equalization setting should be used. The enhanced equalization setting can be used to compensate for exceptionally poor channels, however it will over-compensate a high quality signal and result in degraded performance, so should not be used unnecessarily.

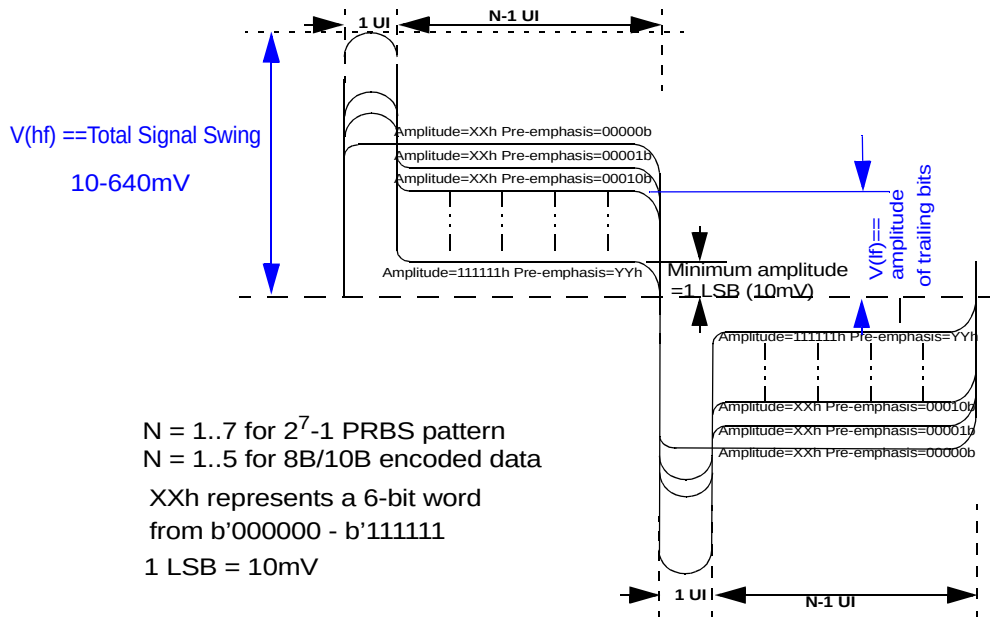
XAUI XDRV Driver

The XAUI driver uses a 2-tap FIR architecture with a 1UI spacing. The main amplitude and post-cursor taps are independently adjustable to compensate for host board transmission media effects. The settings are controlled via MDIO registers and can be set via EEPROM. Each lane is independently controlled.

The post-cursor driver increases the amplitude of the first bit following any transition in the data pattern, the leading edge of the bit being defined by the transition. The driver also decreases the amplitude of subsequent bits having the same binary value as the bit following the transition, until the next data transition occurs.

The post-cursor driver can be disabled via register bits 4.C05Ah[7:4]. The individual XAUI drivers may also be disabled from register bits 4.C05Ah[3:0].

Figure 10: XAUI XDRV Pre-Emphasis



Idealized step response for a square-wave pattern consisting of N consecutive 1's and 0's.

Programming the XAUI Driver

To program the XAUI driver to a desired setting, use the following procedure. Note that the voltages are measured differentially and refer to the peak voltage from GND for an AC-coupled signal.

1. Determine the target peak voltage. This is the "high frequency" amplitude, V(hf), from Fig. 10. Calculate the digital weight of the amplitude, hf_amp, following the formula in Table 2.
2. Determine the target voltage for the trailing bits. This is the "low frequency" amplitude, V(lf), from Fig. 8. Calculate the digital weight of the amplitude, lf_amp, following the formula in Table 2.
3. Calculate the main driver amplitude, main_xdrv_amp, and post-cursor amplitude, post_xdrv_amp.
4. Calculate XDRV_AMP_x, XDRV_DEEMP_x and HF_AMP_x. Program into MDIO register fields for each lane (x = lane number).

Table 2: XAUI Driver Parameters

Parameter	Description	Comment
V(hf)	10-640mV	High frequency voltage. Represents the peak voltage of the signal, measured on the first bit on a string of consecutive identical digits.
hf_amp	hf_amp = int (V(hf) / dV) - 1	Digital weight of the High Frequency voltage. Valid range is 0 - 63. While the maximim allowable weight is 63, a practical limit of 57 should be observed to avoid driver saturation. (This field is equivalent to the sum of the driver weights, such that hf_amp = main_xdrv_amp + post_xdrv_amp)
V(lf)	10-640mV	Low frequency voltage. Represents the voltage of the signal measured on the trailing bits in a string of consecutive identical digits.
lf_amp	lf_amp = int (V(lf) / dV) - 1	Digital weight of the Low Frequency voltage. Valid range is 0 - 63.
main_xdrv_amp	main_xdrv_amp = (hf_amp + lf_amp)/2	Digital weight of the Main Driver in the 2-tap FIR driver. Valid range is 0 - 63.
post_xdrv_amp	post_xdrv_amp = (hf_amp - lf_amp)/2	Digital weight of the Post-cursor Driver Valid range is 0 - 31.
XDRV_AMP_x	XDRV_AMP_x = 63 - main_xdrv_amp	MDIO Register field to program the main driver amplitude. There is one register field for each lane, denoted by x, where x = 0..3. Valid range 0 - 63. The register field is a 6-bit binary weighted number where the maximum value is encoded by '000000' and the minimum by '111111'.
XDRV_DEEMP_x	XDRV_DEEMP_x = 31 - post_xdrv_amp	MDIO Register field to program the post-cursor driver amplitude. There is one register field for each lane, denoted by x, where x = 0..3. Valid range 0 - 31. The register field is a 5-bit binary weighted number where the maximum value is encoded by '00000' and the minimum by '11111'.
XDRV_HF_AMP_x	XDRV_HF_AMP_x equals hf_amp when hf_amp >=30, and equals 0 when hf_amp < 30.	MDIO Register field to program the High Frequency voltage digital weight. There is one register field for each lane, denoted by x, where x = 0..3. Valid range 0 - 63. This field must be programmed only for high amplitude signals and ensures that the step size, dV, remains linear. The register field is a 6-bit binary weighted number. The value is not inverted.
dV	10mV	This is the voltage step size for a +1 LSB change in the driver weight. The main and post-cursor driver step size is the same. Measured as a peak voltage on the differential signal.

Main XDRV Amplitude

The main output driver is set by a 6-bit binary-weighted word. One LSB corresponds to +10mV peak differential voltage swing (or +20mV peak-to-peak). With a flat-channel response (post-cursor driver is off), the digital word will set the amplitude of the output.

The amplitude corresponding to the binary-weighted word is inverted, as described in Table 2.

The drive amplitude can theoretically be set in the range 20-1280mVpp differential. The binary-weighted amplitude should be kept below 57 to avoid saturating the driver (binary word of 6b'000110).

Post-Cursor XDRV Amplitude

The post-cursor output driver is set by a 5-bit binary-weighted word. One LSB corresponds to +10mV peak differential voltage swing (or +20mV peak-to-peak).

The amplitude corresponding to the binary-weighted word is inverted, as described in Table 2.

XDRV HF Amplitude Field

The HF_AMP_x register fields must be programmed to maintain amplitude linearity of the driver for large voltage swings. This field is equivalent to the sum of the main and post-cursor driver weights. When the driver weight sum is below 30, this field should be set to 0.

The register addresses to program the XAUI drivers are listed in Table 3.

Considerations

Two factors must be considered when setting the main and post-cursor amplitudes so as not to violate the chip limits and exceed the capabilities of the driver.

1) The total voltage swing should not exceed the absolute maximum of 640mVpp (single-ended). This means that the sum of the digital amplitude and post-cursor words should be less than 63 (Table 2 recommends a maximum practical limit of 57).

2) The post-cursor amplitude should always be smaller than the main amplitude setting to avoid voltage values of the opposite polarity on subsequent identical digits when looking at the differential waveform.

The calculation rules outlined in Table 2 enforce these restrictions.

Table 3: XAUI Driver Control Registers

Parameter	Register Field	Register Address	Description
Main Drivers	XDRV_AMP_0	4.C057.5:0	Lane 0 Main Driver Amplitude
	XDRV_AMP_1	4.C057.10:6	Lane 1 Main Driver Amplitude
	XDRV_AMP_2	4.C056.5:0	Lane 2 Main Driver Amplitude
	XDRV_AMP_3	4.C056.10:6	Lane 3 Main Driver Amplitude
	XDRV_DIS_x	4.C05A.3:0	Lane 3:0 Main Driver Disable Controls
Post-Cursor Drivers	XDRV_DEEMP_0	4.C059.4:0	Lane 0 Post-cursor Driver Amplitude
	XDRV_DEEMP_1	4.C059.9:5	Lane 1 Post-cursor Driver Amplitude
	XDRV_DEEMP_2	4.C058.4:0	Lane 2 Post-cursor Driver Amplitude
	XDRV_DEEMP_3	4.C058.9:5	Lane 3 Post-cursor Driver Amplitude
	XDRV_PRE_EMP_PWDN_x	4.C05A.7:4	Lane 3:0 Post-cursor Driver Disable Control
HF Amplitude Fields	XDRV_HF_AMP_0	4.C070.5:0	Lane 0 HF Amplitude
	XDRV_HF_AMP_1	4.C070.10:6	Lane 1 HF Amplitude
	XDRV_HF_AMP_2	4.C071.5:0	Lane 2 HF Amplitude
	XDRV_HF_AMP_3	4.C071.10:6	Lane 3 HF Amplitude

10Gbps Interface

Transmit Control

The QT2025 10Gbps serial transmitter has programmable amplitude control and optional post-cursor and pre-cursor emphasis using a finite impulse response (FIR) structure with a maximum of 3 taps. By adjusting FIR architecture and tap weights, different channel responses can be generated for improving signal integrity performance.

The FIR structure is configured using MDIO register FTX_10G_MODE (1.C308h[11:10]), as illustrated in Figure 11 for LR, LR+, SFP+, and KR modes. Example waveforms (differential) are provided in Figure 11 to illustrate pre-cursor and post-cursor effects for each mode, using a bit pattern of 11110000. The FIR structure uses a combination of delay and tap weighting functions to emphasize high frequency content in the waveform. A fixed Stepsize converts the tap weights to a voltage swing, where Stepsize is approximately 10mV/step.

The different 10G mode settings enable users to optimize device performance based on end-application channel characteristics. The KR mode is a requirement of the 802.3ap-2007 Standard and provides the best signal performance for backplanes. The SFP+ mode minimizes the deterministic jitter at the SFP+ module input. The LR+ mode provides a lower-power alternative to the SFP+ mode. The LR mode is a low power setting when no emphasis is desired. The modes are summarized in Table 4.

The main driver channel amplitude is controlled by the 6-bit MDIO word FTX_DATA_LVL (1.C308h[5:0]). The output signal amplitude is equal to Stepsize * C(main) in Figure 11 where C(main) is a binary weighted value set by FTX_DATA_LVL.

Post1-Cursor Emphasis

Post-cursor emphasis is used to adjust the relative amplitude of the *first* bit in a string of consecutive identical digits. This amplitude is controlled by a 5-bit word in MDIO register FTX_PST_LVL (1.C309h[4:0]). The output signal amplitude is equal to Stepsize * C(post1) in Figure 11 where C(post1) is a binary weighted value that is set by FTX_PST_LVL.

For XFP applications, the resulting waveform must still conform to the XFI eye mask with pre-emphasis invoked, which limits the peak amplitude to fall below 385mVpp.

Note that C(post1) in Figure 11 corresponds to -C(+1) in the 802.3ap-2007 Standard (Section 72.7.1.10).

Pre-Cursor Emphasis

Pre-cursor emphasis is used to adjust the relative amplitude of the *last* bit in a string of consecutive identical digits. The amplitude for pre-cursor emphasis is controlled by a 4-bit word in MDIO register FTX_PRE_LVL (1.C309h[8:5]). The output signal amplitude is equal to Stepsize * C(pre) where C(pre) is a binary weighted value that is set by FTX_PRE_LVL.

Pre-cursor emphasis is used for KR mode in Figure 11.

Note that C(pre) in Figure 11 corresponds to -C(-1) in the 802.3ap-2007 Standard (Section 72.7.1.10).

Post2-Cursor Emphasis

Post2-cursor emphasis is used to adjust the relative amplitude of the *second* bit in a string of consecutive identical digits. The amplitude for post2-cursor emphasis is controlled by a 4-bit word in MDIO register FTX_PRE_LVL (1.C309h[8:5]). The output signal amplitude is equal to Stepsize * C(post2) where C(post2) is a binary weighted value that is set by FTX_PRE_LVL.

Post2-cursor emphasis is used in SFP+ mode in Figure 11.

Considerations

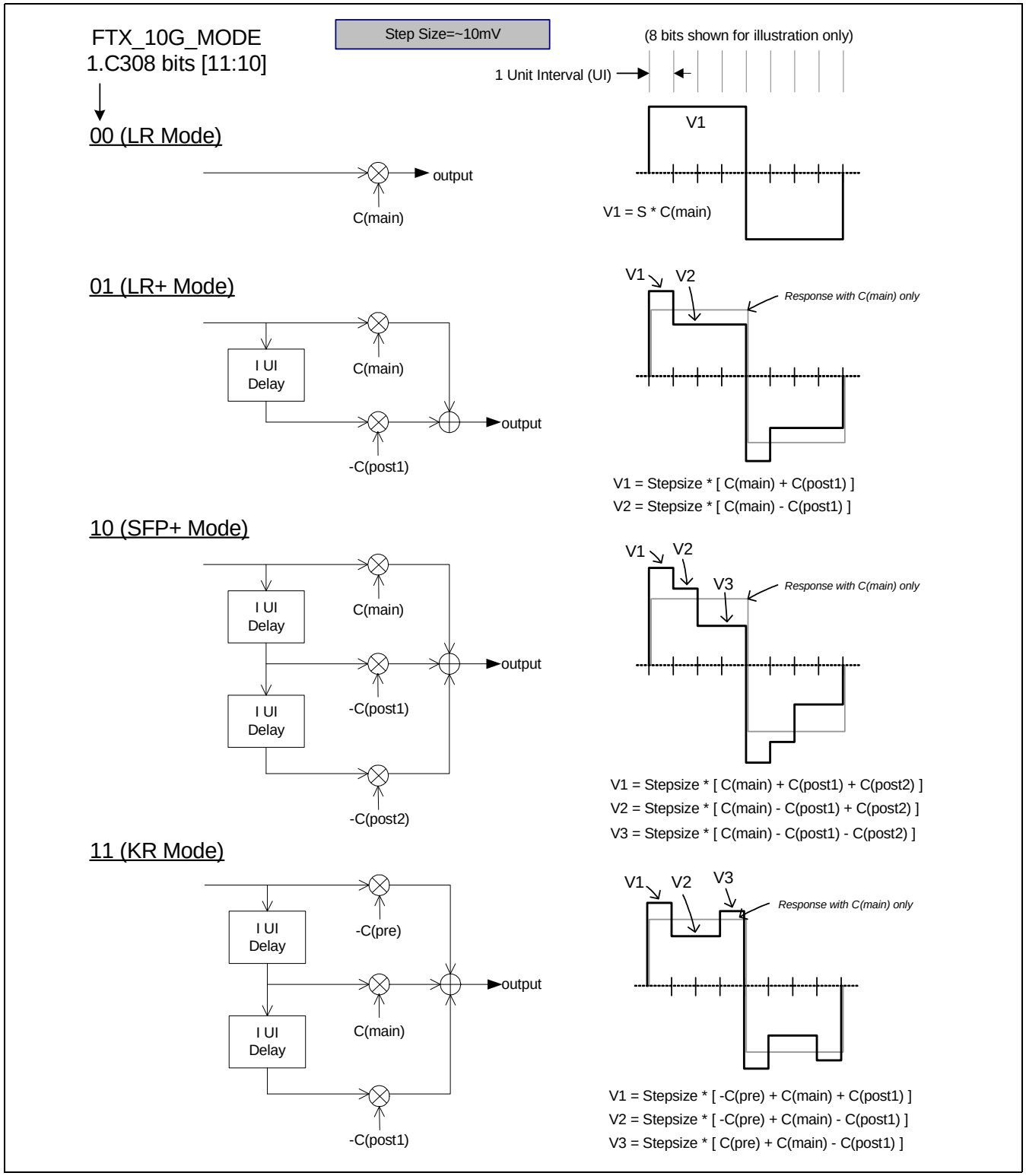
The total weight of all combined tap settings must sum to a value of 63 or less for proper operation. The main tap amplitude must be programmed to a positive voltage greater than 0V.

Post2-cursor and pre-cursor emphasis cannot be used simultaneously e.g. post2-cursor is available in SFP+ mode only, while the pre-cursor is available only in KR mode.

Table 4: 10Gbps Driver Configuration

Transmitter Mode Name	FTX_10G_MODE 1.C308h[11:10]	Pre-cursor	Main	Post1-cursor	Post2-cursor
LR	00		Y		
LR+	01		Y	Y	
KR	11	Y	Y	Y	
SFP+	10		Y	Y	Y

Figure 11: 10G Transmit Driver Modes, Block Diagrams, and Example Differential Waveforms



EDC Engine

The QT2025 includes a sophisticated Electronic Dispersion Compensation (EDC) engine to meet IEEE 802.3ap 10GBASE-KR requirements, IEEE 802.3aq 10GBASE-LRM requirements and SFP+ requirements. The EDC engine is automatic and will adapt in real-time to compensate for dispersion in the transport medium. No external control is required but manual modes are available. The EDC Engine is not used in 1Gbps mode.

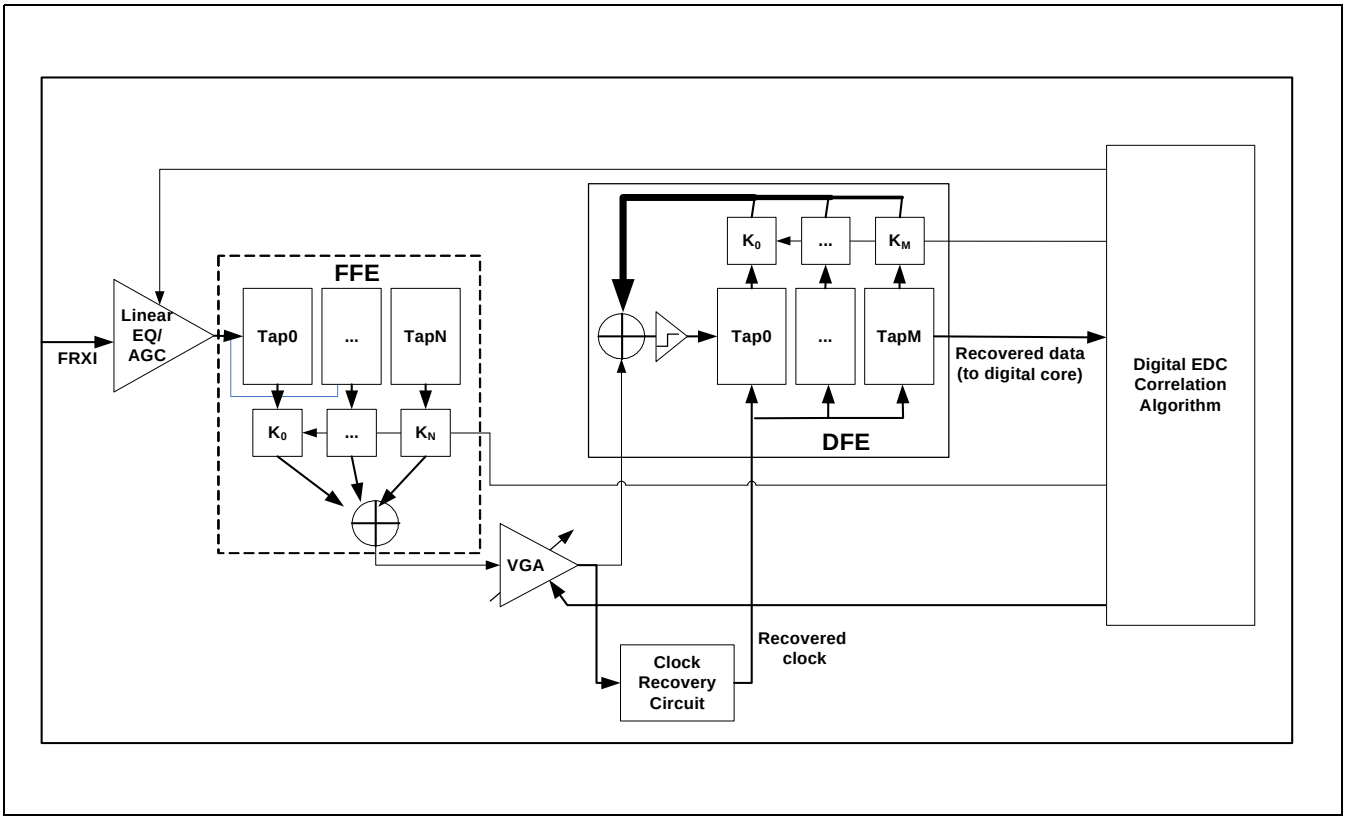
Unique features of the EDC engine include:

- Compensation in excess of the 10GBASE-LRM Standard, allowing reliable transmission over MMF fibers >220 meters in length with PIE-D exceeding 4.5dBm.
- High-performance, dynamic-tracking operation that offers instantaneous correction for dynamic response changes due to environmental factors (fiber vibration, thermal shifts, and other effects).
- Micro-controller software-based EDC algorithm allows for field upgrades and/or user added-value functionality.

Overview

The EDC equalizer employs a multi-tap Feed-Forward Equalizer (FFE) and Decision-Feedback Equalizer (DFE) architecture. The basic EDC block diagram is illustrated in Fig. 12 below. The following sections cover the blocks in more detail.

Figure 12: Data Path Block Diagram



Linear Equalizer

The input stage contains a linear equalizer. The linear equalizer provides an adaptable frequency gain profile to compensate for frequency-dependent loss. It provides a programmable amount of gain at a high frequency relative to a low frequency.

Automatic Gain Control

The input stage includes a variable gain stage (AGC) that allows the chip to accept a range of input amplitudes. The AGC controls the overall gain of the input stage such that the amplitude into the EDC block is set to a fixed amplitude that is optimized for EDC operation.

Adaptive Equalizer

The adaptive equalizer employs a multi-tap Feed Forward Equalizer (FFE) and a multi-tap Decision Feedback Equalizer (DFE) to correct signal impairments caused by the transmission channel response.

Feed-Forward Equalizer (FFE)[1]

The FFE block sends the data signal to multiple taps. Each tap adds a fixed amount of propagation delay relative to the previous tap, resulting in N equally spaced tap signals. Each tap output is adjusted by a tap weighting factor. The outputs are then summed to generate a combined signal.

VGA

The Variable Gain Amplifier (VGA) adjusts the FFE signal amplitude to provide an optimal signal level to the DFE.

Decision Feedback Equalizer (DFE)

The DFE block consists of a summing node, a data slicer, and multiple feedback tap paths. The summing node sums the input data with weighted values of previous data decisions. The slicer makes a digital decision on the resultant signal from the summer. The multiple taps are progressively delayed by a fixed amount.

EDC Correlation Algorithm

The FFE and DFE tap weights are controlled by an EDC Correlation Algorithm. This optimizes the tap weights by minimizing the correlation between data bits in the signal that cause ISI.

Equalization Control and Monitoring

The QT2025 provides a number of features for in-service or test-and-evaluation control and monitoring of the equalization functions.

All receiver optimization features can be monitored and controlled via the standard I2C and MDIO register interfaces. Upon device power up, default settings for the EDC algorithms are configured by the device firmware supplied by AMCC and generally will not need to be modified. Automatic update of these settings can be disabled and frozen and manual settings can be applied as desired. Refer to the register map for details.

1. The use of the FFE and DFE taps is controlled by firmware to optimize power and performance.

KR Interface

The QT2025 has fully 802.3ap compliant 10GBASE-KR receive and transmit interfaces. Clause 73 Auto-negotiation is supported on the backplane interface, allowing datarate negotiation between 10Gbps and 1Gbps with the link partner. 1000BASE-KX protocol is supported (but 10GBASE-KX4 is not supported). The product also supports Link Training and in-band FEC for 10Gbps channels.

10GBASE-KR Receiver

The 10BGASE-KR receiver uses the EDC engine described on Page 26. The VGA has sufficient gain and range to accommodate the supported signalling levels at the FRXIN/P inputs for backplane applications.

KR Transmitter

The KR transmitter contains a 3-tap FIR driver. The driver is fully described in “10Gbps Interface” on page 23 The driver is capable of variable pre-cursor and post-cursor emphasis based on the tap coefficients provided to it by the KR training algorithm. The driver is capable of driving both +ve and -ve FIR tap coefficients. The dynamic range of V1 (pre-cursor level), V2 (steady state level) and V3 (post-cursor level) exceed that required by IEEE 802.3ap Sub-clause 72.7.1.10.

The transmitter tap settings are automatically optimized for the backplane channel by the IEEE 802.3 Clause 72 Link Training protocol, described on Page 34. The tap coefficients can be manually overridden if desired through the MDIO interface.

Auto-Negotiation

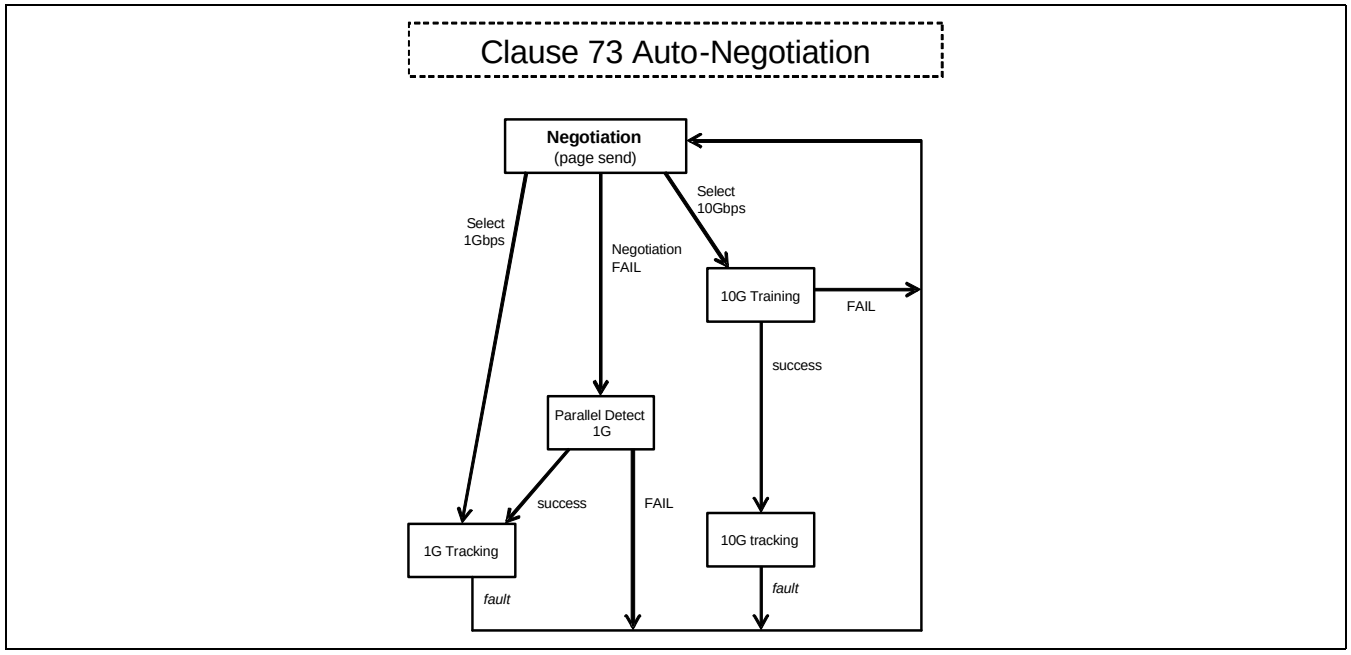
Auto-Negotiation (AN) is defined in Clause 73 of IEEE 802.3ap. This function allows this device to advertise modes of operation to another device at the remote end of an ethernet link across a backplane and to detect corresponding operational modes the other device may be advertising.

The device will select a mode of operation based on the operating mode agreed upon with the link partner during Arbitration. This will always be the highest protocol level advertised by both link partners. Any additional features or modes supported by both link partners will also be enabled.

A simplified Auto-negotiation flow chart is shown in Figure 13 on page 29. The operating mode is determined in the Negotiation phase. If the negotiation is successful at finding a common supported operating mode, the chip will send traffic at 1Gbps or attempt link training at 10Gbps (based on the negotiation outcome). If the negotiation is unsuccessful the chip will attempt parallel detection at 1Gbps on the serial input.

Once a successful link is established, the chip will stay in the tracking state (either 1G or 10G). The chip will re-enter the Negotiation phase when a major fault is detected e.g. lose link partner.

Figure 13: Simplified Auto-Negotiation State Diagram



MDIO Access

All Auto-negotiation functions are accessed through MDIO registers in logical device 7.

Auto-Negotiation Pages

The Auto-Negotiation messaging is transmitted within a differential Manchester encoded (DME) page. The differential Manchester encoding ensures a high transition density.

A DME page consists of a page delimiter field, a 48-bit Link Codeword field and a single bit from a pseudo-random sequence.

Manchester Violation Delimiter

The page delimiter field is called a Manchester violation (MV) delimiter and marks the start of each DME page. The MV delimiter is 8 bit positions long with a transition in position 1 and 5 only.

Link Codeword

The 48-bit Link Codeword field is used to communicate with the link partner and negotiate the supported protocol. Each bit is DME encoded.

DME Page Bit 49 Randomizer

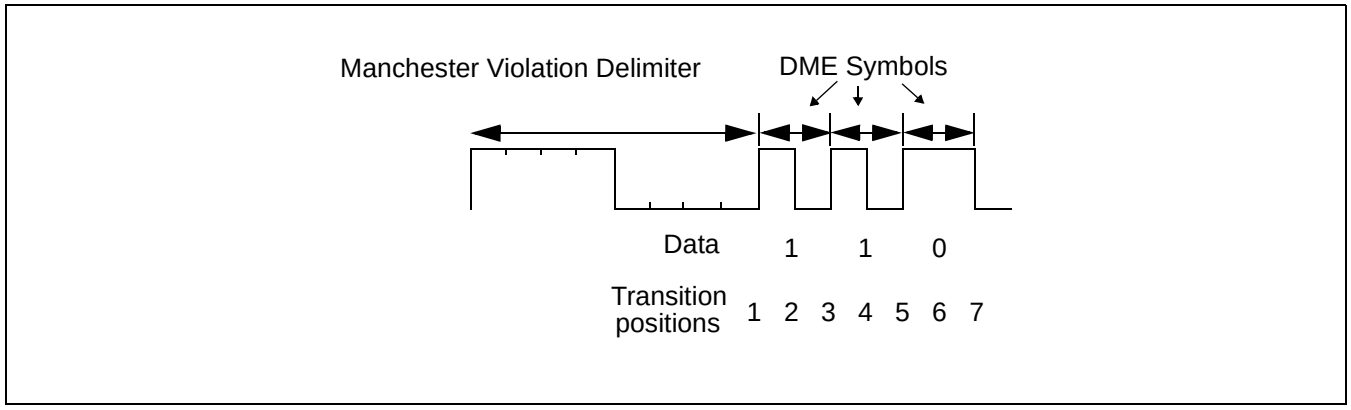
The 49th bit to be transmitted is DME encoded and is generated by a pseudo-random number generator defined by the polynomial $g(x) = x^7 + x^3 + 1$ implemented using a linear feedback shift register (LFSR). The purpose of the 49th bit is to remove spectral peaks that may otherwise occur when sending the same page repeatedly. This randomly inverts or uninverts the DME page encoding so the repeated signal is no longer periodic. The reset seed value of the polynomial is all 1's. The LFSR advances by 1 cycle for each page transmitted.

The MV delimiter and data encoding are shown in Figure 14.

Clocking

The period between transitions is 3.2ns. One DME symbol is therefore 6.4ns long and the MV delimiter is 4 symbols long. One DME page consists of 53 symbols and is therefore 339.2ns long.

Figure 14: MV Delimiter and DME Encoding Format



Link Codeword Format

The base Link Codeword transmitted within a DME page has the format shown in Figure 15, called the Base Page. Bit D0 is transmitted first.

The contents of the AN Base Page can be generally be modified in Registers 7.16-7.18 within the limitations of the chip.

Next Pages are also supported, which have a similar structure to the Base Page with different field definitions.

Selector Field

The Selector Field advertises the IEEE Auto-negotiation standard that is supported by the product. The encoding is shown in Figure 16. The value is fixed.

Figure 15: Link Codeword Base Page Format

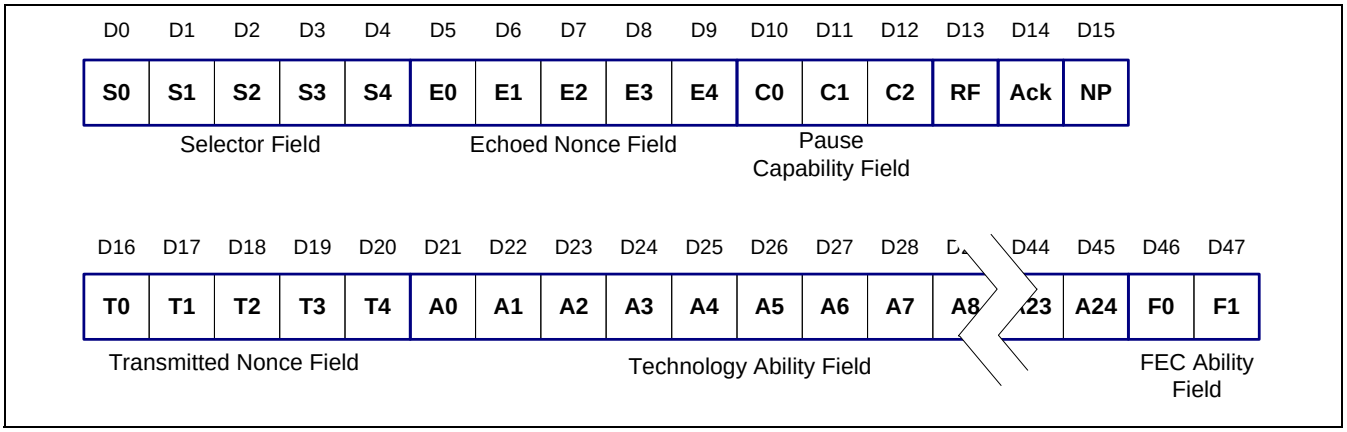


Figure 16: Selector Field Encoding

S4	S3	S2	S1	S0	Selector Description
0	0	0	0	1	IEEE 802.3 compliant

Echoed Nonce Field

The Echoed Nonce Field E[4:0] is a 5-bit field that contains the nonce code received from the link partner (in the Transmitted Nonce field). When the Ack is ‘0’, the Echoed Nonce field contains all 0s. When Ack is ‘1’, it contains the nonce code received from the link partner.

Transmitted Nonce Field

The Transmitted Nonce Field T[4:0] contains a randomly generated value in the range 00000 - 11111. A different nonce code is generated each time link arbitration starts. The nonce values are randomly generated with a uniform distribution.

Pause Ability Field

The Pause Ability Field advertises that the PAUSE function is supported (in C0) and the Asymmetric PAUSE is supported (in C1). Both functions are supported. The advertisement can be modified by changing the value in the appropriate MDIO register.

Technology Ability Field

The Technology Ability field advertises that the product supports 1000BASE-KX and 1GBASE-KR. The encoding is shown in Figure . The value is fixed.

FEC Capability Field

By default, the FEC Capability field (F[0:1]) advertises that the product supports FEC and is requesting FEC to be enabled on the link by default. The advertised values can be modified in the AN Base Page Registers 7.16-7.18.

Figure 17: Technology Ability Field Encoding

Bit	Value	Technology
A0	1	1000BASE-KX supported
A1	0	10GBASE-KX4 not supported
A2	1	10GBASE-KR supported
A3..A24	0	RESERVED

Figure 18: FEC Capability Field Encoding

Bit	Default	Description
F0	1	Device is FEC Capable
F1	0	Device is requesting FEC

Remote Fault (RF) Bit

The Remote Fault bit is used to indicate to the Link Partner that a fault condition has been detected.

Acknowledge (Ack) Bit

The Acknowledge bit indicates that the Link Partner's Link Codeword Base Page was successfully received. The bit is set to '1' after the reception of 3 or more consecutive and consistent DME pages. If Next Page information is to be sent, this bit is set to '1' after the reception of 3 or more consecutive and matching DME pages.

Next Page (NP) Bit

The Next Page bit advertises whether there are any Next Pages to transmit. The value is '0' if there are no Next Pages to send and '1' if there are. If the device has no Next Pages to send but the Link Partner has the NP bit set to '1', the device will send Next Pages with Null messages and the NP bit set to '0' while its Link Partner transmits valid Next Pages.

Arbitration Function

The arbitration function governs the Auto-Negotiation process. It allows the chip to advertise and acknowledge abilities with the link partner. It also determines the highest common denominator (HCD) abilities between the link partners in order to choose the link operating mode.

The Arbitration function is compliant to IEEE 802.3ap-2007 Figure 73-11.

Priority

The HCD ability is determined by the advertised ability that both link partners support with the highest priority. The priority is determined by Table . If 10GBASE-KR is selected, FEC will be enabled on the link based on the advertised values in the FEC Capability field.

Table 5: Priority for Supported Technology

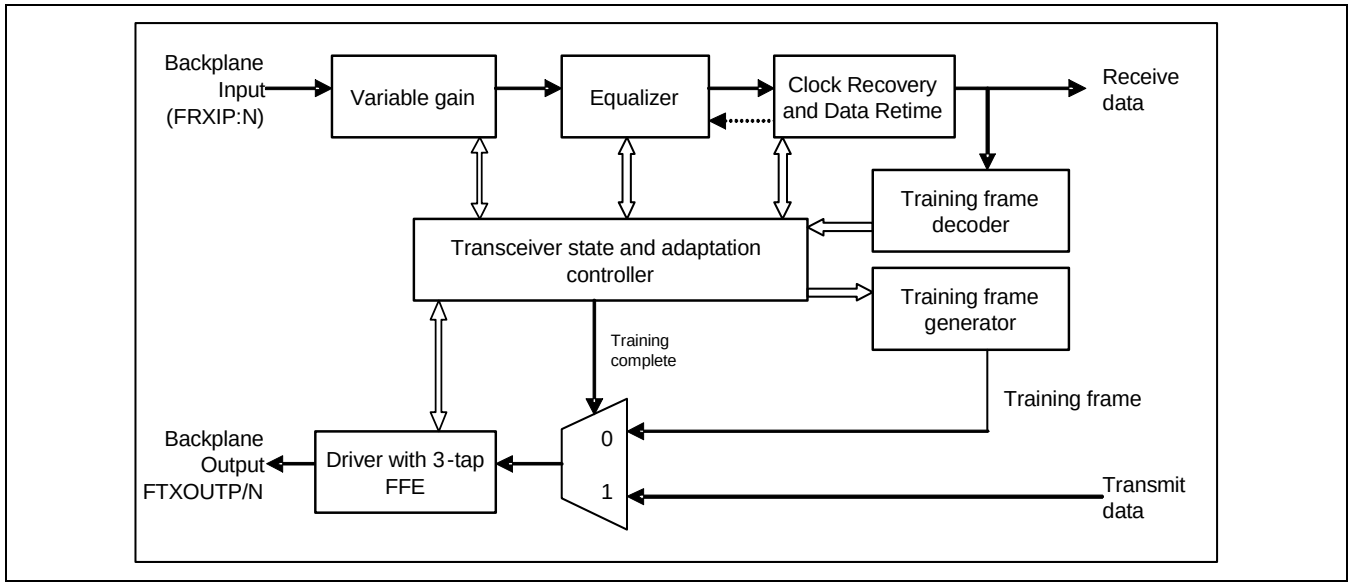
Priority	Technology	Supported
1	10GBASE-KR	YES
2	10GBASE-KX4	NO
3	1000BASE-KX	YES

Clause 72 Link Training

The sole purpose of the link training sequence is to “train” the interface for the particular backplane communication channel. The training sequence starts after system power-up/reset and will restart after a major fault to the KR link (e.g. link partner is unplugged). Once the sequence is completed, optimized transmitter FIR and receiver equalizer tap coefficients are established. The system then switches to tracking mode during which no further transmitter optimization will occur. The transmitter FIR tap coefficients are fixed in tracking mode. The receiver equalizer tap coefficients will continue to dynamically adjust to accommodate changes in the channel.

The training sequence comprises the transmission and reception of 802.3ap compliant training frames. These frames are sent continuously until the training sequence has completed. Embodied within these frames are a 4 byte frame marker, a 32 byte DME (Differential Manchester Encoded) control channel and a 512 byte training sequence as shown in Fig. 21.

Figure 19:KR Training Block Diagram



Framing Marker

The framing marker denotes the start of each training frame. It consists of a unique, fixed pattern of the format 0xFFFF0000.

DME Control Channel

The 32 byte DME control channel comprises a 16 bit co-efficient update field and a 16 bit status report field, compliant to 802.3ap Clause 72.6.10.2.2. The effective baud rate is 1.289Gbps (1/8th of 10.3125Gbps), such that the channel content can be reliably recovered over unequalized channels. The purpose of the channel is to direct the convergence of the link to a low BER solution by optimizing transmitter tap settings. Table 6 & Table 7 detail the contents of the control channel.

Link Training Sequence

The link training sequence is a 512 byte field comprised of 2 sequences of PRBS11 pattern followed by a pair of zeros. The training sequence is used to test the link quality for a given set of driver coefficients. During this period the algorithms within the QT2025 determine the link quality by accumulating errors and calculating the BER. Based on the outcome, the algorithm determines the next set of transmitter FIR tap coefficients for the remote driver and communicates this information via the control channel.

Figure 20: PRBS11 Pattern Generator

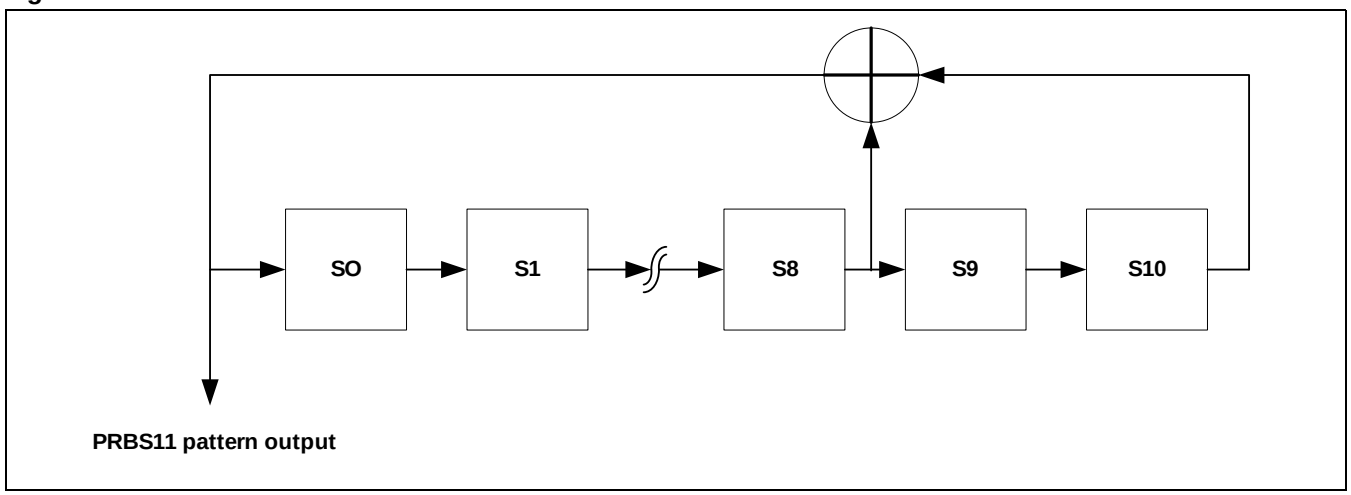


Figure 21: KR Training Frame

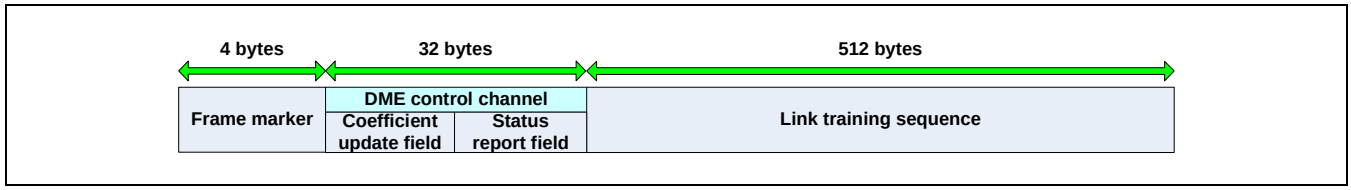


Table 6: Coefficient Update Field

Cell(s)	Name	Description
15:14	Reserved	Transmitted as 0, ignored on reception
13	Preset	1 = Preset coefficients 0 = Normal operation
12	Initialize	1 = Initialize coefficients 0 = Normal operation
11:6	Reserved	Transmitted as 0, ignored on reception
5:4	Coefficient C(+1) update	[5:4] 11 = reserved 01 = increment 10 = decrement 00 = hold
3:2	Coefficient C(0) update	[3:2] 11 = reserved 01 = increment 10 = decrement 00 = hold
1:0	Coefficient C(-1) update	[1:0] 11 = reserved 01 = increment 10 = decrement 00 = hold

Table 7: Status Report Field

Cell(s)	Name	Description
15	Receiver ready	
14:6	Reserved	Transmitted as 0, ignored on reception
5:4	Coefficient C(+1) update	[5:4] 11 = maximum 01 = minimum 10 = updated 00 = not_updated
3:2	Coefficient C(0) update	[3:2] 11 = maximum 01 = minimum 10 = updated 00 = not_updated
1:0	Coefficient C(-1) update	[1:0] 11 = maximum 01 = minimum 10 = updated 00 = not_updated

10GBASE-KR Link Control Algorithms

The link control algorithms are responsible for encoding and decoding the training frames. Figure 22 & Figure 23 depict the link training frame encoding and decoding procedure.

Figure 22: 10GBASE-KR Link Training Encoder

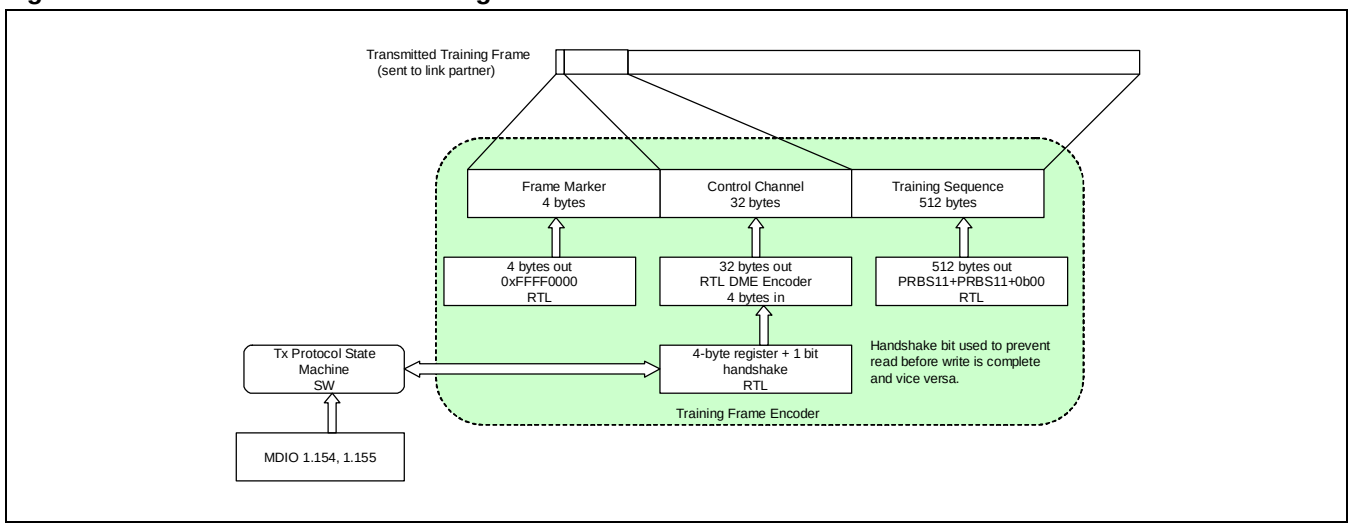
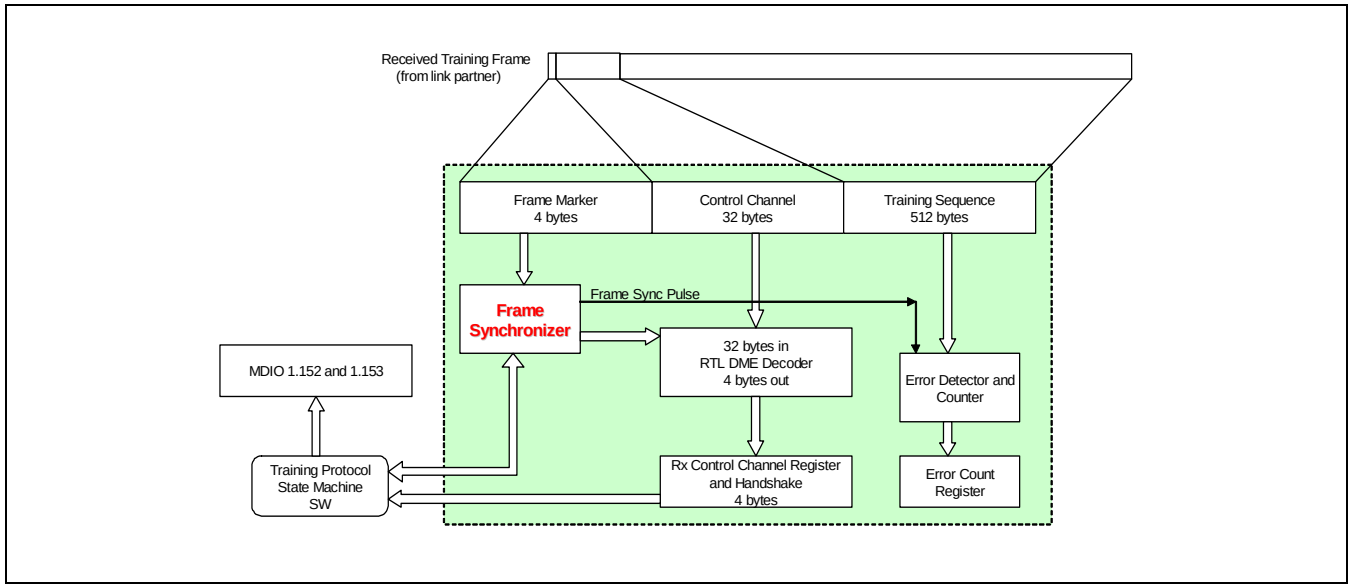


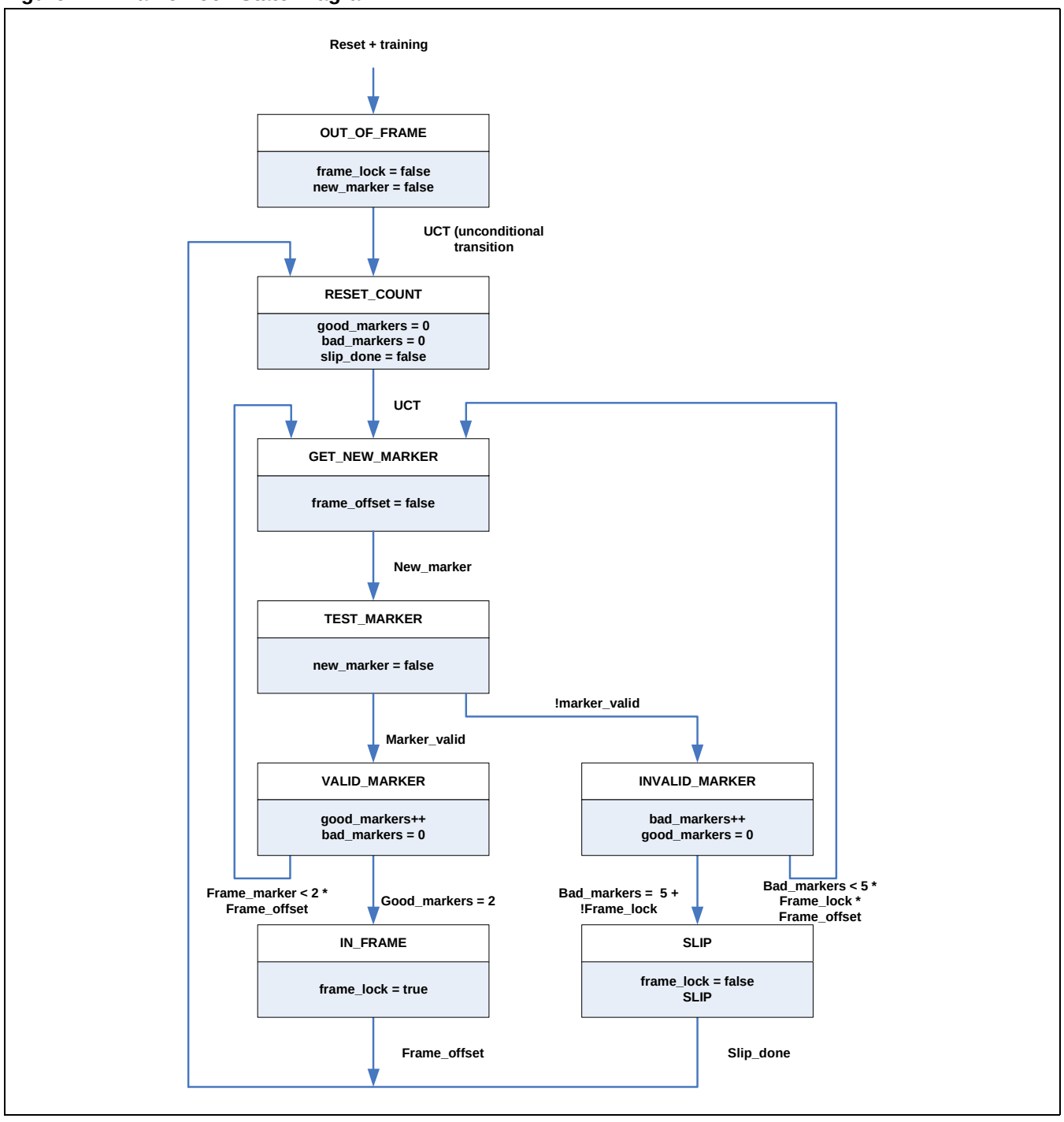
Figure 23: 10GBASE-KR Link Training Decoder



KR Frame Lock State Machine

The frame lock state machine in Figure 24 represents the Frame Synchronizer function highlighted above in Figure 23. Before the contents of the control channel can be extracted and processed, the receiver must perform a frame align, keying in on the unique marker pattern 0xFFFF0000.

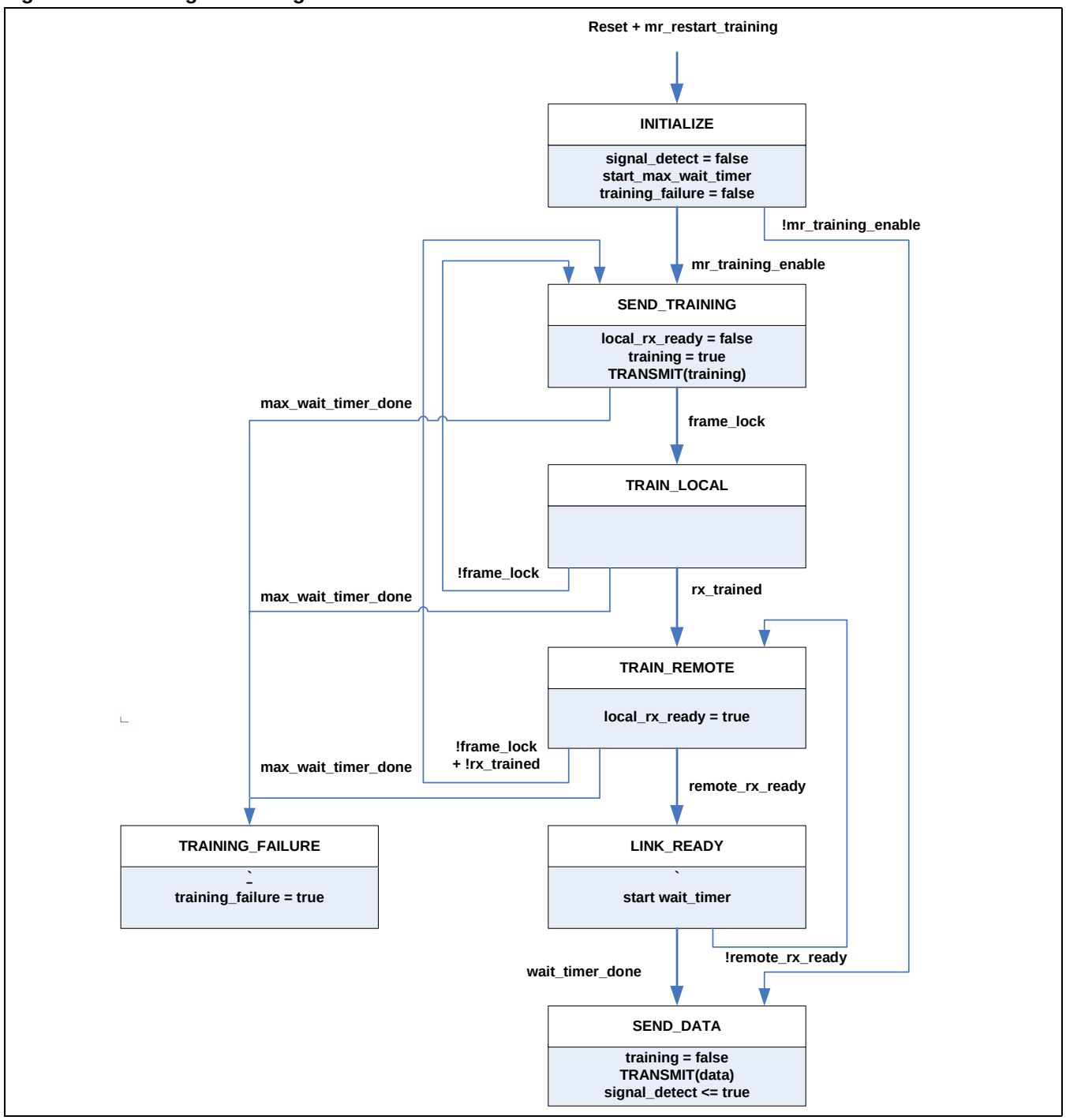
Figure 24: Frame Lock State Diagram



KR Training State Machine

The training state machine (Figure 25) is responsible for initiating and managing both the remote and local training sequences. The training sequence will continue until both link partners report that they have completed training.

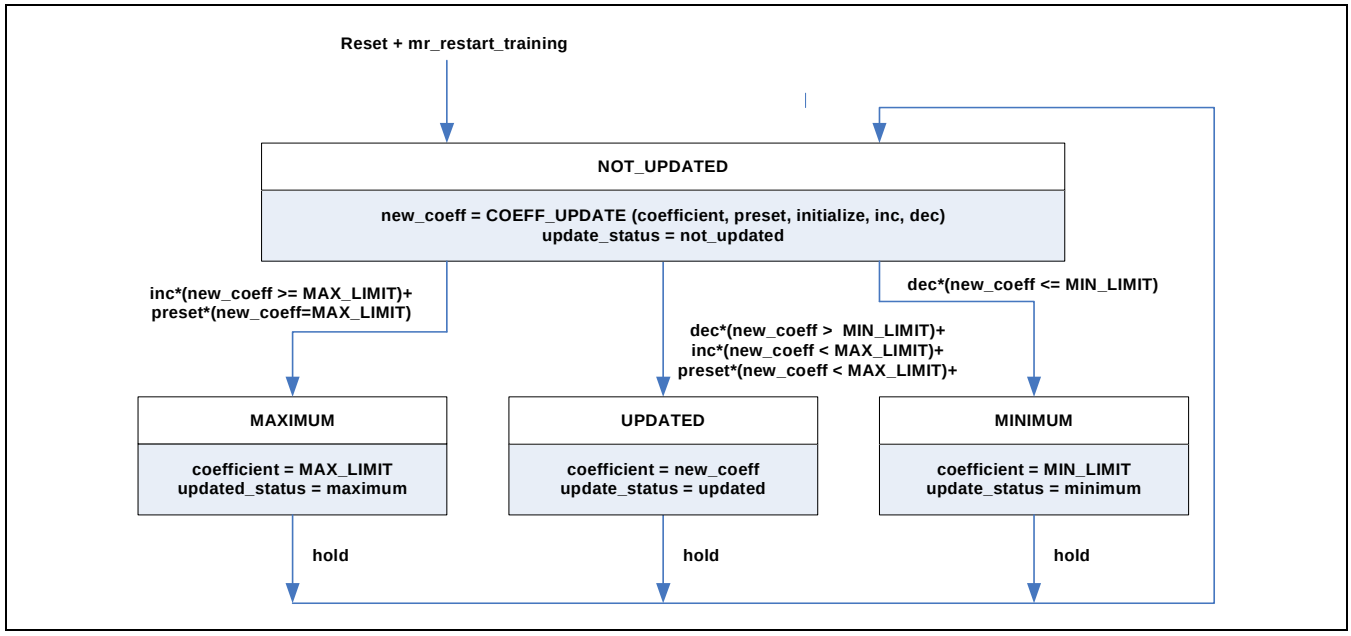
Figure 25: Training State Diagram



KR Coefficient Update State Diagram

Figure 26 illustrates the coefficient update state diagram. The state machine extracts the pertinent fields from the DME control channel and tests the value of the update command against the coefficient limits. Details of the states and state variables for all of the above state machines can be found in the IEEE 802.3ap Standard Sub-clause 72 “Physical Medium Dependant Sublayer and Baseband Medium, Type 10GBASE-KR”.

Figure 26: Coefficient Update State Diagram



FEC Encoding/Decoding

The QT2025 implements an optional FEC (Forward Error Correction) sublayer for 10GBASE-R applications to improve link performance. The chip uses an in-band FEC encoding that does not consume additional bandwidth, and so is compatible with currently supported PMD devices. It is optimized to handle short bursts of errors in the signal. The implementation is compliant to the IEEE 802.3ap Standard and specifically intended for 10GBASE-KR applications.

The FEC sublayer is disabled by default and is controlled by MDIO register fields. The FEC is not compatible with WIS mode (10GBASE-W) or rates below 10Gbps.

Overview

The FEC sublayer acts on the scrambled 66b encoded data blocks from the PCS layer. The algorithm encodes FEC information across a group of 32 data blocks, forming a FEC frame that is 66 x 32 = 2112 bits long. In the encoding process, each block is shortened from 66 bits to 65 bits by reducing the sync header field from 2 bits to 1. A 32-bit parity-check field is calculated across the FEC frame and then added to the frame end. The frame is then scrambled and transmitted.

When a FEC-encoded signal is received on the input, the signal is first unscrambled. The parity-check field is used to correct any correctable bit errors. The corrected 65b data is then converted to 66b and forwarded to the PCS.

The FEC sublayer also supports optional error injection to enhance testing capabilities.

The remainder of this chapter describes the FEC Transmit (Encoding) and Receive (Decoding) functions in detail.

Properties

- In-band FEC, operates at standard line rate by reducing the 2-bit 64/66 encoded sync header field by 1 to create a 32-bit parity check field for each 32 64/66 encoded blocks
- Operates on 66b encoded data at 10Gbps (10GBASE-R)
- Can correct a single burst of errors per FEC block, maximum 11 bits in size. (Errors must be spaced no more than 11 bit locations apart within the FEC block.)
- If errors are spaced by more than 11 bits apart within the FEC block, the algorithm is unable to correct them. No errors will be corrected in this instance.
- Can correct errors within the FEC Parity Field
- Optional error injection capability. Error injection available when FEC encoding disabled.

FEC Transmit Encoder

The FEC Transmit Encoder engine consists of a Transcoder, Encoder and Scrambler. An Error Injector is also available. The following sections review these blocks in detail.

Transcoder

The Transcoder is the first stage of the FEC TX block. The Transcoder strips the most significant bit of the SYNC field, with the least significant bit becoming the Transcode bit. This bit is then XOR'd with DATA[55] (the most significant bit of the 2nd data byte) to correct DC offset. The result is the output Transcode bit, T = SYNC[0] XOR DATA[55].

To better visualize the data mapping, see Table 8 below that shows the input to output data mapping.

Figure 27: FEC Transmit Block Diagram

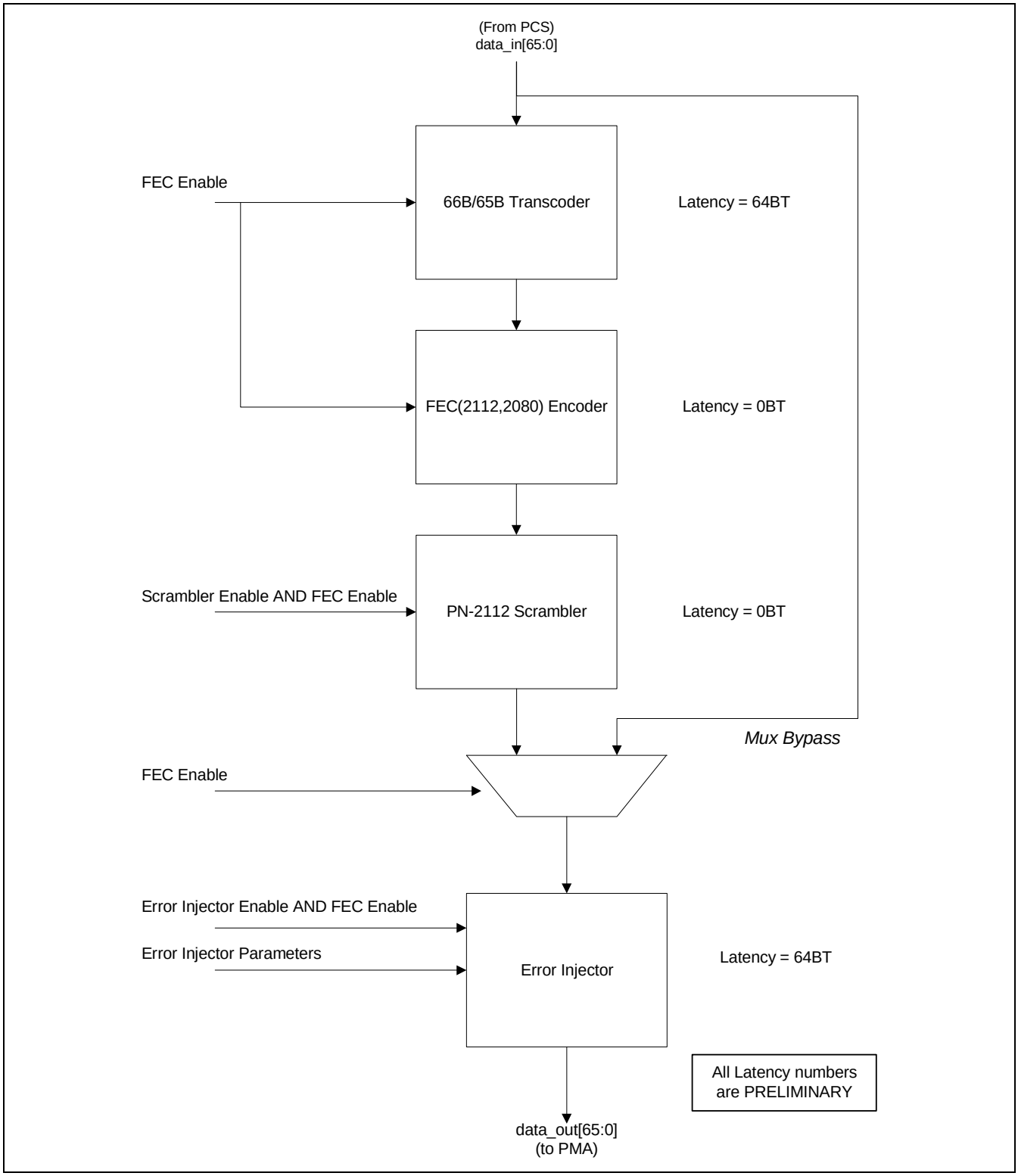


Table 8: Transcoder Data Re-mapping

fec_enc_cnt	Transcoder Input	Transcoder Output
0	$SYNC_0$[1:0],$DATA_0$[63:0]	PREVIOUS BLOCK
1	$SYNC_1$[1:0],$DATA_1$[63:0]	T_0,$DATA_0$[63:0],T_1
2	$SYNC_2$[1:0],$DATA_2$[63:0]	$DATA_1$[63:0],T_2,$DATA_2$[63]
3	$SYNC_3$[1:0],$DATA_3$[63:0]	$DATA_2$[62:0],T_3,$DATA_3$[63:62]
4	$SYNC_4$[1:0],$DATA_4$[63:0]	$DATA_3$[61:0],T_4,$DATA_4$[63:61]
5	$SYNC_5$[1:0],$DATA_5$[63:0]	$DATA_4$[60:0],T_5,$DATA_5$[63:60]
6	$SYNC_6$[1:0],$DATA_6$[63:0]	$DATA_5$[59:0],T_6,$DATA_6$[63:59]
7	$SYNC_7$[1:0],$DATA_7$[63:0]	$DATA_6$[58:0],T_7,$DATA_7$[63:58]
8	$SYNC_8$[1:0],$DATA_8$[63:0]	$DATA_7$[57:0],T_8,$DATA_8$[63:57]
9	$SYNC_9$[1:0],$DATA_9$[63:0]	$DATA_8$[56:0],T_9,$DATA_9$[63:56]
10	$SYNC_{10}$[1:0],$DATA_{10}$[63:0]	$DATA_9$[55:0],T_{10},$DATA_{10}$[63:55]
11	$SYNC_{11}$[1:0],$DATA_{11}$[63:0]	$DATA_{10}$[54:0],T_{11},$DATA_{11}$[63:54]
12	$SYNC_{12}$[1:0],$DATA_{12}$[63:0]	$DATA_{11}$[53:0],T_{12},$DATA_{12}$[63:53]
13	$SYNC_{13}$[1:0],$DATA_{13}$[63:0]	$DATA_{12}$[52:0],T_{13},$DATA_{13}$[63:52]
14	$SYNC_{14}$[1:0],$DATA_{14}$[63:0]	$DATA_{13}$[51:0],T_{14},$DATA_{14}$[63:51]
15	$SYNC_{15}$[1:0],$DATA_{15}$[63:0]	$DATA_{14}$[50:0],T_{15},$DATA_{15}$[63:50]
16	$SYNC_{16}$[1:0],$DATA_{16}$[63:0]	$DATA_{15}$[49:0],T_{16},$DATA_{16}$[63:49]
17	$SYNC_{17}$[1:0],$DATA_{17}$[63:0]	$DATA_{16}$[48:0],T_{17},$DATA_{17}$[63:48]
18	$SYNC_{18}$[1:0],$DATA_{18}$[63:0]	$DATA_{17}$[47:0],T_{18},$DATA_{18}$[63:47]
19	$SYNC_{19}$[1:0],$DATA_{19}$[63:0]	$DATA_{18}$[46:0],T_{19},$DATA_{19}$[63:46]
20	$SYNC_{20}$[1:0],$DATA_{20}$[63:0]	$DATA_{19}$[45:0],T_{20},$DATA_{20}$[63:45]
21	$SYNC_{21}$[1:0],$DATA_{21}$[63:0]	$DATA_{20}$[44:0],T_{21},$DATA_{21}$[63:44]
22	$SYNC_{22}$[1:0],$DATA_{22}$[63:0]	$DATA_{21}$[43:0],T_{22},$DATA_{22}$[63:43]
23	$SYNC_{23}$[1:0],$DATA_{23}$[63:0]	$DATA_{22}$[42:0],T_{23},$DATA_{23}$[63:42]
24	$SYNC_{24}$[1:0],$DATA_{24}$[63:0]	$DATA_{23}$[41:0],T_{24},$DATA_{24}$[63:41]
25	$SYNC_{25}$[1:0],$DATA_{25}$[63:0]	$DATA_{24}$[40:0],T_{25},$DATA_{25}$[63:40]
26	$SYNC_{26}$[1:0],$DATA_{26}$[63:0]	$DATA_{25}$[39:0],T_{26},$DATA_{26}$[63:39]
27	$SYNC_{27}$[1:0],$DATA_{27}$[63:0]	$DATA_{26}$[38:0],T_{27},$DATA_{27}$[63:38]
28	$SYNC_{28}$[1:0],$DATA_{28}$[63:0]	$DATA_{27}$[37:0],T_{28},$DATA_{28}$[63:37]
29	$SYNC_{29}$[1:0],$DATA_{29}$[63:0]	$DATA_{28}$[36:0],T_{29},$DATA_{29}$[63:36]
30	$SYNC_{30}$[1:0],$DATA_{30}$[63:0]	$DATA_{29}$[35:0],T_{30},$DATA_{30}$[63:35]
31	$SYNC_{31}$[1:0],$DATA_{31}$[63:0]	$DATA_{30}$[34:0],T_{31},$DATA_{31}$[63:34]
0	NEXT BLOCK	$DATA_{31}$[33:0],32'd0

FEC(2112,2080) Encoder

The encoder block generates the 32-bit long FEC parity field for each FEC frame. The parity field contains information about the data pattern in the frame. It is used in the receiver to identify and correct errored bits.

The Encoder implements a shortened cyclic code with generator polynomial:

$g(x) = x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$

The parity is represented by: $p(x) = x^{32}m(x) \bmod g(x)$

Thus, the codeword c(x) is given by: $c(x) = x^{32}m(x) + p(x)$

A FEC Block is defined as the 2112 bits that ends with the 32 bit FEC parity field.

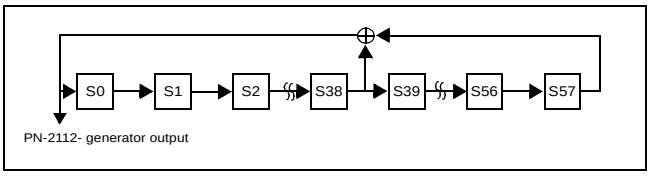
PN-2112 Scrambler

The FEC Transmit employs a synchronous PN-2112 Scrambler given by $r(x) = 1 + x^{39} + x^{58}$. The seed value for the Scrambler, referred to as S[57:0], is 0x2AA_AAAA_AAAA_AAAA.

The output of the Scrambler is XOR'd with the output of the Encoder. The Scrambler seed is reset at the beginning of every FEC block.

This method prevents errors from propagating through the scrambler polynomial and between FEC frames. The Scrambler adds no latency to the FEC Transmit block.

Figure 28: PN-2112 Scrambler



Bypass Mux

The bypass mux is used to disable the FEC encoding. The associated FEC_EN register bit allows the FEC encoder to be bypassed and data will be routed from the PCS when it is inactive.

Error Injector

The Error Injector is after the Scrambler in the data path and is not bypassed when FEC encoding is disabled. This allows for error injection to be performed with FEC on and off for comparative analysis.

The FEC(2112,2080) code is designed to correct a burst of up to 11 bit errors within a single FEC block. The Error Injector will use the contents of FEC_ERR_MASK[31:0] register location as an error mask to be injected at an interval set in the FEC_ERR_PERIOD[31:0] register. Each increment of FEC_ERR_PERIOD[31:0] register represents 64BT. Setting FEC_ERR_PERIOD[31:0] to 0 will cause the FEC_ERR_MASK[31:0] bits to be XOR'd into the data continuously. Setting FEC_ERR_PERIOD[31:0] bits to any value between 1 and 32'hFFFF_FFFF will create an error-free interval of that length between insertions of FEC_ERR_MASK[31:0] bits.

The Error Injector adds 64BT of latency to the data path.

Clocks and Resets

There is only one clock (clk) and one reset (rstb) input to the FEC Transmit block.

When the FEC algorithm is not in use, the associated TX_KR_FEC_RESETN and TX_KR_CK_EN register bits should be set to 0.

To enable the FEC,

Set TX_KR_CK_EN to 1

Set TX_KR_FEC_RESETN to 1

Set KR_FEC_EN = 1

FEC Receive

The FEC Receiver Engine consists of a De-Scrambler, Block Synchronizer, Decoder and Reconstructor, along with an Error Monitor. These blocks are described in detail in the following sections.

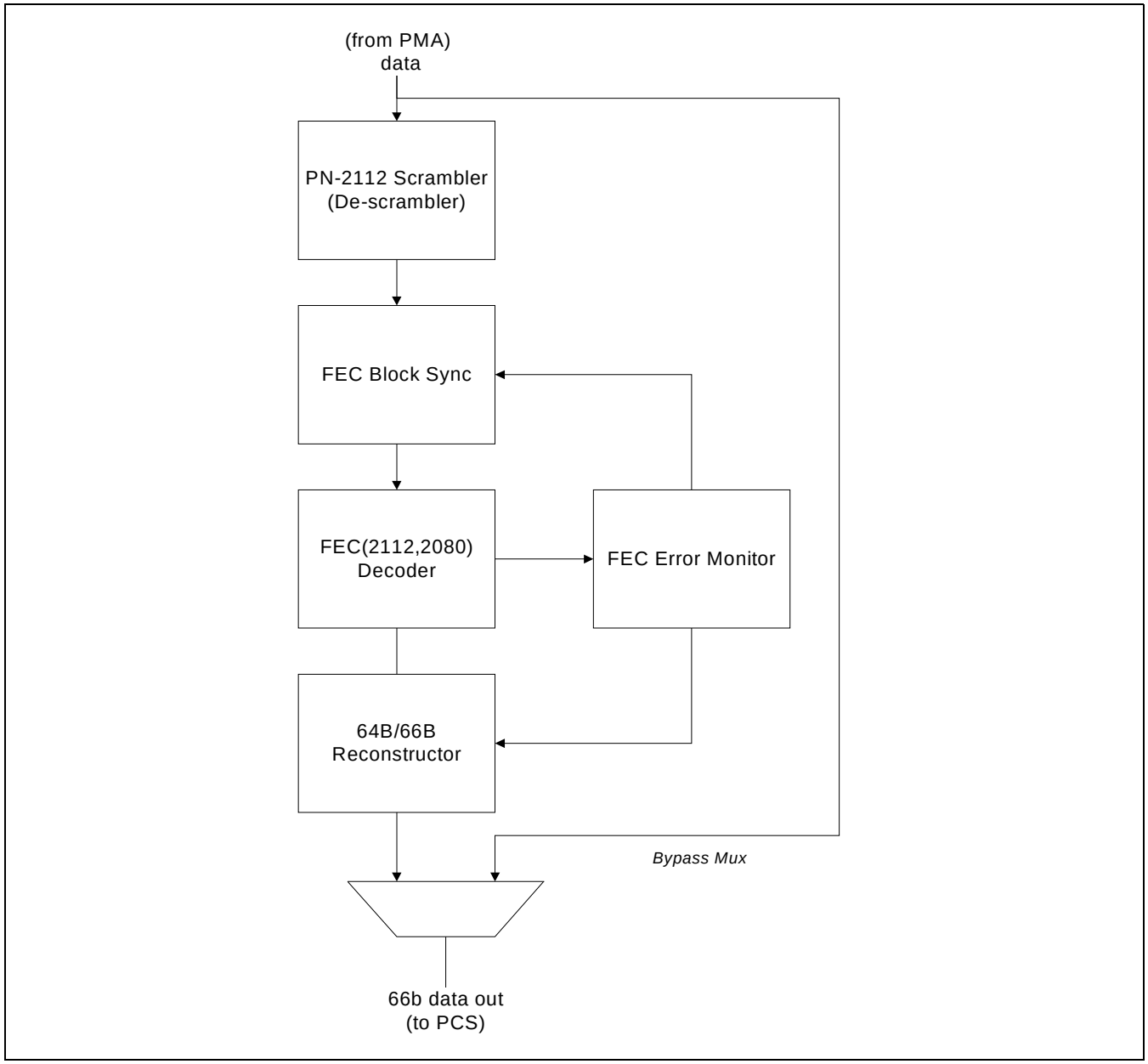
The FEC Receive block can be bypassed with 0 latency by setting the associated FEC enable register bit to FEC_EN = 0. This datapath will work while FEC_CLK_EN = 0 or FEC_CLK_EN = 1.

PN-2112 Scrambler

The PN-2112 Scrambler is used as a de-scrambler in the FEC Receive block. See PN-2112 Scrambler description on Page 44.

The Scrambler has 0BT latency.

Figure 29: FEC Receive Block Diagram



FEC Block Synchronizer

The FEC Block Synchronizer aligns the incoming data to one of 2112 possible FEC block alignments based on feedback from the FEC Error Monitoring block. For a given alignment, the FEC Error Monitoring block calculates the parity for the FEC block. An unerrored block is a block whose calculated parity matches its received parity.

M consecutive unerrored blocks in the same alignment cause the FEC Block Sync to assert fec_signal_ok to the PCS. N consecutive uncorrectable blocks in the same alignment cause the FEC Block Synchronizer to de-assert fec_signal_ok to the PCS. The FEC Block Synchronizer will adjust the bit alignment by 1 bit position when a SLIP command is issued by the Synchronization Finite State Machine (FSM) if fec_signal_ok is de-asserted.

If, during the synchronization process, bit errors occur when the correct alignment is checked, the algorithm will increment the bit position. The alignment process will cycle through all 2112 bit positions until it returns to the correct alignment.

M = 8 and N = 4 are constants in the IEEE 802.3ap, but they are configurable in the AMCC implementation. FEC_M[3:0] defaults to 8 and FEC_N[3:0] defaults to 4.

Receive FEC block synchronization is achieved using conventional n/m serial locking techniques as described below.

FEC(2112,2080) Decoder

The FEC(2112,2080) is a shortened cyclic code with generator polynomial, g(x) of:

Equation 1. $g(x) = x^{32} + x^{23} + x^{21} + x^{11} + x^{2} + 1$

While the syndrome is calculated the received polynomial is buffered in 2112 bit FEC Data Buffer

FEC Data Buffer

The Data Buffer is implemented with a 34x64 bit 2-Port SRAM.

FEC Error Monitor

Required Performance Monitoring

FEC_CORR_BLK_CNT[31:0] is incremented by 1 for each FEC Block that is received with incorrect parity but was corrected by the FEC Decoder.

FEC_UNCORR_BLK_CNT[31:0] is incremented by 1 for each FEC Block that is received with incorrect parity but was not corrected by the FEC Decoder.

65B/66B Reconstructor

The 65B symbols of the FEC Block need to be reconstructed to 66B symbols for the PCS. The Transcode bit is de-scrambled by XOR'ing it with the 9th data bit of the same 65B symbol. The de-scrambled bit is then repeated and inverted to recreate the 66B PCS symbol.

If FEC error reporting is enabled, the SYNC field is forced to 2'b11 in the a,b,c, and d words of the 32-word block.

FEC Bypass Mux

The FEC Bypass Mux is controlled by FEC_EN. When FEC_EN = 1, the Bypass Mux outputs the result of the 64B/66B Reconstructor. When FEC_EN = 0, the Bypass Mux passes the input of the FEC Receive block through to the output.

The Bypass Mux should continue to pass the input to the output regardless of the state of FEC_RX_RESET or FEC_CLK_EN.

Table 9: T to SYNC[1:0] Reconstruction for FEC Block of i=1 to 32 words

T	Error reporting enable	Uncorrectable block	$SYNC_i$[1:0]
0	0	X	10 (i = 1 to 32)
1	0	X	01 (i = 1 to 32)

FEC MDIO Register Mapping

Required FEC Registers

FEC_ability is read-only and ‘1’ and generated in the register map.

FEC_Error_Indication_ability is read-only and ‘0’.

FEC_Enable is FEC_EN.

FEC_Enable_Error_to_PCS support is TBD.

FEC_corrected_blocks_counter is:

FEC_CORR_BLK_CNT.

FEC_uncorrected_blocks_counter is:

FEC_UNCORR_BLK_CNT

Implementation Specific FEC Registers

In addition to the required registers the following implementation-specific register fields are defined:

FEC_RX_RESET is 0 after chip reset. When FEC_RX_RESET is 1, all state registers in the FEC Receive block are held in reset. The hardware insures synchronous assertion and de-assertion of the reset signal by a dual-rank synchronizer. The FEC_RX_RESET must be asserted for at least 4 datapath clock cycle, which is 4 x 6.4 ns = 25.6 ns. The contents of the Data Buffer SRAM are unaffected by reset.

FEC_M[3:0] is 8 after reset. The legal range of FEC_M is from 1 to 15.

FEC_N[3:0] is 4 after reset. The legal range of FEC_N is from 1 to 15.

FEC_SYNC is read-only and 0 after reset. This read-only bit reports the state FEC Synchronization. When FEC_SYNC is 1, the FEC Decoder is synchronized. When FEC_SYNC is 0, the FEC Decoder is not synchronized.

Table 10: MDIO/FEC Variable Mapping

MDIO Variable	PMA/PMD Register Name	Register/BIt Number	FEC Variable
10GBASE-R FEC ability	10GBASE-R FEC ability register	1.0011h[0]	FEC_ability
10GBASE-R FEC Error Indication ability	10GBASE-R FEC ability register	1.00AAh[1]	FEC_Indication_ability
FEC Enable	10GBASE-R FEC control register	1.00ABh[0]	FEC_Enable
FEC Enable Error Indication	10GBASE-R FEC control register	1.00ABh[1]	FEC_Enable_Error_to_PCS
FEC corrected blocks	10GBASE-R FEC corrected blocks counter register	1.00ACh, 1.00ADh	FEC_corrected_blocks_counter
FEC uncorrected blocks	10GBASE-R FEC uncorrected blocks counter register	1.00AEh, 1.00AFh	FEC_uncorrected_blocks_counter

10GBASE-KR Considerations

The PMA System Loopback is not guaranteed to operate in 10GBASE-KR mode. If the loopback is enabled while the AN is enabled, it can trigger the AN state machine to re-negotiate. The PHY will not generally be able to complete the negotiation with the loopback enabled.

It is possible to override the AN state machine to prevent this from occurring. However, the PMA System Loopback may still not run error-free.

1GE Mode

Overview

Example applications of 1GbE mode are illustrated in Figure 30 and Figure 31. The board should be designed for simultaneous operation with a 10.5Gbps and 1.25Gbps signal. It is expected that the high-speed I/O design will exceed the requirements for highest I/O rate (~10.5Gbps).

On the fiber side, the optical signal is terminated by a 1000BASE-SX/LX compatible SFP module. The SFP module provides no retiming in either direction. The module receive output is voltage limited and AC coupled. The module transmit input is internally AC coupled and limited. The module connects to the QT2025 through a SFP+ compatible medium, which includes an SFP+ connector and differential stripline or microstrip circuit trace. For SFP module applications, the QT2025 SFP+ input and output specifications are based upon SFP MSA signal levels and 1000GBASE-SX/LX jitter. For backplane applications, the specifications are based upon 1000BASE-KX.

On the board side, the QT2025 connects with another device (e.g., MAC PHY) through a XAUI compatible medium. For 1GbE, the QT2025 XAUI input and output specifications are specified to suit the characteristics of connecting devices and jitter transfer characteristics of the QT2025.

Transmit Path

In the transmit (Tx) path, the 1.25 Gbps XAUI input signal on Lane 0 is detected and retimed by a clock and data recovery (CDR) block. The output clock locks to an external reference. The rate adaptation block accommodates differences in clock rates by inserting or deleting IDLE ordered sets. No jitter is transferred from the XAUI input to the SFI output.

Receive Path

In the receive (Rx) path the 1.25 Gbps SFI input signal is detected and retimed by a CDR block. The receive path supports Rate Adaptation Mode.

Rate Adaptation Mode

In the rate adaptation mode, the XAUI output clock locks to an external reference. The rate adaptation block accommodates differences in clock rates by inserting or deleting IDLE ordered_sets. No jitter is transferred from the SFI input to the XAUI output. This mode is recommended for best control of jitter at the XAUI output at the expense of extra and variable latency.

The 1GbE signal is sent in 1000BASE-X format, i.e. 8B/10B encoded 1.25 Gbps.

Figure 30: SFP+ Board with 1GbE SFP Module Application: Rate Adaptation Mode

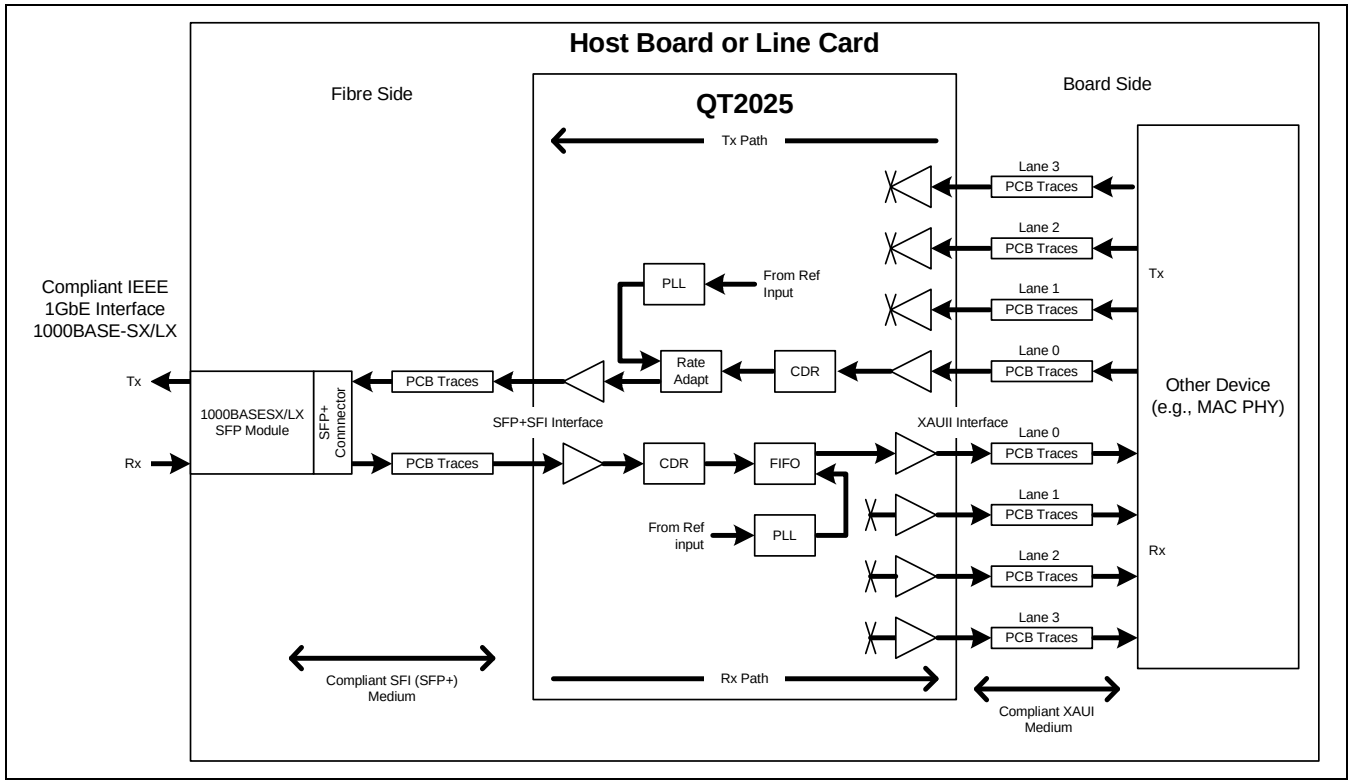
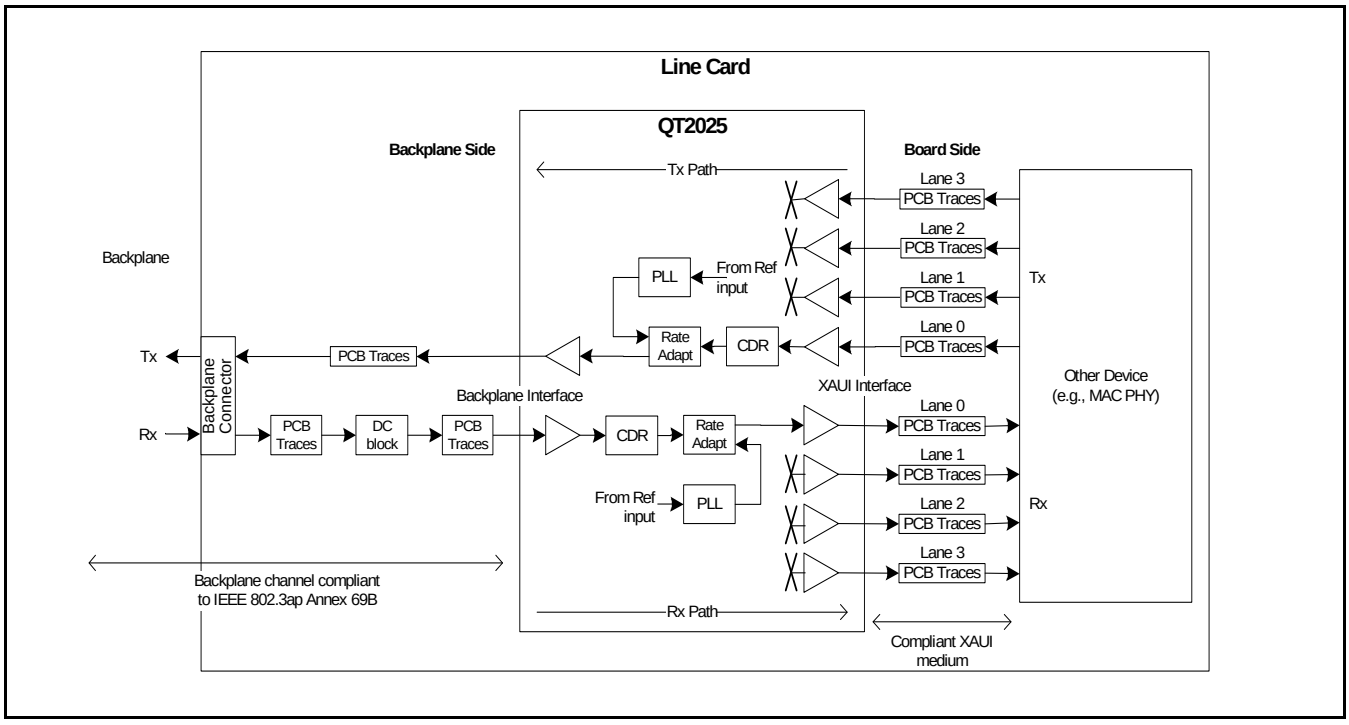


Figure 31: Backplane1GE Application with Rate Adaptation on Rx Path



Features

SFI/Backplane Interface

- Compatible with 1000GBASE-LX/SX SFP modules
- Compatible with 1000BASE-KX for backplane applications
- Signal levels based on SFP MSA and 1000BASE-KX specification
- Driver output jitter is compliant with 1000GBASE-LX/SX Clause 38.5 TP1 where TP1 is measure at the output of the host board through SFP+ connector using a host test board. The jitter includes both jitter generated by the SERDES and jitter passed through the XAUI input on the board side.
- Receiver jitter tolerance is compliant with 1000GBASE-LX/SX Clause 38.5 TP4 where TP4 is measured at the output of the SFP+ connector using a module test board.

XAUI Features

- Levels compatible with XAUI levels in IEEE 802.3 Clause 47.3

General

- In rate adaptation timing mode, complete jitter isolation between inputs and outputs
- Power in 1GbE mode is less than or equal to 10G mode. Unused 10G blocks are shut down.
- Reference oscillator of 156.25 MHz or 52.083 MHz is used in common with 10G mode.
- Tunnel from MDIO to SFP module via I2C
- Rate may be selected through MDIO register.
- FIFO includes reset control and fill level status through MDIO.

Considerations

- Through timing mode is not supported on TX path.
- LOS monitoring not provided.
- PCS monitoring not provided.
- Does not perform Clause 37 Auto-negotiation

1GE Test Patterns and Loopbacks

The chip has the capability of generating several different test patterns, outlined below. All test patterns are generated on the Receive path (XDRV0 output). The Network Loopback can be enabled in order to output the patterns on the Transmit path (FTXOUT output).

These test features are not available on the 10G data path.

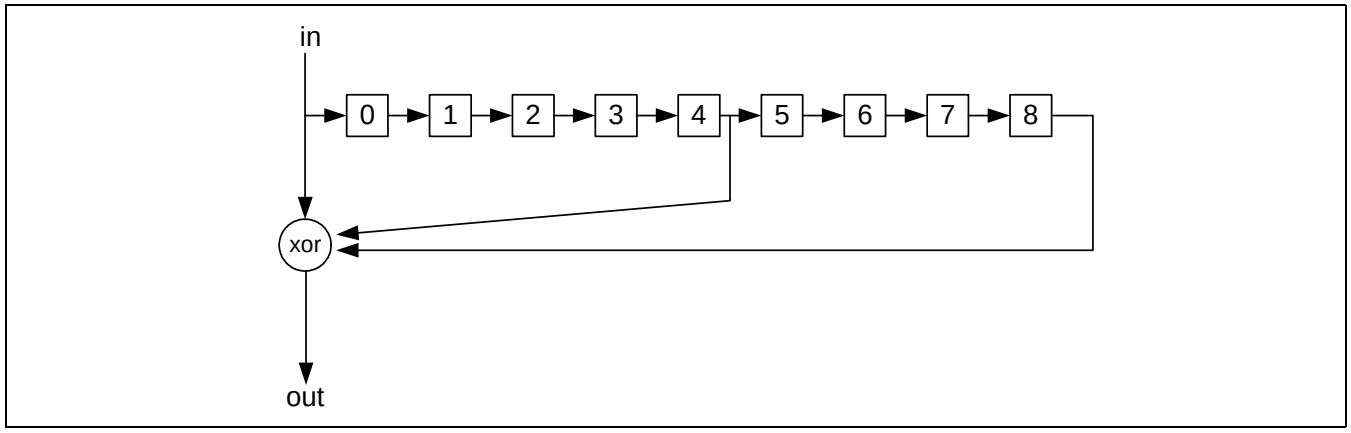
PRBS9 Test Pattern

A pseudo-random pattern generator capability is available to test the 1.25Gbps performance. When enabled, a PRBS9 pseudo-random pattern is output. Two independent pattern generators are available in the chip, one on each data path (Tx and Rx), as shown in Figure 35. The polynomial $1+x^5+x^9$ is used to generate the pattern, as shown in Figure 67 on page 113.

A PRBS9 pattern checker capability is also available which uses a 16-bit error counter to count the errors. The counter is read only, clear on read. A self-synchronizing algorithm is used to count PRBS9 errors, as shown in Figure 32. Two independent error counters are available in the chip, one on each data path (Tx and Rx), as shown in Figure 35.

When an isolated bit error occurs, it will cause the PRBS9 pattern error output to go high 3 times, once when it is received and once when it is at each tap. Thus, each isolated error will be counted 3 times in the counter.

Figure 32: 1.25Gbps PRBS9 Pattern Checker



40-bit Programmable Test Pattern

A user-programmable 40 bit long test pattern can be generated by the PHY. The chip accepts any arbitrary 40 bit sequence and can also output a static pattern (all 0's). This feature is useful for generating common test patterns such as square wave signals or Idle codes.

Two independent 40-bit pattern generators are located in the transmit and receive paths. For each generator, the pattern is programmed across 3 registers. The pattern output bit order is described in the following sections. The output order is non-sequential.

Programming Transmit 40-bit Pattern

This pattern is programmed into MDIO registers 3.C04A, 3.C04B and the lower byte of 3.C04C. The relationship between the register contents and the output sequence order is shown in Figure 33, where Pattern bit 39 is output first.

e.g. in order to program the transmit pattern generator to send out Idle codes /K28.5/D16.2/, program the registers as follows:

3.C04A = 0x5F28

3.C04B = 0x95F2

4.C04C = 0x0089

Figure 33: 1.25Gbps Transmit Path 40-bit Pattern Output Order

3.C04A

Register bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pattern bit position	30	31	32	33	34	35	36	37	38	39	20	21	22	23	24	25

3.C04B

Register bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pattern bit position	26	27	28	29	10	11	12	13	14	15	16	17	18	19	0	1

3.C04C

Register bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pattern bit position	-	-	-	-	-	-	-	-	2	3	4	5	6	7	8	9

Programming Receive 40-bit Pattern

This pattern is programmed into MDIO registers 3.C042, 3.C043 and the lower byte of 3.C044. The relationship between the register contents and the output sequence order is shown in Figure 34, where Pattern bit 39 is output first.

e.g. in order to program the transmit pattern generator to send out Idle codes /K28.5/D16.2/, program the registers as follows:

3.C042 = 0xE2D3

3.C043 = 0x4E2D

4.C044 = 0x0034

Figure 34: 1.25Gbps Receive Path 40-bit Pattern Output Order

3.C042																
Register bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pattern bit position	35	36	37	38	39	30	31	32	33	34	25	26	27	28	29	20
3.C043																
Register bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pattern bit position	21	22	23	24	15	16	17	18	19	10	11	12	13	14	5	6
3.C044																
Register bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pattern bit position									7	8	9	0	1	2	3	4

Network (Line) Loopback

This loopback routes the signal on the receive path to the transmit path. It is also useful for sending internally generated test patterns to the FTXOUT outputs. Its location is shown in Figure 35.

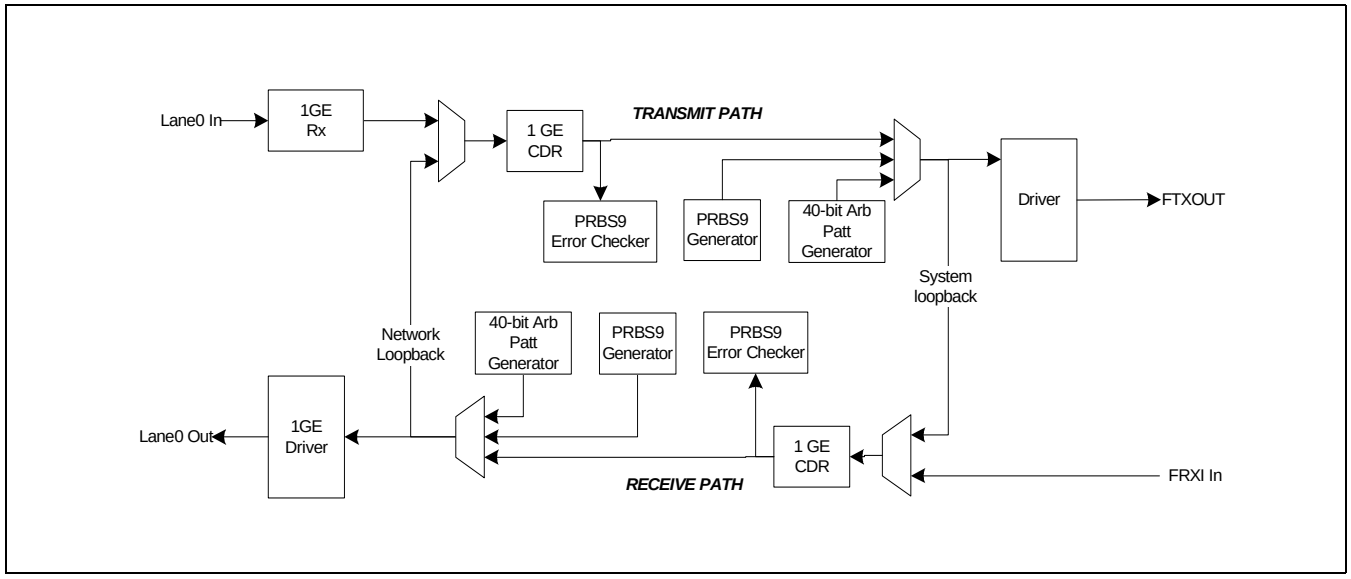
System (Diagnostic) Loopback

This loopback routes the signal on the transmit path to the receive path. It is useful for looping back the signal generated by the MAC/switch. Its location is shown in Figure 35.

Table 11: 1.25Gbps Loopback Control Registers

Loopback Name	Control Register Field(s)	Register Address	Comments
System Loopback	UC_PMA_SYS_LPBK	1.F053.<6>	
Network Loopback	XDRV_ANETLPBK_EN XCDR_ANETLPBK_EN	4.C05B.<13> 4.C05F.<8>	Register fields must be programmed in the order listed.

Figure 35: Location of 1.25Gbps Test Patterns and Loopbacks



10G Mode Datapath Clocking

This section explains the clocking architecture and features of the QT2025.

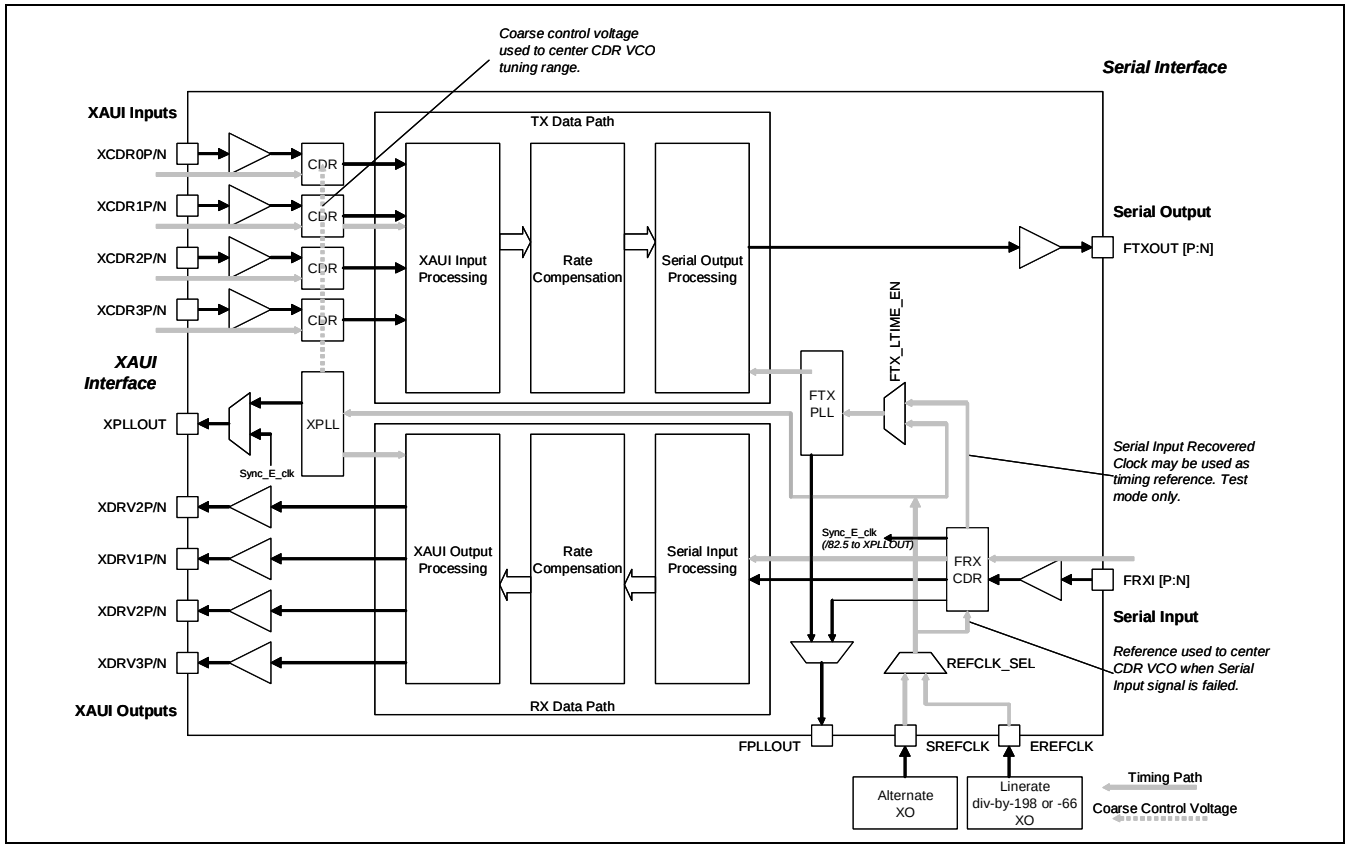
Datapath clocking MDIO Registers

Table 12 lists all the MDIO registers mentioned in this chapter that are used to control the datapath clocking. Please refer to this table for register addresses.

Table 12: MDIO Registers for Datapath Clocking

Name	Address[bit]	Description
CUS_LAN_WAN_CONFIG	1.C31Ah[7] (PRELIM)	Global control bit to select between LAN and WAN (WIS) mode.
FRX_FRC_SYNCERR	1.C030h[4]	Force PMA Sync Error
FRX_FRC_SYNCERR_VAL	1.C030h[5]	Select high Sync Error
FRX_FRCVCO	1.C030h[10]	Force Fiber input VCO
FRX_SYNC_ERR	1.C001h[1]	Status of PMA Sync Error
LTIMEOK_MSK_SYNCERR	1.C001h[7]	Mask control for sync_err defect in LTIMEOK logic
FTX_AUTOLTIME_EN	1.C001h[14]	Automatic Line Timing Mode Enable
FTX_LTIME_EN	1.C001h[9]	Force Line Timing Mode Enable
LANMODE	1.C301h[0]	LAN Mode Enable
PMA_SYSLPBK	1.0000h[0]	PMA System Loopback Enable
LANMODE_REFCLK_SEL	1.C001h[7]	Select External Clock Reference Input (selects SREFCLK for LAN)
REFSEL50	1.C301h[4]	low frequency reference applied to SREFCLKN/P input.
RXLOSB_I_FRPAD	1.000Ah[0]	Status of RXLOSB_I input pin.
RXLOSB_I_MSK	1.C001h[10]	RXLOSB_I Override
SREFCLK_FREQ	1.C302h[1]	low frequency reference applied to SREFCLKN/P input.
FTX_NETWORK_SYNC_SELECT	1.C308h[14]	Enable Control for div-by-82.5 recovered clock (LAN only)
AISL	2.0021h[4]	Latched Line Alarm Indication Signal
LOF	2.0021h[7]	WIS LOF Status (Loss of Frame). NOT USED IN 10GBASE-KR App.
LTIME_MSK_AISL	1.C030h[14]	Line Timing AISL Override. NOT USED IN 10GBASE-KR App.
LTIME_MSK_LOF	1.C030h[15]	Line Timing LOF Override. NOT USED IN 10GBASE-KR App.
VCXOENB	1.C301h[2]	VCXO PLL Enable. NOT USED IN 10GBASE-KR App.
VCXOONLY	1.C301h[1]	VCXO is only reference clock available. NOT USED IN 10GBASE-KR App.
VCXOSEL50	1.C301h[3]	low frequency reference applied to VCXOIN/P input. NOT USED IN 10GBASE-KR App.
WIS_EN	2.0007h[0]	Port Type Selection. NOT USED IN 10GBASE-KR App.

Figure 36: LAN Mode Timing (10GBASE-R)



LAN Application Timing Modes

This section describes the LAN timing mode of the QT2025. The LAN timing mode is selected when QT2025 is placed in LAN mode (LANMODE = 1) for 10GBASE-R transport.

The XDRV and Fiber output quadrants share timing references, but are generally independent of the XCDR and fiber input quadrants. The timing architecture and timing paths in LAN mode are illustrated in Figure 36.

The 10G output derives timing from a line-rate divide-by-66 or alternatively a line-rate divided-by-198 external reference clock applied at EREFCLK (or an alternate reference applied at SREFCLK, when MDIO register field LANMODE_REFCLK_SEL = 1). The FTX PLL generates a line-rate clock from the reference by multiplying the frequency. The FTX PLL output provides a clock for the 10G output processing block and outputs.

The 10G input CDR locks to the received signal and generates a recovered clock. The recovered clock provides timing to the fiber input processing block. When a SYNCERR is generated, the Fiber Input CDR will lock to the reference applied to the selected reference, either EREFCLK or SREFCLK, to pull the frequency back to nominal. Once the SYNCERR has cleared, the CDR will attempt to lock to the fiber Input signal.

The XDRV outputs derive timing from the XPLL. The XPLL generates the 3.125 GHz clock from the EREFCLK or SREFCLK reference. The XPLL output provides a clock for the XAUI output Processing Block and I/Os.

For each XCDR input, a CDR locks to the received signal and generates a recovered clock. The recovered clock from lane 1 (XCDR1) provides a clock for the XCDR processing block. Transfer of data across clock boundaries along each data path is accomplished through rate compensation blocks.

If the FRXI(P/N) data rate is +/- 500 ppm from the FTXOUT(P/N) data rate a sync error alarm will be generated.

Forced Line Timing Mode

The Forced Line Timing mode forces the 10Gbps driver output to derive timing from the 10Gbps Input recovered clock. The Forced Line Timing mode is useful for various test scenarios or implementations where the timing is controlled externally. Forced Line Timing is invoked by setting MDIO register field FTX_LTIME_EN to 1.

Synchronous Ethernet Output Clocks

The PHY is able to output a subrate recovered clock from the 10Gbps input for use by an external device for synchronous ethernet applications. A 125 MHz clock is available on the XPLLOUT output (linerate div-by-82.5), while a 156.25MHz clock is available on both the XPLLOUT and FPLLOUT outputs (Line Rate div-by-66).

Truth tables for both outputs indicate how to program the PHY (see Page 65).

Considerations

The receiver can only be programmed to supply one recovered clock frequency at a time. The div-by-82.5 and div-by-66 clocks cannot be generated at the same time.

The 125MHz clock cannot be output when internal Line Timing is enabled.

WAN Application Timing Modes (10GBASE-W Mode)

This section describes additional timing modes supported only in WAN (WIS) mode, which is enabled by setting the CUS_LAN_WAN_MODE field to 1b when firmware is initialized. Note: WIS_EN enable (2.0007h[0]=1b) is set by default. The timing paths through the QT2025 vary depending upon the mode of the device. Some modes that affect these paths include:

1. VCXO PLL Mode (VCXOENB): enable or disable (default) using external VCXO for line timing.
2. Line Timing Mode (FTX_LTIME_EN and FTX_AUTOLTIME_EN): Disabled, Automatic, or Forced.

In order to understand the relationship between timing reference and the behavior of input and output signals it is important to understand the general timing architecture of the QT2025. In the following sections, the timing architecture in the WAN mode is explained.

Timing Architecture in WAN mode

The typical timing architecture and timing paths in WAN mode are illustrated in Figure 37 and Figure 38. An optional “VCXO only” configuration mode is available where the VCXO is the sole WAN timing reference, (called VCXOONLY mode). The VCXO control loop is enabled by setting VCXOENB to 0b and the device is set to have the VCXO as the only input by setting VCXOONLY to 1b.

Figure 37: Timing with Fixed Frequency Reference (10GBASE-W)

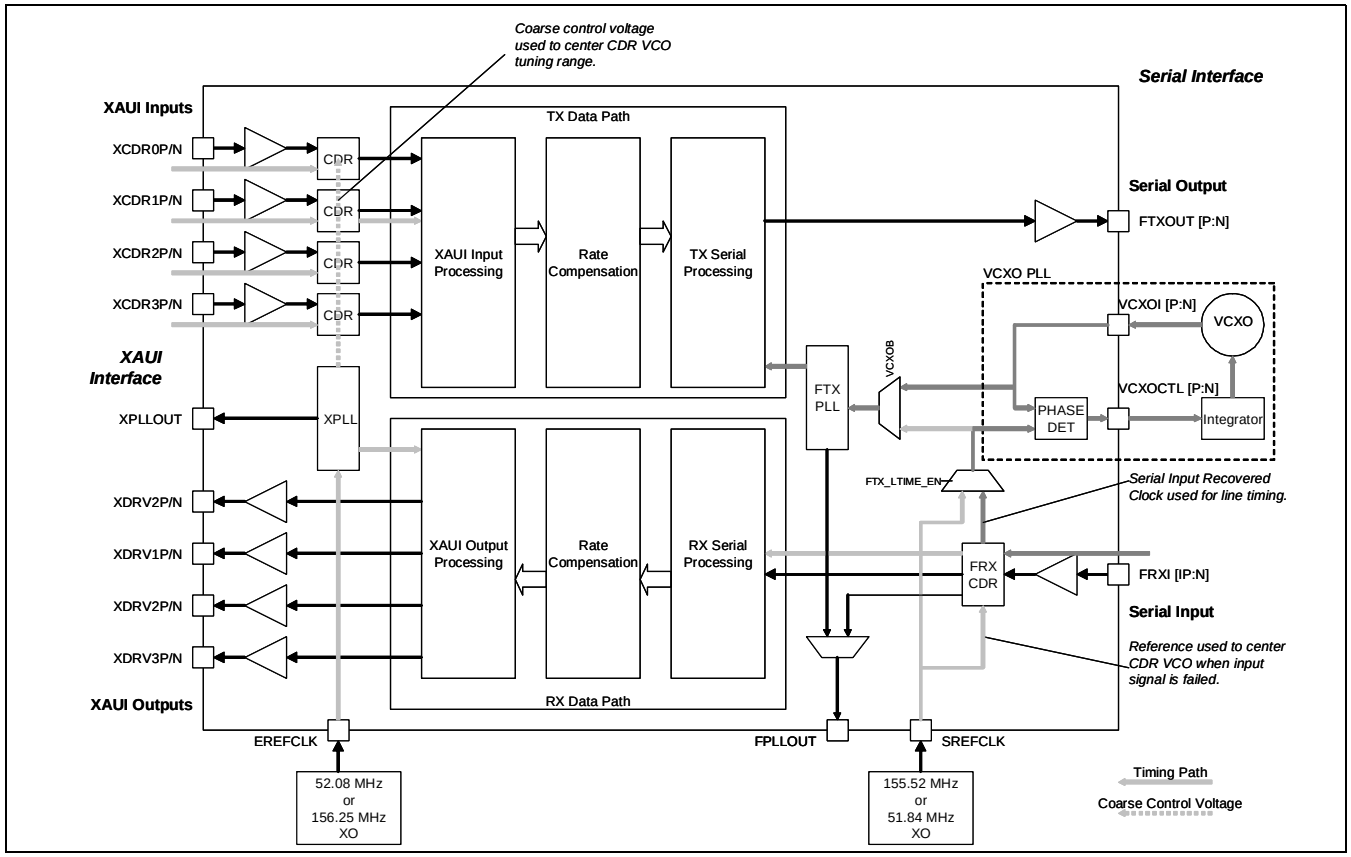
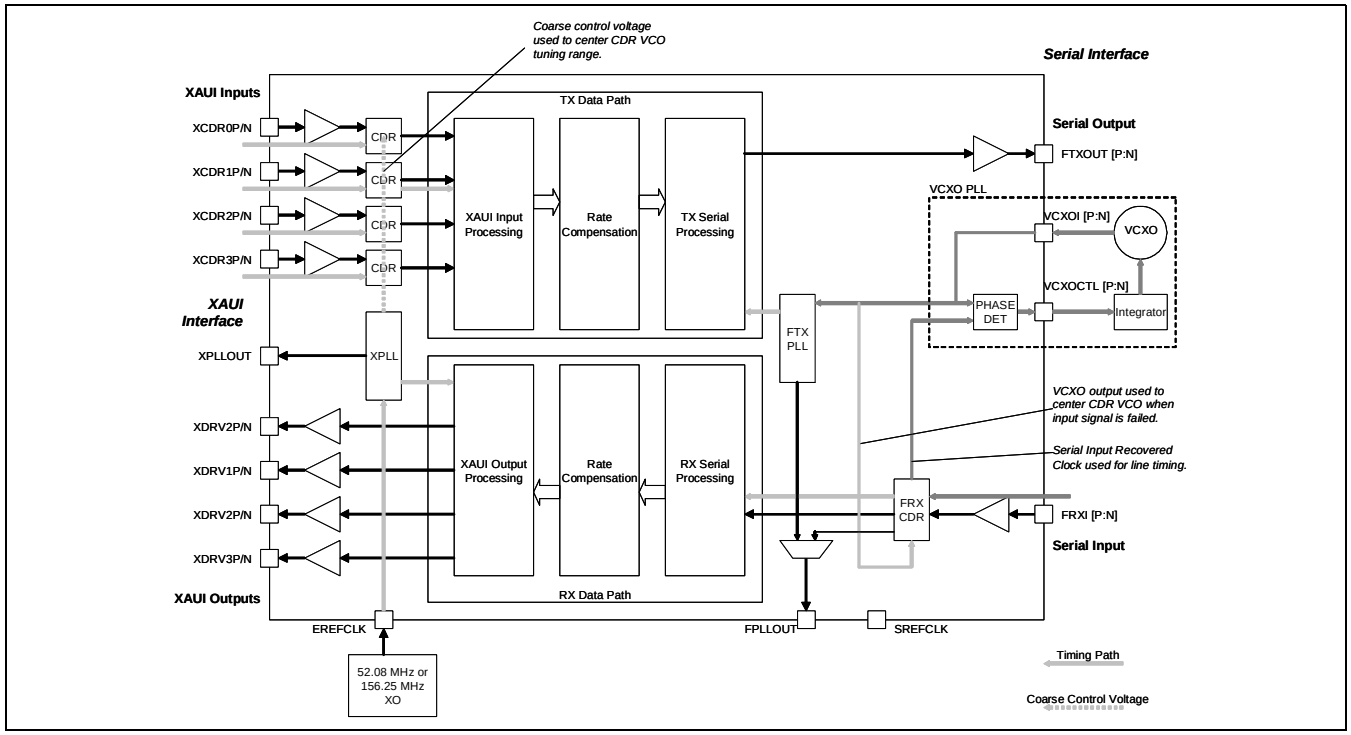


Figure 38: Timing without Fixed Frequency Reference (10GBASE-W)



The FTXOUT output derives timing from a line rate divided-by-192 or by-64 clock applied at SREFCLK or the received signal on the FRXI input in line timing modes. The FTX PLL generates a line rate clock from the selected reference by multiplying the frequency. The FTX PLL output provides timing for the serial processing block and FTXOUT output. By default the FTX PLL will lock to the reference applied at SREFCLK, however it may optionally lock to the recovered clock from the 10G CDR (in line timing modes). In order to reduce phase noise from the selected reference and consequently on the FTXOUT output, an optional VCXO PLL may be used to filter phase noise on the linetiming reference clock.

The FRX CDR locks to the received signal and generates a recovered clock. The recovered clock provides a clock to the FRXI input processing block and provides an optional reference for the FTXOUT output (for line timing modes). When the recovered clock deviates by >500ppm from the reference clock, the FRXI input CDR will then lock to the reference from SREFCLK (or VCXOI when in VCXOONLY mode) to pull the VCO frequency to nominal frequency. The CDR will lock to the FRXI input signal when the clock rate is <500ppm from the reference.

The XAUI outputs derive timing from a 52.083 MHz or a 156.25 MHz clock applied at EREFCLK. The XPLL generates the 3.125 GHz clock from the reference by multiplying the frequency. The XPLL output provides a clock for the XAUI processing block and I/Os. For each XAUI input, a CDR locks to the received signal and generates a recovered clock. The recovered clock from lane 1 (XCDR1) provides timing to the XAUI input processing block.Transfer of data across clock boundaries along each data path is accomplished through rate compensation blocks.

Line Timing

Line timing is used only in the QT2025 WIS Mode to ensure the transmitted data is synchronized to the SONET network. In line timing mode, the reference clock used for the transmit PLL is derived from the recovered receive clock. Line timing mode is enabled by the FTX_AUTOLTIME_EN field (see Table 12 on page 55).

Line timing permits the FTXOUT output to derive timing from the FRXI input. This mode is useful for applications where it is necessary or desirable for the FTXOUT output to be synchronous with equipment at the far end. For example, the 10G serial interface may connect to a SONET ADM (Add/Drop Multiplexer) which directs synchronous SONET payloads to one of several line outputs.

Three line timing control modes are provided: Line Timing Disabled, Automatic Line Timing, and Forced Line Timing. The Automatic Line Timing control mode is supported only in WAN mode. The line timing control mode is determined by the MDIO line timing control bits 1.C001h[9] and 1.C001h[14] which are interpreted as described in Table 13.

Table 13: Line Timing Control Modes

Force Line Timing 1.C001h.9	Automatic Line Timing 1.C001h.14	Line Timing Mode
0	0	Line Timing Disabled In WAN mode the FTXOUT output always derives timing from SREFCLK (or VCXOI in VCXOONLY mode). In LAN mode the FTXOUT output always derives timing from EREFCLK or SREFCLK.
0	1	Automatic Line Timing Line timing with holdover. In WAN mode only, the FTXOUT output derives timing from the recovered clock from the FRXI input when the FRXI input has a valid signal. When the FRXI input does not have a valid signal, the clock source for the FTXOUT output automatically switches to the local SONET reference clock (SREFCLK, or VCXOI in VCXOONLY mode).
1	x	Forced Line Timing In WAN or LAN mode, the FTXOUT output always derives timing from the recovered clock from the FRXI input.

Line Timing Disabled Mode

The Line Timing Disabled mode is the default Line Timing mode. In this mode, line timing is fully disabled. This mode is used in applications where the FTXOUT output is intended to always derive timing from a local frequency source such as a crystal oscillator. In WAN mode, the FTXOUT output will always derive timing from SREFCLK or VCXOI in VCXOONLY mode. In LAN mode, the FTXOUT output will always derive timing from either EREFCLK or SREFCLK.

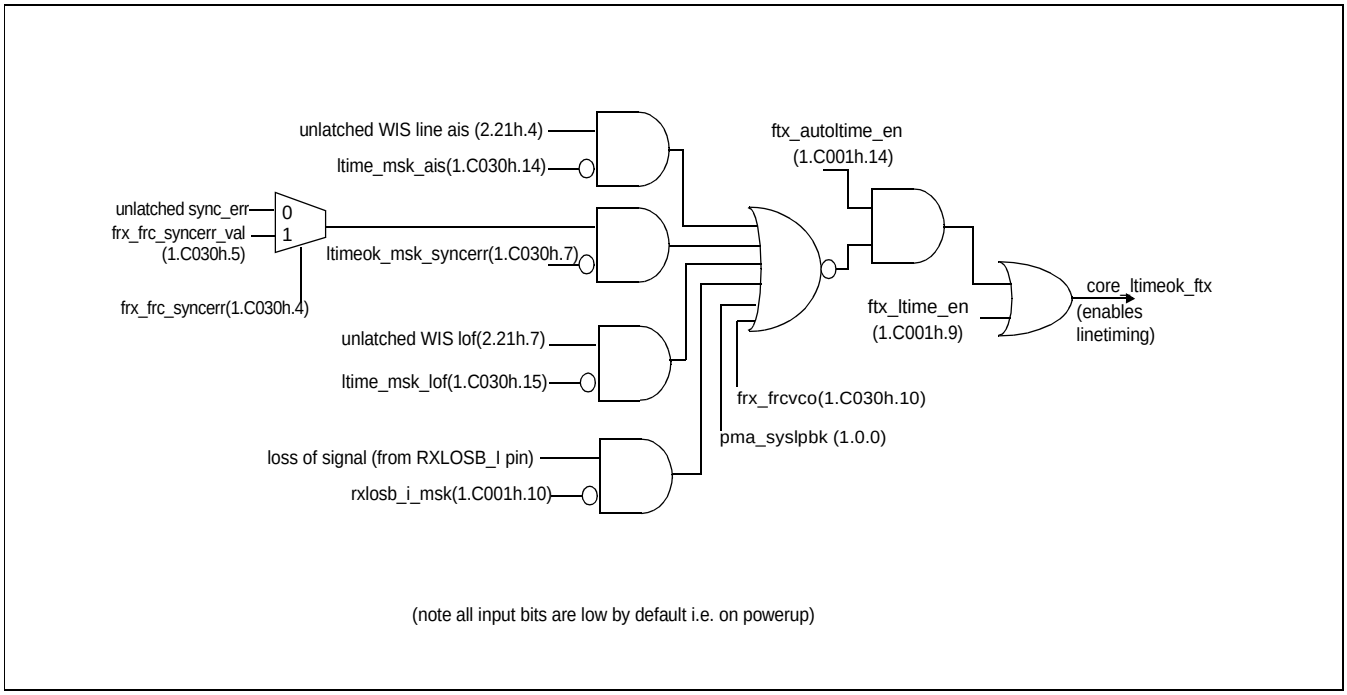
Automatic Line Timing Mode

The Automatic Line Timing mode allows the FTXOUT output to derive timing from a valid recovered clock from the FRXI input. When the FRXI input is not valid, the FTXOUT output derives timing from SREFCLK (or from VCXOI in VCXOONLY mode). The QT2025 deems the recovered clock from the FRXI input to be valid when all of the following conditions are TRUE:

1. Serial receive CDR VCO is not in forced mode (FRX_FRCVCO = 0)
2. Serial Interface is not in PMA System Loopback (PMA_SYSLPBK = 0)
3. PMA LOS defect is clear RXLOSB_I = 0 (visible in RXLOSB_I_FRPAD) or LOS Override is Set (RXLOSB_I_MSK).
4. PMA_SYNCERR unlatched defect or SYNCERR Override is Set (FRX_FRC_SYNCERR = 0 & FRX_FRC_SYNCERR_VAL = 1)
5. WIS LOF unlatched defect is clear (latched version visible in LOF) or LOF Override is Set (LTIME_MSK_LOF)
6. WIS Line AIS unlatched defect is clear (latched version visible in AISL) or AIS Override is Set (LTIME_MSK_AISL)

For each of the line timing conditions, a mask capability is provided. By default, the mask for each defect is off but may be independently activated to prevent the associated defect from disabling line timing. The internal signal, ltimeok, is used to control the line timing state. The effective logic used to generate the ltimeok signal is represented in Figure 39.

Figure 39: Line Timing Enable Logic



Further qualification of the signal may be required by external software. For example, it must be determined whether the use of the received signal as a line timing reference will result in a timing loop. This may happen if the far end is also in line timing mode. Qualification of the received signal may be achieved using the Synchronization Status Message (SSM) in the WIS S1 byte.

Forced Line Timing Mode

The Forced Line Timing mode forces the FTXOUT output to derive timing from the FRXI input recovered clock. The Forced Line Timing mode is useful for various test scenarios or implementations where the timing is controlled externally. This mode is supported in WAN and LAN modes.

Support for External Line Timing Control

In order to support external control (e.g., by firmware) of the line timing the LASI may be configured to interrupt on any of the relevant receiver conditions. Relevant defects and conditions include:

1. PMA LOS defect
2. PMA sync_err defect (FRX_SYNC_ERR)
3. WIS LOF defect (LOF)
4. WIS Line AIS defect (AISL)
5. Validated Synchronization Status message in received WIS S1 byte has changed.

A separate interrupt enable bit for each of the conditions listed above is provided. By default, each enable bit is clear. The enable bit for each condition may be set as required by the implementation.

VCXO PLL

There is also a configuration to provide support for a line rate divided by 64 VCXO based PLL to filter phase noise on the SREFCLK or recovered clock to ensure compliant jitter generation and jitter transfer performance as measured on the FTXOUT output. The VCXO PLL is supported only in WAN mode. There is also support for a self-centering VCXO to reduce board cost by eliminating the need for a fixed frequency XO driving SREFCLK when the VXCO PLL is used.

VCXO PLL Interface

The VCXO PLL interface is illustrated in Figure 40 on page 63.

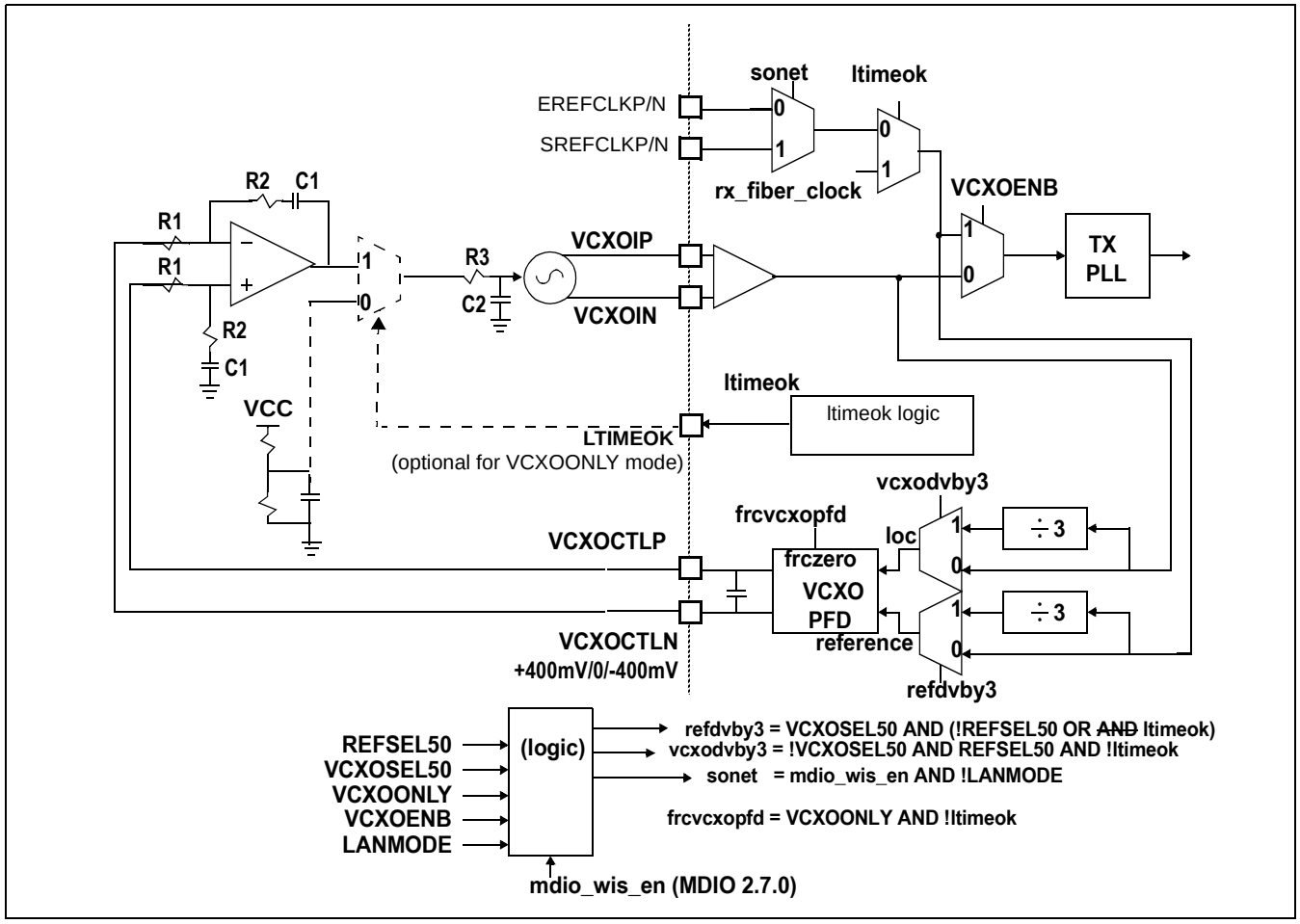
When using the VCXO PLL, VCXOENB is set low, and the VCXO drives the reference input of the TX PLL. The on-chip VCXO phase-frequency detector (VCXO PFD) compares the phase and frequency of the VCXO clock with that of a reference clock and generates a tri-state output which drives an external opamp configured as a differential integrator. The external opamp and power supply are chosen to provide the appropriate voltage swing for the VCXO. The reference clock input to the VCXO PFD may be from either SREFCLK or the FRXI input recovered clock (rx_fiber_clock). The selectable divide-by-3 blocks at the VCXO PFD inputs allow for any combination of line rate divide-by-64 or divide-by-192 reference clock and VCXO frequencies based on the settings of REFSEL50[1] and VCXOSEL50. For implementation details refer to “VCXO PLL Implementation Recommendations” on page 64

The LTIMEOK output indicates that line timing conditions are valid and that line timing is internally enabled. In a linetiming application with no reference applied to SREFCLK, indicated by setting VCXOONLY to 1, the LTIMEOK output being low may be used to force the VCXO to its center frequency; when the LTIMEOK output is low, the VCXO PFD differential output is coincidentally forced to 0 V. The logic which generates LTIMEOK is illustrated in Figure 39.

The VCXO interface parameters are specified in the Table 62 on page 153.

1. For proper operation REFSEL50 should be set to the same value as SREFCLK_FREQ.

Figure 40: VCXO PLL Interface block diagram



VCXO PLL Implementation Recommendations

VCXO PLL Register Settings

Recommended register settings for each potential application of the VCXO PLL are listed in Table 14.

XPLLOUT Output Clock Driver

The XPLLOUT interface is a differential subrate clock driver and comprises a differential signal pair, XPLLOUTP and XPLLOUTN. It is capable of providing several subrate clocks synchronous to the transmitter and a div-by-82.5 clock synchronous to the recovered 10Gbps data. Configuration is described in Table 15.

XPLLOUT is internally terminated to 50Ω on each signal. The outputs must be AC coupled into 50Ω loads via 50Ω transmission lines.

FPLLOUT Output Clock Driver

The FPLLOUT interface is a differential clock driver and comprises a differential signal pair. FPLOUTP and FPLLOUTN. It is capable of providing several subrate clock outputs. There is one FPLLOUT interface for each port.

FPLLOUT is internally terminated to 50Ω on each signal. The outputs must be AC coupled into 50Ω loads via 50Ω transmission lines. The output driver is a CML type.

FPLLOUT Clock Output Modes

A subrate clock from the transmit PLL (FTX PLL) can be output on pins FPLLOUTP/N, for example to serve as a reference clock to the XFP module in an XFP host board application or for test purposes. A clock from the receive PLL (FRX PLL) can also be output on FPLLOUTP/N to monitor FRXI received clock. A divide-by-66 receive clock is generated in LAN mode, while a divide-by-64 receive clock is generated in WAN mode.

Configuration is performed using MDIO registers. Table 16 illustrates the register settings to set the FPLLOUT signal.

Table 14: VCXO PLL Control Pin Settings

Implementation			Register Settings			
VCXO PLL Present?	**SREFCLK Frequency (MHz)**	**VCXO Frequency (MHz)**	**VCXOENB 1.C301[2]**	**VCXOONLY 1.C301[1]**	**REFSEL50 1.C301[4]**	**VCXOSEL50 1.C301[3]**
No	51.84	x	1	x	1	x
No	155.52	x	1	x	0	x
Yes	51.84	51.84	0	0	1	1
Yes	51.84	155.52	0	0	1	0
Yes	155.52	51.84	0	0	0	1
Yes	155.52	155.52	0	0	0	0
Yes	No source [1]	51.84	0	1	x	1
Yes	No source [1]	155.52	0	1	x	0

1. If no SREFCLK is implemented, and 20ppm operation for SONET applications is required, then the VCXO will likely need to be temperature-compensated.

Table 15: XPLLOUT Configuration Settings

XPLLOUT Clock Output	XPLLOUT_EN 4.C05Bh [10]	XPLLOUT_SEL 4.C05Bh [12:11]	FTX_NETWORK_SYNC_SELECT 1.C308h [14]	XPLLOUT_CLK_EN 1.C0FDh[1]	Notes
Output Off	0	xx	x[1]	0	
156.25MHz Reference Clock	1	00	x	0	XAUI Linetiming must be disabled.
312.5MHz Reference Clock (MAC Clock)	1	01	x	0	
250MHz Ring Oscillator Output	1	11	x	0	Test feature only.
Recovered Clock from 10Gbps input					
Line Rate div-by-82.5 (125MHz) Synchronous Ethernet Clock	1	10	1	1	
Line Rate div-by-66 (156.25MHz) LAN Mode or Line Rate div-by-64 (155.52MHz) WAN Mode	1	10	0	1	Output clock rate changes from LAN to WAN modes.

1. An ‘x’ in the table indicates that the field value does not affect the resultant state (“don’t care” bits).

Table 16: FPLLOUT Configuration Settings

FPLLOUT Clock Output	FPLLOUT_DIV32_EN 1.C308h[9]	FPLLOUT_156BUFF_PWDN 1.C309h[12]	FPLLOUT_FRXBUFF_PWDN 1.C30Ah[0]	FPLLOUT_EN 1.C30Ah[1]	FPLLOUT_SEL 1.C30Ah[3:2]	FTX_NETWORK_SYNC_SELECT 1.C308h[14]
Transmit Clock (derived from local reference clock)						
Line Rate div-by-64	1	1	1	1	00	0
Line Rate div-by-66	0	0	1	1	10	0
Recovered Clock from 10Gbps input						
Line Rate div-by-66 (156.25MHz) LAN Mode or Line Rate div-by-64 (155.52MHz) WAN Mode	0	1	0	1	01	0
Line Rate div-by-82.5 (125MHz) Synchronous Ethernet Clock	0	1	0	1	01	1

WIS Mode

This section describes the function and extended features of the WIS block in the QT2025 devices. The WIS block can be bypassed by setting the MDIO register 2.0007h. When bypassed, the QT2025 is 10GE (or 10GFC) protocol compliant. The WIS transmitter and receiver functionality is compliant with IEEE 802.3 Clause 50. In addition, the QT2025 provides WIS compliant test pattern generation features.

Extended WIS Features

In addition to supporting the IEEE 802.3-2005 WIS requirements, the QT2025 integrates a series of additional features common for SONET framers.

SS Bits (H1)

The QT2025 allows the user to specify the s0 s1 bits which are found in bits 5 and 6 of the H1 octet in a SONET frame. For SONET networks, this value is 00 and is ignored by SONET receivers. This feature allows QT2025 to be compatible with SDH networks, where the SS bits are typically set to 10.

APS Channel (K1 and K2)

The APS channel bytes are located in the first STS-1 of the STS-192 only and are used for automatic protection switching signaling.

A new value in either byte is only validated after it has been received in 3 consecutive frames. Upon validation of a new K1 or K2 byte, the respective K byte is stored in a status register and an interrupt is generated (the interrupt can be masked). The validation of the K bytes is not affected by any alarm or defect.

If 3 identical consecutive K bytes are not found in 12 frames, an inconsistent K byte interrupt is generated (the interrupt can be masked).

A programmable value for K1 and K2 can be transmitted by QT2025 if the feature is enabled.

Synchronization Status (S1)

The synchronization status bytes byte is located in the first STS-1 of the STS-192 only, and is used to convey the synchronization status of the network element.

A new value is only validated after it has been received in 8 consecutive frames. Upon validation of a new S1 byte, the S1 byte is stored in a status register and an interrupt is generated (the interrupt can be masked).

A programmable value for S1 can be transmitted by QT2025 if the feature is enabled.

Line BIP-8 Signal Fail (SF)

QT2025 generates a Signal Failure (SF) alarm if the number of Line BIP-8 (B2) errors monitored during a programmable timing window (2.C410h) exceeds a programmable threshold (2.C411h). There is a second programmable threshold (2.C412h) which is used to provide hysteresis when removing the SF alarm. The user must specify the correct thresholds and timing window to achieve the desired BER monitoring. SF coding violations over the timing window are reported in 2.C413h, a 16 bit non-rollover counter.

At the end of each timing window, a time-out alarm is generated to notify the user and the number of coding violations is latched to 2.C413h. The user can generate the SF in system firmware by taking advantage of the LASI interrupt and the ‘SF Timing Window Expired Flag’ in the WIS Extended Alarm register (MDIO register bit 2.C502h[11]).

SF monitoring is enabled by setting MDIO register bits 2.C002h[8] to 1.

Line BIP-8 Signal Degrade (SD)

QT2025 generates a Signal Degrade (SD) alarm if the number of Line BIP-8 (B2) errors monitored during a programmable timing window (2.C400h) exceeds a programmable threshold (2.C401h). There is a second programmable threshold (2.C402h) which is used to provide hysteresis when removing the SD alarm. The user must specify the correct thresholds and timing window to achieve the desired BER monitoring. SD coding violations over the timing window are reported in 2.C403h, a 16 bit non-rollover counter.

At the end of each timing window, a time-out alarm is generated to notify the user and the number of coding violations is latched to 2.C403h. The user can generate the SD in firmware by taking advantage of the LASI interrupt and the ‘SD Timing Window Expired Flag’ in the WIS Extended Alarm register (MDIO register bit 2.C502h[9]).

SD monitoring is enabled by setting MDIO register bits 2.C002h[7:1].

Pointer Justification Event Counters

QT2025 implements an 8 bit counter incremented by one on every Positive Stuff event. This counter does not rollover and is cleared to 0 on read. The Positive Stuff event counter is located in the lower 8 bits of MDIO register 2.C020h.

Likewise, the QT2025 implements an 8 bit counter incremented by one on every Negative Stuff event. This counter does not rollover and is cleared to 0 on read. The negative Stuff event counter is located in the upper 8 bits of MDIO register 2.C020h.

Extended J1 Trace Messaging (64 bytes)

The QT2025 supports both 16 and 64 byte J1 trace messaging. The IEEE 802.3 compliant 16 byte J1 trace messaging is the default mode of operation. To use 64 byte J1 trace messaging, the user must enable this mode by writing to register 2.C002h: the WIS TX will then transmit the J1 bytes located in registers 2.C200h to 2.C217h and the WIS RX will store the received J1 bytes in registers 2.C100h to 2.C117h.

Transport Overhead Serial Interface

This feature allows Transport Overhead byte insertion in the WIS TX SONET frame and Transport Overhead byte extraction from the WIS RX SONET frame. This gives the user extra flexibility to use and process SONET overhead bytes that are not supported by the IEEE 802.3 Clause 50: the user can now use the DCC bytes for example. This feature supports 4 modes of operation on both RX and TX:

- insert/extract all STS-1 Transport Overhead Bytes (27 bytes per frame, corresponding to Section and Line overhead).
- insert/extract the D1 to D3 Bytes (3 bytes per frame).
- insert/extract the D4 to D12 Bytes (9 bytes per frame).
- insert/extract the D1 to D12 Bytes (12 bytes per frame).

The mode is controlled for both the Tx and Rx paths by MDIO register 2.C010h. The interface is enabled using register bits 2.C002h[3:2].

QT2025 has a two-wire interface on the transmit path for byte insertion: an output clock pin (TDCC_CLK) that runs at 1.944MHz (155.52MHz/80) and an input data pin (TDCC) that is used to sample the incoming data (serial OH bytes). Similarly, QT2025 has a 2 wire interface on the receive path for byte extraction: an output clock pin (RDCC_CLK) that runs at 1.944MHz and an output data pin (RDCC) that is used to shift out the data (serial OH bytes). QT2025 will drive a new data value on the falling edge of the clock (the chip connected to the serial interface can safely latch the data on the rising edge of the pin).

Programmable Overhead Byte Insertion

This feature allows the insertion of 3 bytes in the WIS TX SONET frame. The insertion is limited to the transport / path overhead, fixed stuff and the first data of the payload until column 127. The location and number of frames is determined through 3 programmable registers, located at MDIO registers 2.C601h - 2.C603h.

Programmable Overhead Byte Extraction

This feature allows the extraction of 3 bytes in the WIS RX SONET frame. The extraction is limited to the transport overhead and path overhead bytes only. The location and number of frames is determined through 3 programmable registers, located at MDIO registers 2.C611h - 2.C613h. Three separate controls bits are used to initiate extraction of each byte, located in register bits 2.C610h[2:0]. After the bytes are extracted, their values are stored in 3 separate registers, using the lower 8 bits of MDIO registers 2.C614h - 2.C616h.

Control and Status Pins Description

I/O Polarity and Monitoring

The user can read MDIO register 1.D002h to monitor the state of most low speed CMOS inputs. Exceptions are PRTAD<4:0>, TRST_N and RESETN. The state of most low speed CMOS outputs can be found in MDIO register 1.D004h.

The user can also control the polarity of most low speed CMOS pins (MDIO registers 1.D003h, 1.D005h). Changing the polarity of a pin inverts the logic of the pin function.

Control (Input) Pins

These inputs are compatible with 1.2V CMOS logic, but can tolerate up to 3.3V logic levels. This section provides additional information.

Reset Control Pin (RESETN)

The RESETN pin is used to apply a hard reset to the chip. When the RESETN pin is '0' the chip is placed in a reset state and will not carry traffic or respond to MDIO commands. When the RESETN pin transitions from a '0' to a '1' the startup sequence will be initiated.

On power up, the RESETN pin must be held low for 500µs after the power supplies reach their nominal values before allowing the startup sequence to begin.

Receive LOS Control Pin (RXLOSB_I)

The RXLOSB_I input is used to indicate a loss of the optical signal on the high-speed input (FRXIP/N). This input may be connected to the RX_LOS signal from an XFP module or the LOS signal from an SFP+ module.

The input is active high. When an LOS is detected, the chip will squelch traffic.

As 10GBASE-KR back plane applications do not involve optical modules, the RXLOS_I input may be driven directly by the LOSOUTB output pin with the QT2025 device.

The pin status is monitored in MDIO register 1.C200h[3] and 1.D002h[2].

Port Address Control Pins (PRTAD<4:0>)

The PRTAD bits set the port address for MDIO transactions.

TXON Pin

The TXON pin has two different operating modes in the PHY, either as an input or an output. The operating mode is determined by the XFP register field (1.C301h[11]). TXON acts as an input when XFP=0 and as an output when XFP=1. Operation in each mode is described below.

1. OUTPUT: The TXON pin can be used as an output, intended to drive the MOD_DESEL pin of an XFP module. The output state is register controlled by the MOD_DESEL_TOPAD field.
2. INPUT: It can also be used as an input pin. In this mode, TXON control the TXENABLE pin output. When TXON=0, it forces the TXENABLE signal high. In SFP+ applications, it is used to drive the TX_DIS signal.

The firmware supplied with the PHY sets the XFP bit for each application (i.e. different boot modes).

- XFP Applications: set XFP=1.
- Backplane Applications: set XFP=0.
- SFP+ Applications: may set XFP=0 or 1. It is set to '1' when the DOM memory space is mapped to MDIO register range 1.8007-1.8106. It is set to '1' when the DOM memory space is mapped to 1.A000-1.A0FF.

The customer should not change the XFP register field, as this may cause unexpected behavior.

The TXON pad status is monitored in MDIO register 1.D002h[0].

EEPROM Write Protect Control Pin (EEPROM_PROT)

The EEPROM_PROT pin may be used to indicate the absence of an XFP or SFP+ module. A high level indicates the module is absent. This pin should be connected to the XFP module or SFP+ module 'Mod_ABS' pin.

The pin status is monitored in MDIO register 1.C200h[0].

The EEPROM_PROT pin may alternately be used to provide write protection to the EEPROM memory

space. When the EEPROM_PROT pin is low, full MDIO write access to MDIO registers 1.8007 - 1.8106h is allowed. When EEPROM_PROT is high, it blocks MDIO writes to the registers corresponding to EEPROM registers 0 to PL and PU to 255 inclusive thereby preventing changes to these EEPROM registers. When EEPROM_PROT is high, it also blocks MDIO writes to the DOM register space from 1.A000 - 1.A0FFh. I2C write access is also blocked.

The pin status is monitored in MDIO register 1.D002h[4].

LASI Interrupt Control Pin (LASI_INTB)

LASI_INTB input is used as the XFP module interrupt pin. When used in an XFP application, this pin should be connected to the XFP module interrupt pin output. When the LASI_INTB input is asserted low (alarm condition), Register bit 1.9005h.3 is set to 1, causing the LASI output to be asserted.

The pin status is monitored in MDIO register 1.D002h[3].

Laser Fault Control Pin (TXFAULT)

The TXFAULT pin is an input used as a status indicator from an external optical module. It should be connected to the Mod_NR signal of an XFP module or the TXFAULT pin of an SFP+ module in an SFP+ application.

The pin status is monitored in MDIO register 1.C200h[1] & 1.D002[1].

TAP Port Reset Pin (TRST_N)

The TRST_N pin is the reset pin for the Test Access Port (TAP) port. During normal operation, the TAP port is not used and should be held in reset by grounding the TRST_N pin.

Low-Speed Output Pins

All low-speed output pins have an open drain output. An external 10-20kΩ pullup resistor to Vdd is required. The MDIO pin can also be configured as a push-pull driver.

Link Alarm Status Interrupt Pin (LASI)

The LASI pin is an active-low output used to indicate a link fault condition has been detected in either the receive or transmit paths. It can be used as an interrupt to a host controller. Control registers are provided so LASI can be programmed to assert only for specific fault conditions.

Receive Loss-of-Signal Pin (LOSOUTB)

In SFP+ and KR applications, LOSOUTB is used to report when a loss of signal (LOS) is declared against the input signal at FRXIN/P. The criteria for LOS assertion/deassertion can be set via register settings. LOSOUTB=1 indicates that LOS is asserted.

In XFP applications, LOSOUTB is used as a reset controller and is intended to drive the P_down/RST module input.

The pin status is monitored in MDIO register 1.D004h[2].

TXENABLE

In an SFP+ application, the TXENABLE pin on the PHY is used to control the TX_Disable input of the SFP+ module. This is used to turn off the transmitter output.

In an XFP application, the TXENABLE Pin is used to control the TX_DIS input of the XFP module. This is used to turn off the transmitter output.

By default, TXENABLE will be in the enable state and the driver pulls the TXENABLE output low. In the disable state, the open drain output is high-Z allowing an external pull-up resistor to pull the TXENABLE output high. In this state, a driver on another device may pull the signal low to enable the module.

The output state can be inverted from the current state using the control in MDIO register 1.D005h[1]. This allows the pin to be used as a generic GPIO pin in

other applications including the QT2025 device. See Table 17 for TXENABLE truth table logic..

Table 17: TXENABLE Logic[1]

Transmit Disable Control TXENABLE_TOPADB (1.0009h[0])	Low Power Mode Control [2] MDIO_PWDN == PMA_PWDN or PCS_PWDN or XGXS_PWDN	TXON_FRPAD [3] 1.D002[0]	XFP 1.C301[11]	TXENABLE Driver State
1	1	1	0	Float (off)
0	0	x	1	Float (off)
0	1	x	1	Float (off)
1	0	0	1	Float (off)
1	1	0	1	Float (off)
1	0	1	1	Low (on)
1	1	1	1	Low (on)
0	0	0	0	Low (on)
0	0	1	0	Low (on)
0	1	0	0	Low (on)
1	0	0	0	Low (on)
0	1	1	0	Low (on)
1	0	1	0	Low (on)
1	1	0	0	Low (on)

1. The TXENABLE logic is given by: TXENABLE == [TXENABLE_TOPADB AND not(MDIO_PWDN) AND (TXON_FRPAD or XFP)] xor XFP
2. If any of the listed register fields is set to '1', it will set TXENABLE = 0. PMA_PWDN = 1.0000[11]; PCS_PWDN = 3.0000[11]; XGXS_PWDN = 4.0000[11]
3. This is the status of the TXON pad input. The status is reported in the MDIO noted register field.

Line Timing OK

The Line Timing OK (LTIMEOK) status pin is used in WIS applications where an external VXCO PLL circuit has been implemented, line timing is enabled and a fixed reference is not available on SREFCLK. The LTIMEOK pin is to be used to force the external VCXO to its center frequency when line timing conditions are not valid or line timing is disabled. When linetiming conditions are valid and linetiming is enabled, a logic HIGH on LTIMEOK indicates that the VCXO may lock to the Serial RX recovered clock. When linetiming conditions are not valid or line timing is disabled, a logic low on the LTIMEOK output pin will force the VCXO to its center frequency.

LED1/LED2/LED3 Drivers

The QT2025 incorporates three bidirectional I/Os whose primary application is as direct LED drivers in hostboard applications. They can also be used for general purpose input or output.

Each LED driver may be programmed to one of several different modes using the LED Configuration Registers 1.D006h, 1D007h and 1.D008h (for LED1, LED2 and LED3 respectively).

In 10Gbps operation, each LED can be programmed to indicate one of the following conditions:

RX or TX Link Status Only

RX or TX Activity Only

RX or TX Link Status and Activity

LED on

LED off

Each LED driver can be independently programmed to monitor either the transmit path or the receive path, controlled by bit 3 of the LED Configuration Registers.

'Link Status' Definition

The link status is monitored independently for the transmit and receive paths as follows:

Tx Link Status == XAUI Lane Align (4.18h bit 12)

Rx Link Status == PCS block_lock (3.21h bit 15)

The 'Link Status' monitor for driving the LEDs is only available in 10Gbps operation. It is provided by a hardware circuit in the PHY. This capability is not available in 1.25Gbps operation.

'Activity' Definition

A packet activity event is generated when the packet start code ||S|| is detected in the PCS encoder for transmit path or in the PCS decoder for the receive path.

The 'Activity' monitor is only available in 10Gbps operation. It is provided by a hardware circuit in the PHY. This capability is not available in 1.25Gbps operation.

In 'Activity' mode the LED will be off normally and flash on for 50 or 100ms on at each activity event, and will be subsequently turned off for 25 or 50ms. Any packet activity events that occur before the LED toggle cycle finishes will be ignored. Figure 41 on page 73 shows the LED stretching behavior for activity only mode.

In 'Link Status / Activity' mode the LED is ON to indicate the link is up and OFF to indicate the link is down. When the link is up, the LED will turn off for 25 or 50ms for each activity event, and will be subsequently turned on for 50 or 100ms. Any packet activity events that occur before the LED toggle cycle finishes will be ignored. Figure 42 on page 73 shows the LED stretching behavior for link/activity combined mode.

The stretch time is controlled by bit 4 of the LED Configuration Registers. This determines the amount of time the LED will flash on during a packet activity event. When set to a 0 (default) the stretch time is 50ms; when set to a 1, the stretch time is 100ms. The time the LED is turned off during the packet activity event is equal to half the stretch time.

When in 'Link Status Only' mode, the LED is OFF when the link is down. The LED is ON when the link is up.

The LED driver pins are open drain circuits (10mA max current rating). When the LED is ON, the driver pin is driven low (control register bits 2:0 = '101'). When the LED is OFF, the driver pin is high impedance (control register bits 2:0 = '100').

The LED driver polarity can be controlled independently for each pin[1]. This allows the logic to be inverted. Polarity control is provided by the LED1_POL, LED2_POL and LED3_POL register fields.

LED Default Settings

LED1: Rx 'Link Status and Activity'

LED2: Tx 'Link Status and Activity'

LED3: Rx 'Link Status Only'

The LED2 pin is also used to enable one-byte' direct addressing on the EEPROM_SDA/EEPROM_SCL bus. To enable this feature, the LED2 pin is held low during a hard reset (using RESETN pin).

LED Usage in 1.25Gbps Operation

The Link Status and Activity monitoring capabilities are not available in 1.25Gbps operation. The LEDs may be turned on or off through register access.

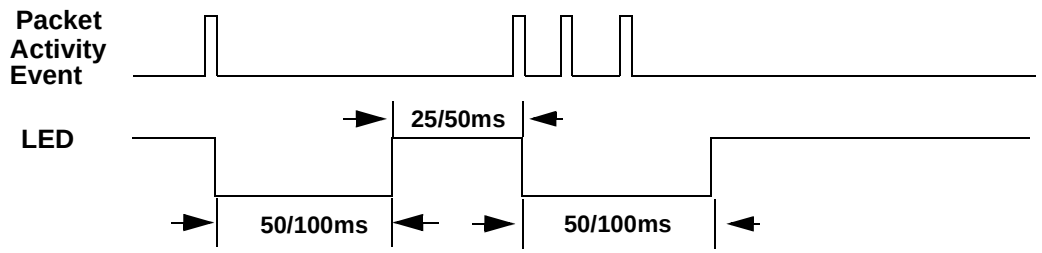
Firmware vs. Hardware Control

There is an option to allow firmware control of the LEDs, which is valid in both 10Gbps and 1.25Gbps operation. The firmware controls the LEDs by actively writing to the LED Configuration registers and toggles the LEDs between the "On" and "Off" states. When firmware control is enabled it will overwrite any value programmed in a configuration register on the next state change. The firmware is not capable of Activity detection.

The firmware default settings are different from the hardware defaults. Consult the Firmware Release Notes for details.

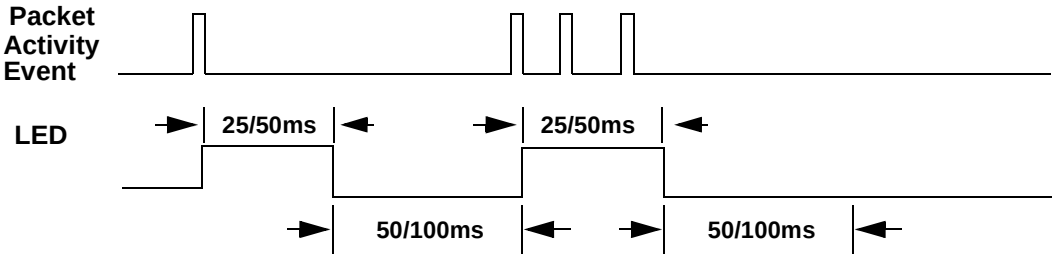
1. This is a new feature in the Rev. D product.

Figure 41: LED Timing for 'Activity Only' Mode



Note: The direct drive LED output in this diagram is shown as active low

Figure 42: LED Timing for 'Link Status/Activity' Mode

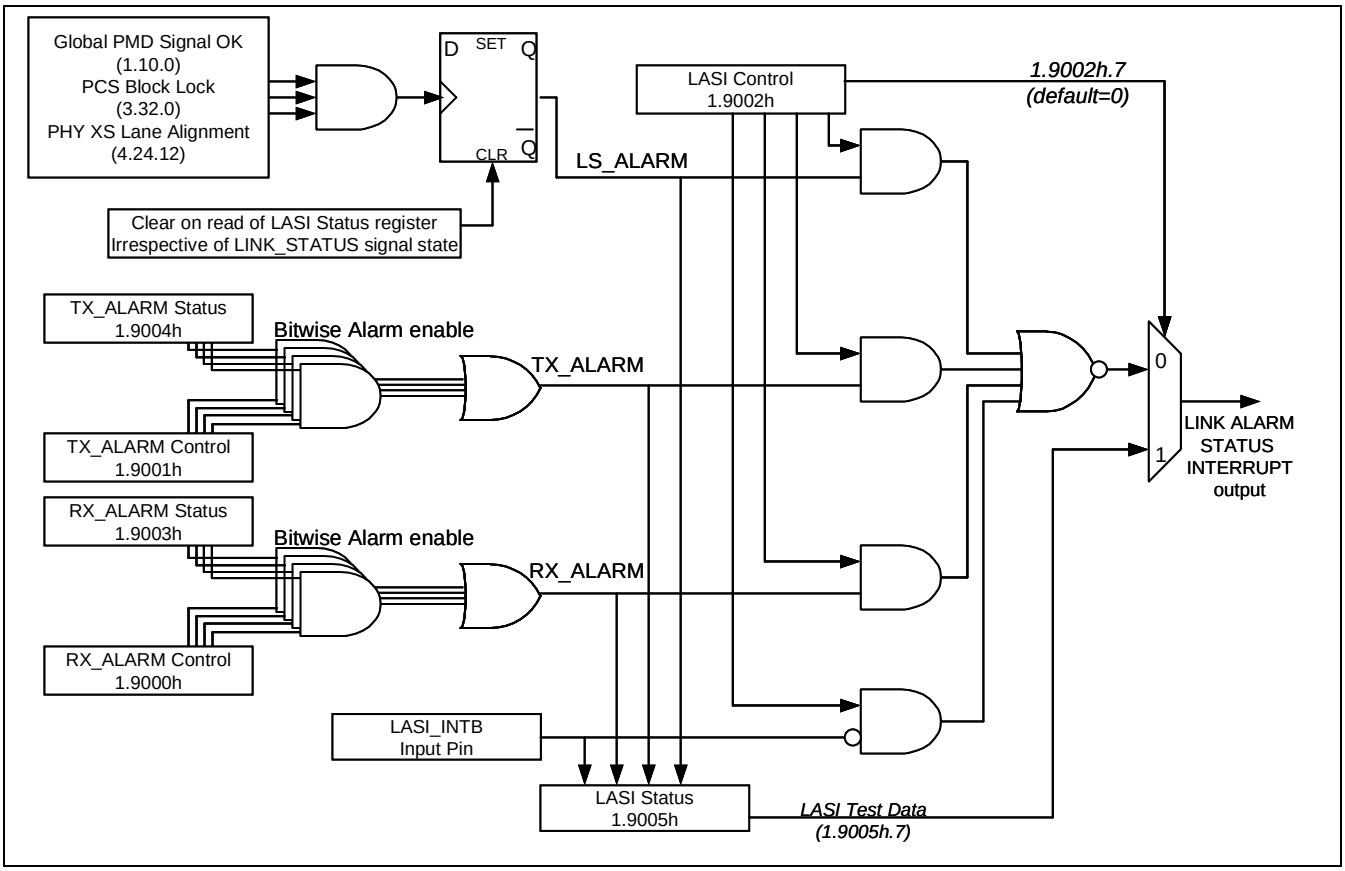


Note 1) : This assumes the link is up
2) : The direct drive LED output in this diagram is shown as active low

Link Alarm Status Interrupt Pin (LASI)

The LASI pin is an active-low output used to indicate that a link fault condition has been detected in either the receive or transmit paths. It can be used as an interrupt to a microcontroller. The block diagram for LASI is shown in Figure 57. Control registers are provided so LASI can be programmed to assert only for specific fault conditions.

Figure 43: LASI Block Diagram



LASI = {OR of (reg 1.9005h.n 'bit wise AND' reg 1.9002h.n) for n=0..15}, where register 1.9005h contains the alarm states, and register 1.9002h contains the enable bits for each alarm.

LASI Usage in 1.25Gbps Operation

Most of the alarms that propagate into LASI are generated only in the 10Gbps datapath. For these alarms, there is no equivalent when the PHY is operating in 1.25Gbps mode. This includes but is not limited to all device-specific Local Fault alarms (e.g. PMA Receive Local Fault). The following LASI functions are valid in 1.25Gbps mode:

- LASI_TST_DATA
- LASI_INTB
- rx_flag
- tx_flag
- Receive Optical Power Fault (1.9003.5)
- Laser Output Power Fault (1.9004.7)
- Laser Temperature Fault (1.9004.8)
- Laser Bias Current Fault (1.9004.9)

LASI_TST_DATA

Register bit 1.9005h.7 is a writable LASI_TST_DATA register bit which can be used to test the LASI pin connectivity. It is enabled by setting LASI_TST_EN (register bit 1.9002h.7) to 1. When enabled, the LASI output state will be determined by the LASI_TST_DATA value. This feature is used by firmware to indicate a module insert or removal event.

Table 18: LASI Control Registers

Description	MDIO Status Register		MDIO Enable Register	
	16b hex	type	16b hex	default value
LS_ALARM	1.9005.0	RO/LH	1.9002.0	0
TX_ALARM	1.9005.1	RO	1.9002.1	0
RX_ALARM	1.9005.2	RO	1.9002.2	0
LASI_INTB interrupt	1.9005.3	RO	1.9002.3	0
unused	1.9005.4	RO	1.9002.4	0
unused	1.9005.5	RO	1.9002.5	0
unused	1.9005.6	RO	1.9002.6	0
LASI_TST_DATA	1.9005.7	R/W	1.9002.7	0
unused	1.9005.f:8	RO	1.9002.f:8	0

Link State Alarm (LS_ALARM)

The LS_ALARM signal is a 10Gbps-specific alarm that is latched high each time any of the following signals changes state:

- PMD signal detect (MDIO 1.10.0)
- PCS block_lock (MDIO 3.32.0)
- PHY_XS lane alignment (MDIO 4.24.12)

This alarm is not active in 1.25Gbps mode.

RX_ALARM

RX_ALARM is used to indicate that a fault has occurred on the receive path. RX_ALARM is the bitwise OR of the receive path status register bits in register 1.9003h. RX_ALARM can be programmed to assert only when specific receive path fault conditions are present. The programming is performed by writing to a mask register at address 1.9000h. The contents of register 1.9003h is AND'ed with register 1.9000h prior to application of the OR function to generate the RX_ALARM signal.

RX_ALARM = {OR of (reg 1.9003.n 'bit wise AND' reg 1.9000.n) for n=0..9})

Table 19: Receive Alarm Registers (RX_ALARM)

Description	Definition		MDIO Status Register (RO)		MDIO Enable Register (R/W)	
	LEGACY=0	LEGACY=1	16b hex	type	16b hex	default value
PHY_XS Receive Local Fault (MDIO 4.8.10 = 1.0008.a h)	*NOT (XAUI PLL locked)*		1.9003.0	RO/LH	1.9000.0	1
rx_flag	bitwise OR of *rx_flag* register, 1.9007h		1.9003.1	RO/LH	1.9000.1	0
PCS Receive Code Violation	*invalid 66b code word detected*		1.9003.2	RO/LH	1.9000.2	0
PCS Receive Local Fault	*NOT(block_lock)* (linked to 3.8.10)		1.9003.3	RO/LH	1.9000.3	1
PMA Receive Local Fault	*NOT(Receive PLL Lock)* (linked to 1.8.10)	*NOT(Receive PLL Lock) or RXLOSB_I==0* (linked to 1.8.10)	1.9003.4	RO/LH	1.9000.4	1
Receive Optical Power Fault [1]	*1.A071h.7 OR 1.A071h.6*	Reserved, RO	1.9003.5	RO	1.9000.5	1, LEGACY=0 0, LEGACY=1
PHY_XS Receive Rate Error	*Receive FIFO overflow/underflow error* (4.C002h.7 OR 4.C002h.6)		1.9003.6	RO/LH	1.9000.6	0
WIS Alarm Interrupt Flag [2]	bitwise OR of *WIS ALARM INTERRUPT* register, 2.33 (2.21h)		1.9003.7	RO	1.9000.7	0
WIS Extended Alarm Interrupt Flag [2]	bitwise OR of *WIS EXTENDED ALARM INTERRUPT* register, 2.C502h		1.9003.8	RO	1.9000.8	0
WIS Local Fault [2]	*NOT(SONET frame sync)* (linked to 2.1.7)		1.9003.9	RO/LH	1.9000.9	0
Reserved, set to 0			1.9003.f:a	RO	1.9000.f:a	0

1. undefined if LEGACY = 1.
2. Valid in WAN mode only.

rx_flag Alarm Register

rx_flag is used to flag a DOM receive alarm.

rx_flag = {OR of (reg 1.A071.n 'bit wise AND' reg 1.9007.n) for n=0 to 7}

Table 20: rx_flag Alarm Registers

Description	MDIO Status Register (RO,LH)	MDIO Enable Register (R/W)	MDIO Enable Register default value
Receive Optical Power High Alarm	1.A071h.7	1.9007h.7	0
Receive Optical Power Low Alarm	1.A071h.6	1.9007h.6	0
rx_flag alarm bits 0 through 5 *[1]	1.A071h.5:0	1.9007h.5:0	0

1. rx_alarm bits 0 through 5 are read from the DOM device and mapped to registers 1.A071h.5:0. The function of these bits is not specifically defined in the XENPAK MSA, but they are used in generating the rx_flag signal in order to allow for vendor specific alarms to be defined. These alarms should be disabled via the associated MDIO register bits 1.9007.5:0 when not is use.

TX_ALARM

TX_ALARM is used to indicate that a fault has occurred on the transmit path. TX_ALARM is the bitwise OR of the transmit path status register bits in register 1.9004h. TX_ALARM can be programmed to assert only when specific transmit path fault conditions are present. The programming is performed by writing to a mask register at address 1.9001h. The contents of register 1.9004h is AND'ed with register 1.9001h prior to application of the OR function to generate the TX_ALARM signal.

tx_alarm = {OR of (reg 1.9004.n 'bit wise AND' reg 1.9001.n) for n=0..10}

Table 21: Transmit Alarm Registers (TX_ALARM)

Description	Alarm Definition		MDIO Status Register (RO)		MDIO Enable Register (R/W)		
						default	
	LEGACY=0	LEGACY=1	16b hex	type	16b hex	LEGACY =0	LEGACY 1
PHY_XS transmit local fault	*NOT(TxXAUI Lane Align)* (linked to 4.8.11)	*NOT(TxXAUI CDR lock<3:0>)* (linked to 4.8.11)	1.9004.0	RO/LH	1.9001.0	1	
tx_flag	bitwise OR of *tx_flag* register, 1.9006h		1.9004.1	RO/LH	1.9001.1	0	
PHY_XS transmit rate error	*Transmit FIFO overflow/underflow error* (4.C002h.9 OR 4.C002h.8)		1.9004.2	RO/LH	1.9001.2	0	
PCS transmit local fault (MDIO 3.8.11)	*Transmit FIFO overflow/underflow error* (linked to 3.8.11)	*NOT(TxXAUI Lane Sync) or NOT (TxXAUI Lane Align)* (linked to 3.8.11)	1.9004.3	RO/LH	1.9001.3	1	

Table 21: Transmit Alarm Registers (TX_ALARM) (Continued)

Description	Alarm Definition		MDIO Status Register (RO)		MDIO Enable Register (R/W)		
						default	
	LEGACY=0	LEGACY=1	16b hex	type	16b hex	LEGACY =0	LEGACY 1
PMA transmit local fault	*Transmit PLL not locked* (linked to 1.8.11)	*(Transmit PLL not locked) OR (TXFAULT)* (linked to 1.8.11)	1.9004.4	RO/LH	1.9001.4	1	
latched version of $\overline{\text{txlock}}$	*NOT(Fiber transmit PLL locked)* (reflects value in 1.C001h.0)		1.9004.5	RO/LH	1.9001.5	0	
latched version of TXFAULT (based on input pin)	*TXFAULT*		1.9004.6	RO/LH	1.9001.6	0	1
Laser Output Power Fault [1]	*DOM alarm 1.A070h.1:0*	Reserved, RO	1.9004.7	RO	1.9001.7	1	n/a
Laser Temperature Fault [1]	*DOM alarm 1.A070h.7:6*	Reserved, RO	1.9004.8	RO	1.9001.8	1	n/a
Laser Bias Current Fault [1]	*DOM alarm 1.A070h.3:2*	Reserved, RO	1.9004.9	RO	1.9001.9	1	n/a
PHY_XS code error	*TxXAUI invalid 8b/10b code word detected* (logical OR of 4.C006h.3:0)		1.9004.a	RO/LH	1.9001.a	0	
reserved, set to 0			1.9004.f:b	RO	1.9001.f:b	n/a	

1. undefined if LEGACY = 1.

tx_flag Alarm Register

tx_flag is used to flag a DOM transmit alarm.

tx_flag = {OR of (reg 1.A070.n 'bit wise AND' reg 1.9006.n) for n=0 to 7}

Table 22: tx_flag Alarm Registers

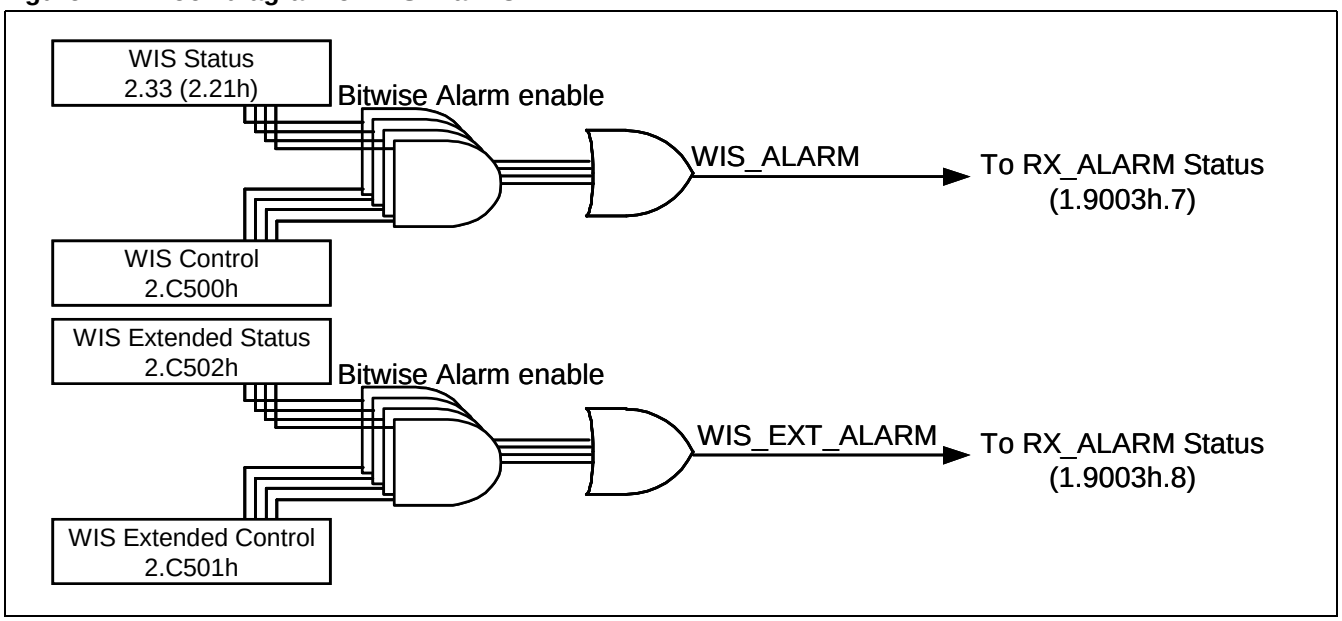
Description	MDIO Status Register (RO/ LH)	MDIO Enable Register (R/W)	MDIO Enable Register default value
Transmit Temperature High Alarm	1.A070h.7	1.9006h.7	0
Transmit Temperature Low Alarm	1.A070h.6	1.9006h.6	0
tx_*flag* alarm bits 4 and 5 [1]	1.A070h.5:4	1.9006h.5:4	0
Laser Bias Current High Alarm	1.A070h.3	1.9006h.3	0
Laser Bias Current Low Alarm	1.A070h.2	1.9006h.2	0
Laser Output Power High Alarm	1.A070h.1	1.9006h.1	0
Laser Output Power Low Alarm	1.A070h.0	1.9006h.0	0

1. tx_alarm bits 4 through 5 are read from the DOM device and mapped to registers 1.A070h.5:4. The function of these bits is not specifically defined in the XENPAK MSA, but they are used in generating the tx_flag signal in order to allow for vendor specific alarms to be defined. These alarms should be disabled via the associated MDIO register bits 1.9006h.5:4 when not is use.

WIS Alarms

When operating the QT2025 in WAN mode, additional WIS alarms can be programmed to assert LASI. These alarms are used to report a WIS-related link fault on the receive path. The block diagram for the WIS alarms is shown in Figure 58. The alarms feed into RX_ALARM.

Figure 44: Block diagram of WIS Alarms



WIS_ALARM

WIS_ALARM is used to indicate that a WAN-related fault has occurred on the receive path. WIS_ALARM is the bit-wise OR of the WIS Status 3 Register bits in register 2.21h. WIS_ALARM can be programmed to assert only when specific receive path fault conditions are present. The programming is performed by writing to a mask register at address 2.C500h. The contents of register 2.21h is AND'ed with register 2.C500h prior to application of the OR function to generate the WIS_ALARM signal.

WIS_ALARM = {OR of (reg 2.21h.n 'bit wise AND' reg 2.C500.n) for n=0..11}

Table 23: WIS Status 3 Register (WIS_ALARM)

Description	Definition	MDIO Status Register (RO)		MDIO Enable Register (R/W)	
		16b hex	type	16b hex	default value
LOP-P	Loss of Pointer	2.21.0	RO/LH	2.C500.0	0
AIS-P	Alarm Indication Signal	2.21.1	RO/LH	2.C500.1	0
PLM-P	Loss of Label Mismatch	2.21.2	RO/LH	2.C500.2	0
LCD-P	Path Loss of Cell Delineation	2.21.3	RO/LH	2.C500.3	0
AIS-L	Line Alarm Indication Signal	2.21.4	RO/LH	2.C500.4	0
RDI-L	Line Remote Defect Indication	2.21.5	RO/LH	2.C500.5	0
LOS	Loss of Signal (based on no transitions as described in ANSI T1.416-1999)	2.21.6	RO/LH	2.C500.6	0
LOF	Loss of Frame	2.21.7	RO/LH	2.C500.7	0
Reserved, set to 0		2.21.8	RO	2.C500.8	0
Far End AIS-P/LOP-P	Far-end Alarm Indication Signal	2.21.9	RO/LH	2.C500.9	0
Far End PLM-P/LCD-P	Far-end Loss of Label Mismatch	2.21.a	RO/LH	2.C500.a	0
SEF	Severely Errored Frame	2.21.b	RO/LH	2.C500.b	0
Reserved, set to 0		2.21.f:c	RO	2.C500.f:c	0

WIS_EXT_ALARM

WIS_EXT_ALARM is used to indicate that a WAN-related fault has occurred on the receive path. WIS_EXT_ALARM is the bitwise OR of the WIS Extended Alarms Status Register bits in register 2.C502h. WIS_EXT_ALARM can be programmed to assert only when specific receive path fault conditions are present. The programming is performed by writing to a mask register at address 2.C501h. The contents of register 2.C502h is AND'ed with register 2.C501h prior to application of the OR function to generate the WIS_ALARM signal.

WIS_ALARM = {OR of (reg 2.C501h.n 'bit wise AND' reg 2.C502.n) for n=0..11}

Table 24: WIS Extended Alarms Status Register (WIS_EXT_ALARM)

Description	Definition	MDIO Status Register (RO)		MDIO Enable Register (R/W)	
		16b hex	type	16b hex	default value
K1 Validated Byte Flag	Incorrect K1 Validated Byte	2.C502.0	RO/LH	2.C501.0	0
K2 Validated Byte Flag	Incorrect K2 Validated Byte	2.C502.1	RO/LH	2.C501.1	0
Received Inconsistent K1 Bytes Flag	Received Inconsistent K1 Bytes	2.C502.2	RO/LH	2.C501.2	0
Received Inconsistent K2 Bytes Flag	Received Inconsistent K2 Bytes	2.C502.3	RO/LH	2.C501.3	0
S1 Validated Byte Flag	Incorrect S1 Validated Byte	2.C502.4	RO/LH	2.C501.4	0
Reserved	Reserved	2.C502.5	RO	2.C501.5	0
Received New J0 Trace Message Flag	New J0 Trace Message detected	2.C502.6	RO/LH	2.C501.6	0
Received New J1 Trace Message Flag	New J1 Trace Message detected	2.C502.7	RO/LH	2.C501.7	0
SD Alarm Flag	Detected Signal Degrade Alarm	2.C502.8	RO/LH	2.C501.8	0
SD Timing Window Expired Flag	Signal Degrade Timing Window Expired	2.C502.9	RO/LH	2.C501.9	0
SF Alarm Flag	Detected Signal Fail Alarm	2.C502.a	RO/LH	2.C501.a	0
SF Timing Window Expired Flag	Signal Fail Timing Window Expired Flag	2.C502.b	RO/LH	2.C501.b	0
Reserved		2.C502.f:c	RO	2.C501.f:c	0

Embedded Micro-controller

The QT2025 integrates an 8051 micro-controller which provides a flexible efficient environment in which to control the EDC algorithms and associated monitor functions.

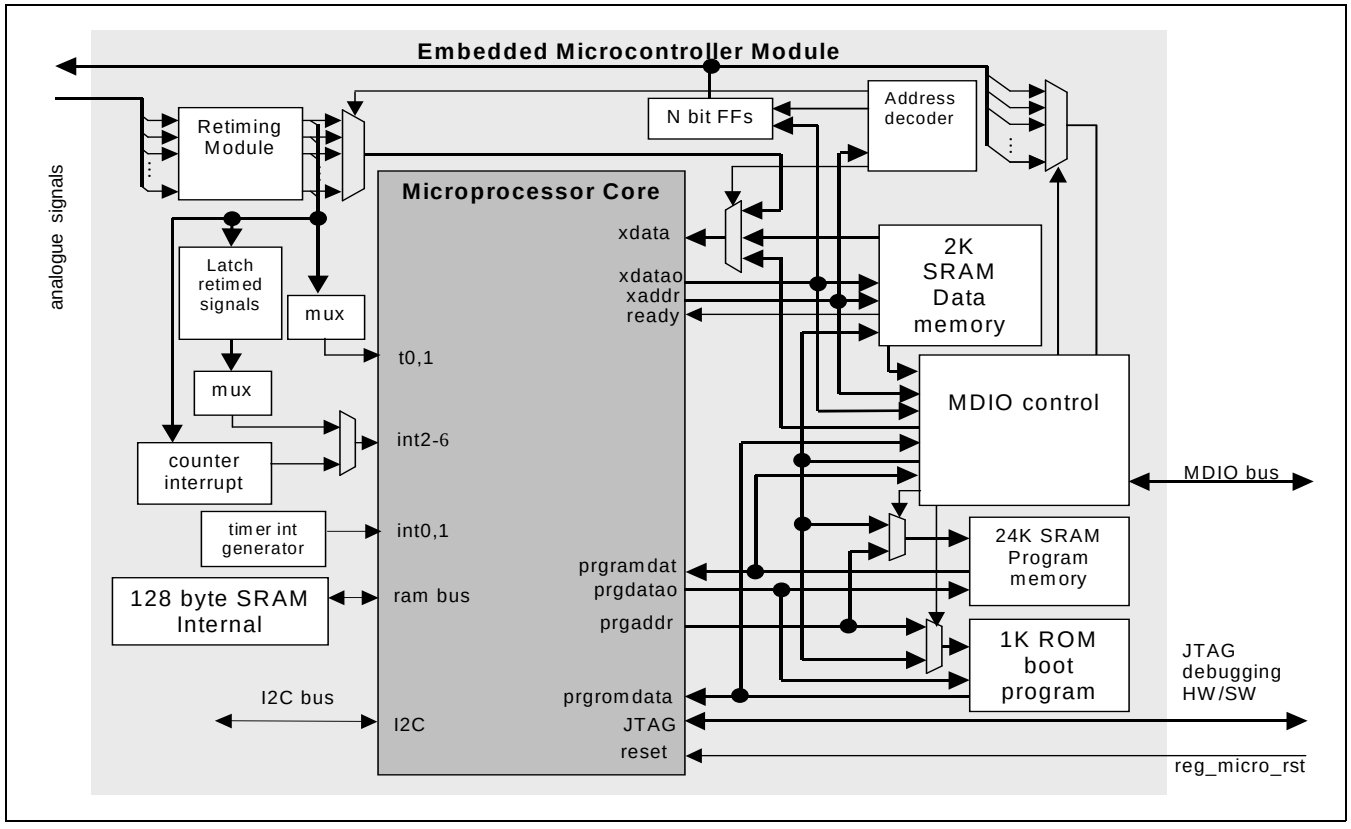
Micro-controller Architecture

Figure 45 depicts the embedded microcontroller core and its peripherals in the QT2025. It includes one internal memory (128 byte), one data memory (2k) and 2 program memories (1k Boot ROM & 24K SRAM). The 24k SRAM program memory is programmable using the I2C or MDIO bus.

The micro-controller runs at a nominal clock frequency of 156.25MHz. This clock frequency can be modified via register 1.C302h[4:2] to run from 9 - 312.5MHz. The embedded micro-controller (also referred to as the “CPU”) is primarily used for initial device configuration and EDC algorithm control and scheduling.

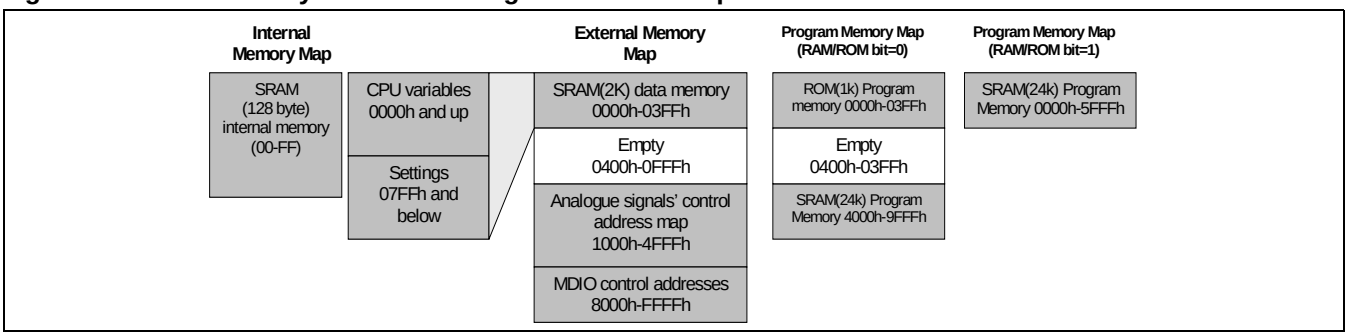
Within this section, “external” signals refer to signals that are external to the microcontroller block.

Figure 45: Micro-controller Architecture



Memories

Figure 46: 8051 Memory and Control Signal Address Map



Memory is organized as follows:

- 128 byte internal memory. Required by the micro for internal use (including stack). This memory is connected only to the micro but can be accessed through the MDIO bus.
- 24[1] kbytes SRAM program memory. This memory can be programmed through I2C and MDIO bus and is disabled when ROM is used as program memory.
- 1 kbytes ROM program memory. The ROM contains AMCC-specific hard-coded programming for device management and EDC adaptation.

At boot time, the ROM-resident program checks for a valid, alternative code image in the external 32k EEPROM. If an alternative image is found, the external 32kB EEPROM code is loaded into the SRAM and executed. The micro can be programmed to bypass the EEPROM check and run directly from internal SRAM.

Microcontroller I/O

The embedded micro-controller has the following I/O capabilities:

- **I2C Interface.** The CPU can become an I2C bus master to allow it to read/write to any external I2C peripheral.
- **MDIO Registers.** The CPU has full read/write access to all on-chip MDIO registers, effectively allowing it to control the entire device.
- **Mailbox Registers.** These registers, in MDIO space, allow messages to be passed to the CPU.
- **General Purpose I/O.** The 8051 core has access to the General Purpose I/O pins which can be used as either simple I/O or as interrupt inputs.

1. Version A of the device provided only 16 Kbytes of SRAM.

Program Execution

The QT2025 firmware may be stored in an external 32kB EEPROM or written directly into SRAM via the MDIO bus. If MDIO register 3.E854h[6] is set to 0b, the micro-controller fetches and runs a boot sequence from the Boot ROM program memory. This boot sequence downloads the firmware program from the external EEPROM via the µC_SCL/SDA I2C interface. Once completed, the micro-controller sets a hardware control bit that resets the CPU and disables the ROM. After the micro comes out of this self-imposed reset it now sees the SRAM as the main program memory and starts executing the firmware program. The equivalent boot sequence is performed by setting 1.C300 bit 1 to '1'.

However, if 3.E854[6] is set to 1b the microcontroller will start running directly from SRAM, using any code previously written there.

The main firmware program is written and supplied by AMCC. Two files are available:

- MDIO Hex file which is to be loaded via the MDIO interface.
- EEPROM hex file which is to be loaded from the external 32kB EEPROM.

Note that the MDIO and EEPROM hex files are slightly different in they are optimized for their application. Additional startup details are available at the end of the Two Wire Interface section.

Program Memory Location

The 24kB of program memory space is accessible by MDIO. The first 16kB of memory is located in the address range 3.8000h - 3.BFFFh. The next 8kB of memory is located at 4.8000h - 4.9FFFh.

The supplied Intel .hex file must be written into this address space when using the MDIO programming option. The file must be written to memory beginning at address 3.8000h until address 3.BFFFh is reached. When memory offset 0x4000 is reached in the .hex file, the data must now be written starting at address 4.8000h.

Program upload from EEPROM automatically writes to the proper memory locations.

Management Data I/O (MDIO) Interface

The MDIO interface provides a simple, two wire serial interface to connect a station management entity (STA) and a managed PHY (aka: QT2025) for the purpose of controlling and monitoring the PHY. The MDIO protocol consists of the two-wire physical interface, a frame format, a protocol specification for exchanging the frames and a register set that can be read and written using these frames. The two wires of the physical interface are the Management Data Clock (MDC) and the Management Data I/O (MDIO).

The MDIO bus requires a valid LAN reference clock to be supplied to the EREFCLK input to operate the MDIO bus after reset is removed. The reference clock cannot be interrupted at any time during operation or a non-recoverable MDIO bus failure may occur. If the power is cycled or a hard reset is applied to the chip, the LAN reference clock must be present to re-initialize the bus.

MDIO Bus Speed

The MDIO interface supports a maximum bus rate of 25MHz. The maximum rate may also limited by the programmed clock rate for the internal microprocessor, such that the maximum bus speed equals the lesser of 25MHz or 1/5th the micro clock speed. The micro clock speed is set by the UC_CLK_SEL register field. The clock speed is set to a specific value that is determined by the requirements of the firmware load. Consult the Firmware Release Notes to determine the required clock speed.

Firmware for backplane applications use a reduced micro clock speed of 78.125MHz. This limits the MDIO bus speed to 15.625MHz.

As a rule, most other applications use the full-rate micro clock speed and support the maximum MDIO rate.

Users may wish to maximize the bus speed while programming the firmware microcode into memory. To use the full 25MHz bandwidth, set UC_CLK_SEL to 156.25MHz during programming. Reduce UC_CLK_SEL to the lower clock rate before starting code execution. The clock rate cannot be changed after code execution begins.

Clock Signal (MDC)

The MDC is sourced by the Station Management entity to the PHY as the timing reference for transfer of information on the MDIO signal. MDC is an aperiodic signal that has no maximum high or low times.

QT2025 MDC input pin has built-in hysteresis.

Data Signal (MDIO)

MDIO is a bidirectional signal between the PHY and the STA. It is used to transfer control and status information. Data is always driven and sampled synchronously with respect to MDC.

The MDIO can be configured as either open drain or a push-pull driver and meets electrical specifications as per IEEE 802.3-2005 Clause 45 (specifically Clause 45.4 Electrical Interface.)

MDIO Management Frame Format

The QT2025 has an internal Address register which is used to store the address for MDIO reads and writes. This MDIO Address register is set by sending a MDIO Register Address Command frame which specifies the register address to be accessed within a particular logical device.

After a Register Address Command frame has been sent, the following Write, Read or a Post-Read-Increment-Address Command frame to the same logical device accesses the register whose address is stored in the QT2025 MDIO Address register. A Register Address Command frame should be followed immediately by the associated Write, Read or Post-Read-Increment-Address Command frame.

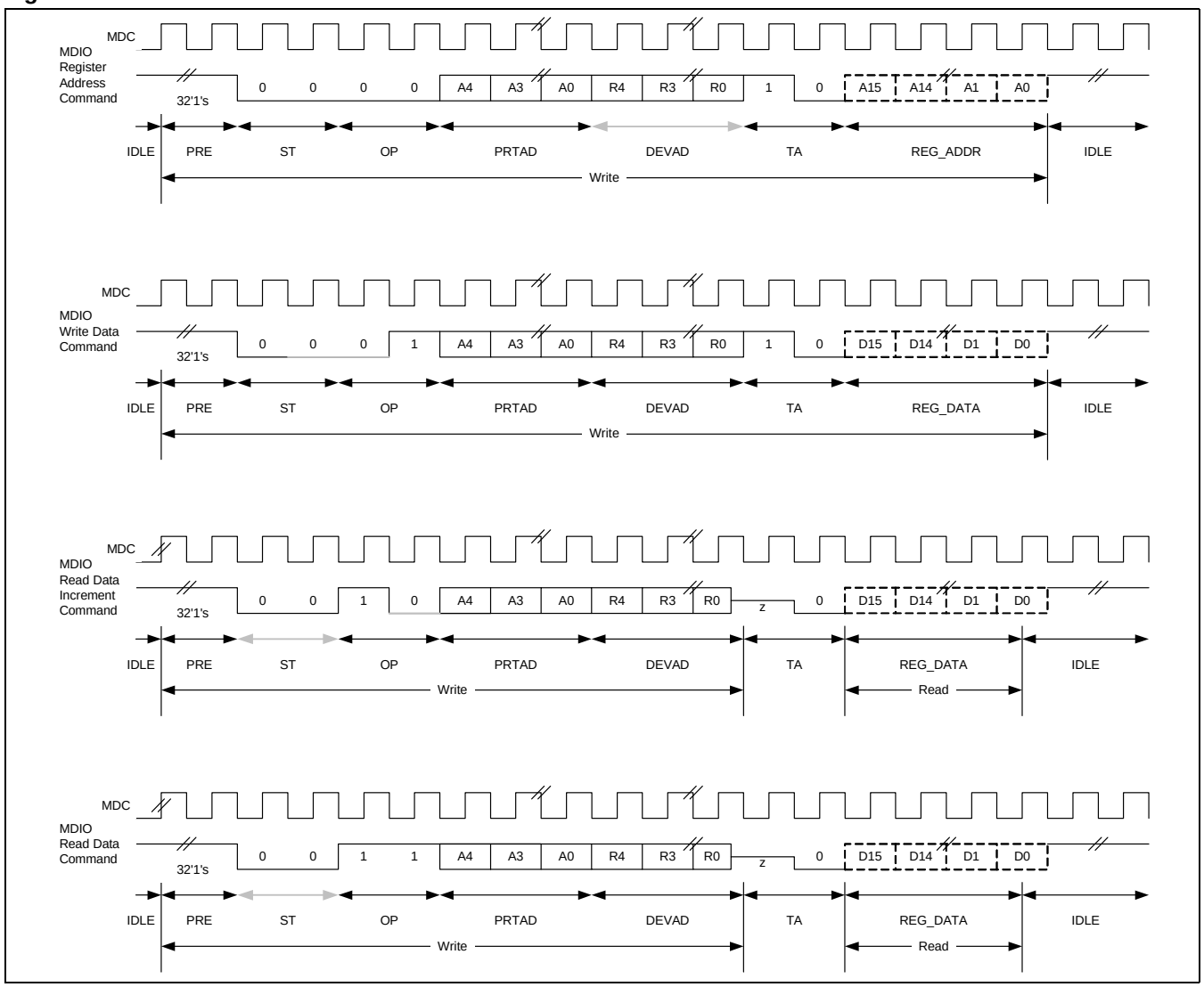
Upon receiving a Post-Read-Increment-Address Command frame and having completed the read operation, the QT2025 shall increment the stored address in the MDIO Register Address register. If no Register Address Command frame is received before the next Write, Read or Post-Read-Increment-Address Command frame, then the QT2025 shall use the incremented address currently stored in the Register Address register.

The Management Frame Format for Indirect Access is specified below in Figure .

Table 25: MDIO Management Frame Format

Management Frame Fields								
COMMAND FRAME	PRE	ST	OP	PRTAD	DEVAD	TA	REG_ADDR/DATA	IDLE
ADDRESS	1...1	00	00	PRTAD[4:0]	DA[4:0]	10	REG_ADDR[15:0]	Z
WRITE	1...1	00	01	PRTAD[4:0]	DA[4:0]	10	REG_DATA[15:0]	Z
READ-INC	1...1	00	10	PRTAD[4:0]	DA[4:0]	Z0	REG_DATA[15:0]	Z
READ	1...1	00	11	PRTAD[4:0]	DA[4:0]	Z0	REG_DATA[15:0]	Z

Figure 47: MDIO Frame Structure



Preamble Field (PRE)

At the beginning of each transaction the STA shall send a preamble sequence of 32 contiguous logic one bits on MDIO with 32 corresponding cycles on MDC, to provide the QT2025 with a pattern that it can use to establish synchronization. The QT2025 must observe this preamble sequence before it responds to any transaction

Start Field (ST)

The Start of Frame is indicated by a <00> pattern.

Operation Code Field (OP)

The Operation Code field describes the major function of the frame. Four frame types are supported, corresponding to the frames shown in Figure 47. The OP Codes for each frame type are shown below in Table 26.

Table 26: MDIO OP Code Definitions

OP Code	Operation
00	Register Address
01	Write Data
11	Read Data
10	Post Read Data + Increment

Port Address Field (PRTAD)

The Port Address is five bits, allowing 32 unique port addresses. The QT2025 port address is set through pins PRTAD<4:0>

Device Address Field (DEV_ADDR)

The Device Address is five bits, allowing 32 unique devices per port. The QT2025 supports device addresses 1 (PMA/PMD), 2 (WIS), 3 (PCS), and 4 (XGXS). This represents the first digit in the QT2025's register address notation (ex. 2.xxxxh for WIS)

Turnaround Field (TA)

The Turnaround time is a two bit time spacing between the Register Address field and the Data field of a management frame to avoid contention during a read transaction.

Register Data/Address Field (REG_DATA/REG_ADDR)

The Register Data/Address field is 16 bits. For the 'Register Address' frame, this field contains the register address. For all other field types, it contains the register data. The first bit transmitted/received is bit 15, MSB, and the last bit is bit 0, LSB.

Idle Field (IDLE)

The IDLE condition on MDIO is a high-impedance state. The open drain driver will be turned off and the external pull-up resistor will pull the MDIO line to a logic one.

MDIO Timing Relationship to MDC

MDIO is a bidirectional signal that can be sourced by the STA or the PHY. When the STA sources the MDIO signal, the STA shall provide a minimum of 10ns of setup time and a minimum of 10ns of hold time referenced to the rising edge of MDC. See Figure 48.

When the MDIO signal is sourced by the PHY, it is sampled by the STA synchronously with respect to the rising edge of MDC.

Open Drain Operation

When the MDIO driver is configured in open drain mode, an external pullup resistor to Vcc is required on the MDIO signal. When outputting a logic '1', the driver enters a high-Z state. The risetime is determined by the RC time constant of the bus. When outputting a logic '0', the driver actively pulls the signal low.

IEEE 802.3-2005 specifies a maximum Vcc of 1.5V, however the bus is 3.3V tolerant. A larger pullup resistor is required.

Push-Pull Operation

When configured in push-pull mode, the MDIO driver now actively drives a logic '1'. The risetime is fast and deterministic. It is not dependent on the bus RC time constant. No external pullup to Vcc is required.

Voh Voltage on VTERM

VTERM must be biased to a voltage in the range 1.2 - 3.3V for proper operation. In Push-Pull mode, the MDIO driver will drive a logic ‘1’ to the Voh voltage supplied to the VTERM input pin of the chip. If an external pullup on MDIO is present, then VTERM must be equal to or greater than the pullup voltage.

If VTERM is significantly less than Vpu, damage to the circuit may result.

In open drain mode, VTERM must still be biased. This prevents the push-pull circuitry from interfering with operation. The value of the voltage supplied to VTERM should be equal to or greater than the pullup voltage on MDIO.

Figure 48: MDIO/MDC Timing

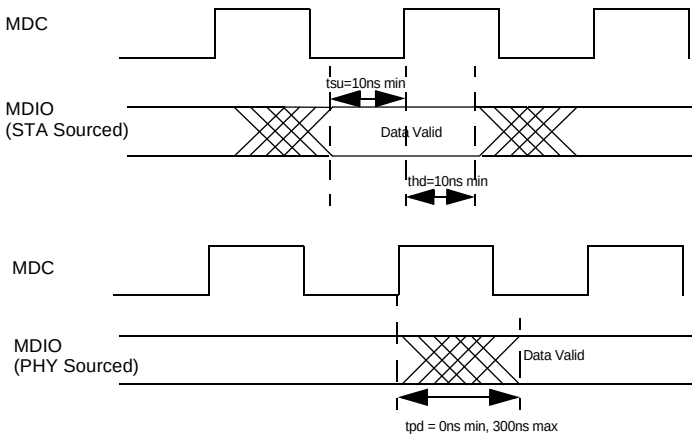
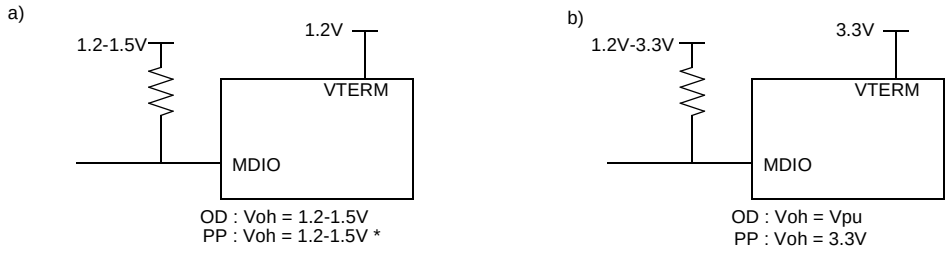


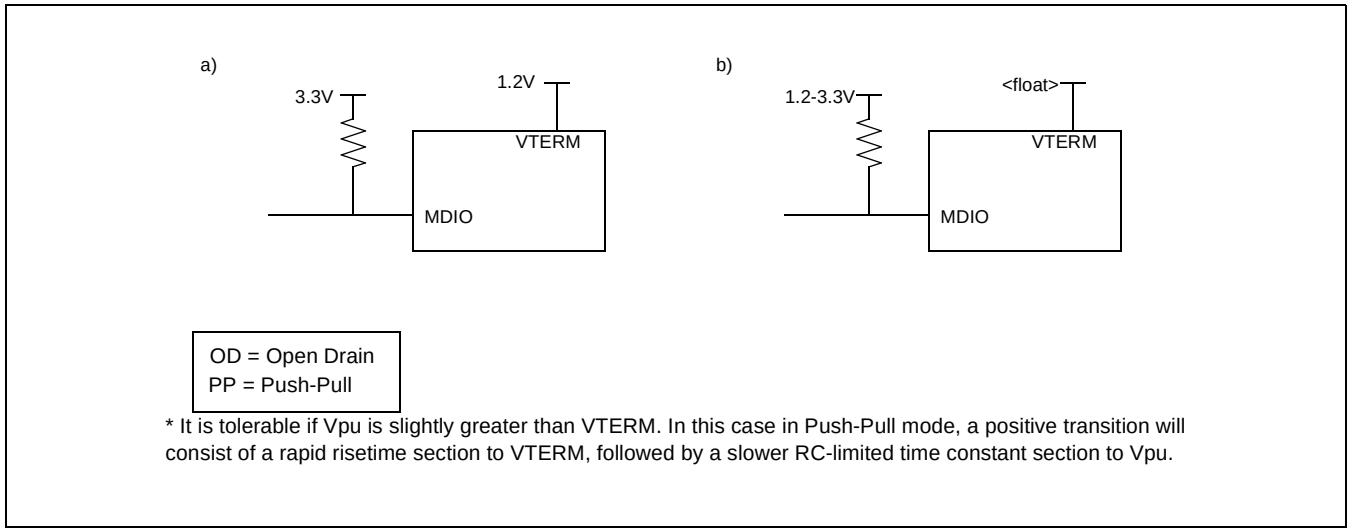
Figure 49: Valid MDIO Bias Schemes



OD = Open Drain
PP = Push-Pull

* It is tolerable if Vpu is slightly greater than VTERM. In this case in Push-Pull mode, a positive transition will consist of a rapid risetime section to VTERM, followed by a slower RC-limited time constant section to Vpu.

Figure 50: Invalid MDIO Bias Schemes



* It is tolerable if Vpu is slightly greater than VTERM. In this case in Push-Pull mode, a positive transition will consist of a rapid risetime section to VTERM, followed by a slower RC-limited time constant section to Vpu.

MDIO Configuration

Configuration of the MDIO driver mode is controlled by the 'MDIO_CFG' field located in MDIO register 1.C30Fh[8:6]. This allows selection between open drain or push-pull mode. As well, the internal termination can be selected. Available choices are 50kΩ pulldown to GND, 50kΩ pullup to Vcc or no internal resistive termination.

Default operation is open drain with no internal resistive termination.

XFP/SFP+ Module Access through MDIO

The MDIO interface can be used to access an XFP or SFP+ module. The XFP/SFP+ module 2-wire interface must be connected to the UC_SCL and UC_SDA clock and data lines. The XFP module address is 1010000, while the SFP+ module uses memory at addresses 1010000 and 1010001. The entire module address space will be automatically read upon powerup, reset or module hotplug by detection of the MOD_ABS signal. A 400ms delay is observed before upload to allow the module to initialize.

The memory at module address 1010000 is mapped to MDIO register range 3.D000 - 3.D0FFh. Read/write access to the module memory is controlled by MDIO register 3.D100h. This applies to both module types.

The memory at module address 1010001 is mapped to MDIO register range 1.8007 - 1.8106h. No read/write access to the module memory is provided.

Two Wire Interfaces

The QT2025 has two independent two wire control/ status interfaces listed below.

1. The EEPROM_I2C two wire interface (EEPROM_SCL/SDA).
2. A UC_I2C two wire interface (UC_SCL/SDA)

Two Wire Data Transfer Protocol

This section details the two-wire data transfer timing requirements. Separate timings are given for both 1-byte and 2-byte addressing mode.

Data Transfer

The data on the SDA line must be stable during the HIGH period of the clock SCL. The HIGH or LOW state of the data line can only change when SCL is LOW

Start and Stop Conditions

A HIGH to LOW transition on the SDA line while SCL is high defines a START condition. A LOW to HIGH transition on the SDA line while SCL is high defines a STOP condition. START and STOP conditions are generated by the QT2025 (master), not by the external devices (slaves).

Figure 51: Data Bit Transfer

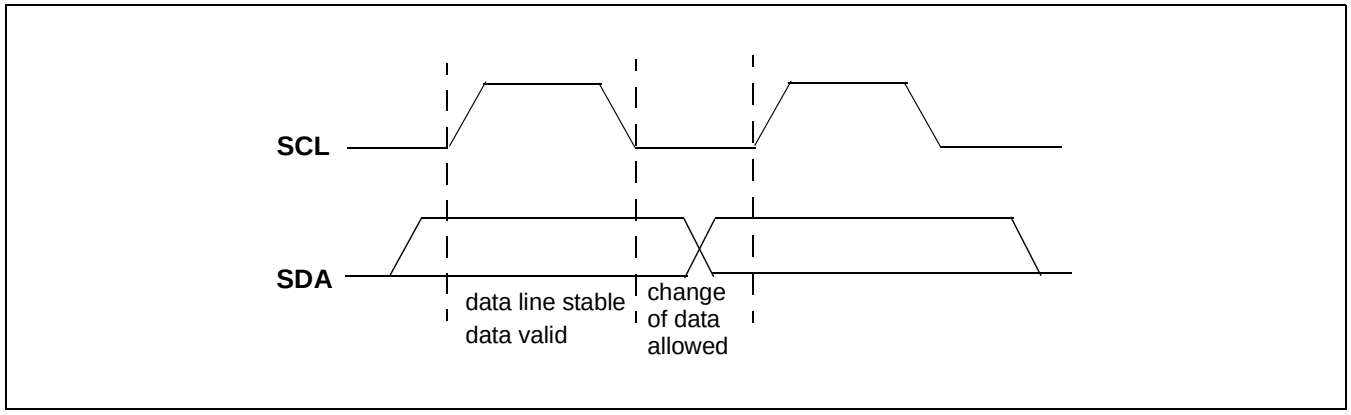
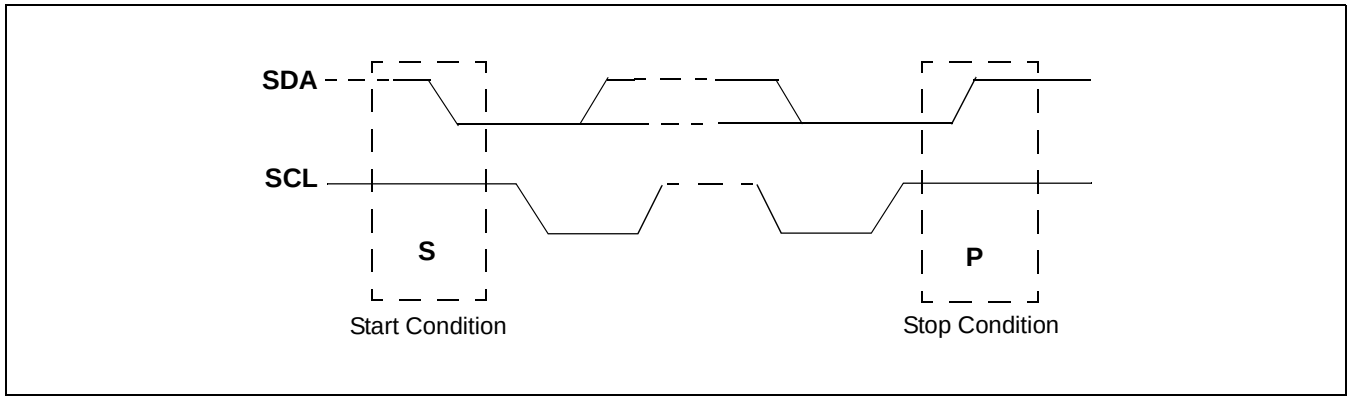


Figure 52: Start and Stop Conditions



Acknowledge

The transmitting device releases the SDA line after transmitting eight data or address bits. During the ninth cycle the receiving device pulls the SDA line low (“0”) to acknowledge that it has received the bits.

Bus Rate Control

The bus rate can be adjusted for both two wire interfaces independently. Table 27 details the configuration for bus rate control.

Figure 53: Acknowledge Condition

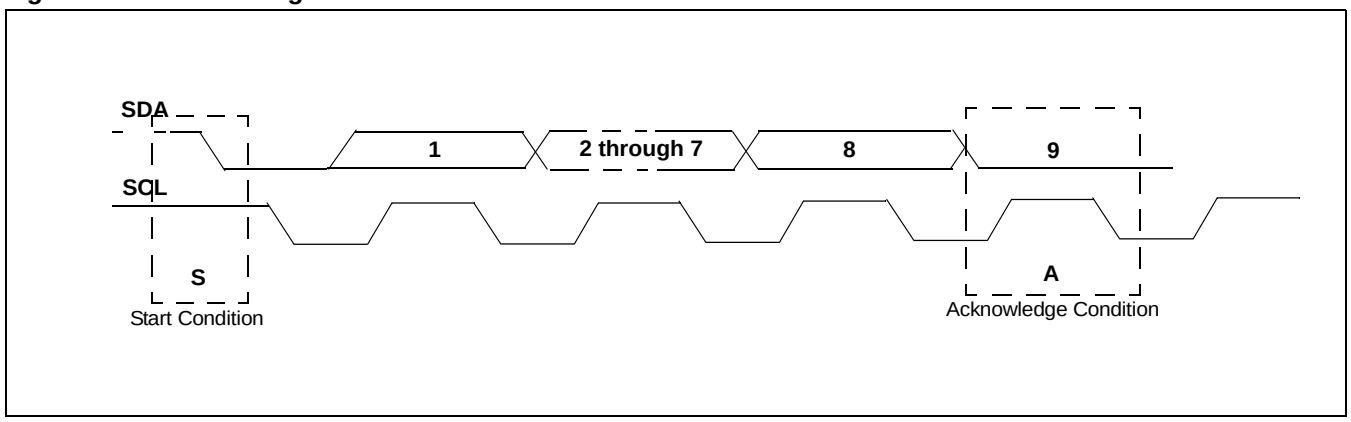


Table 27: Two-Wire Bus Rate Control Settings

Bus (Rate Select Register)	Register Setting	External Reference Clock	Two-Wire Bus Rate
EEPROM_I2C (NVR_BUS_RATE : 1.C003h[15:14])	00b (default)	156.25 MHz	100 kHz
		52.083 MHz	33 kHz
	01b	156.25 MHz	400 kHz
		52.083 MHz	133 kHz
UC_I2C (UC_I2C_DIV : 1.C316h[8:0])	0x13h (default)	156.25 MHz	400 kHz
		52.083 MHz	400 kHz
	0x4Dh	156.25 MHz	100 kHz
		52.083 MHz	100 kHz

UC_I2C Microcontroller Two Wire Interface

The UC_I2C microcontroller two wire interface (UC_SCL/SDA) is an industry standard serial two-wire interface that is directly connected to the internal microcontroller inside the QT2025. The internal microcontroller acts as the master on the bus to control external peripheral devices. This interface also supports multi-master mode through bus arbitration. The µC two-wire interface supports the following.

1. Loading microcontroller firmware stored in an external 32kB Firmware EEPROM
2. Control and status monitoring for XFP/SFP/SFP+ modules. These features are provided by firmware.

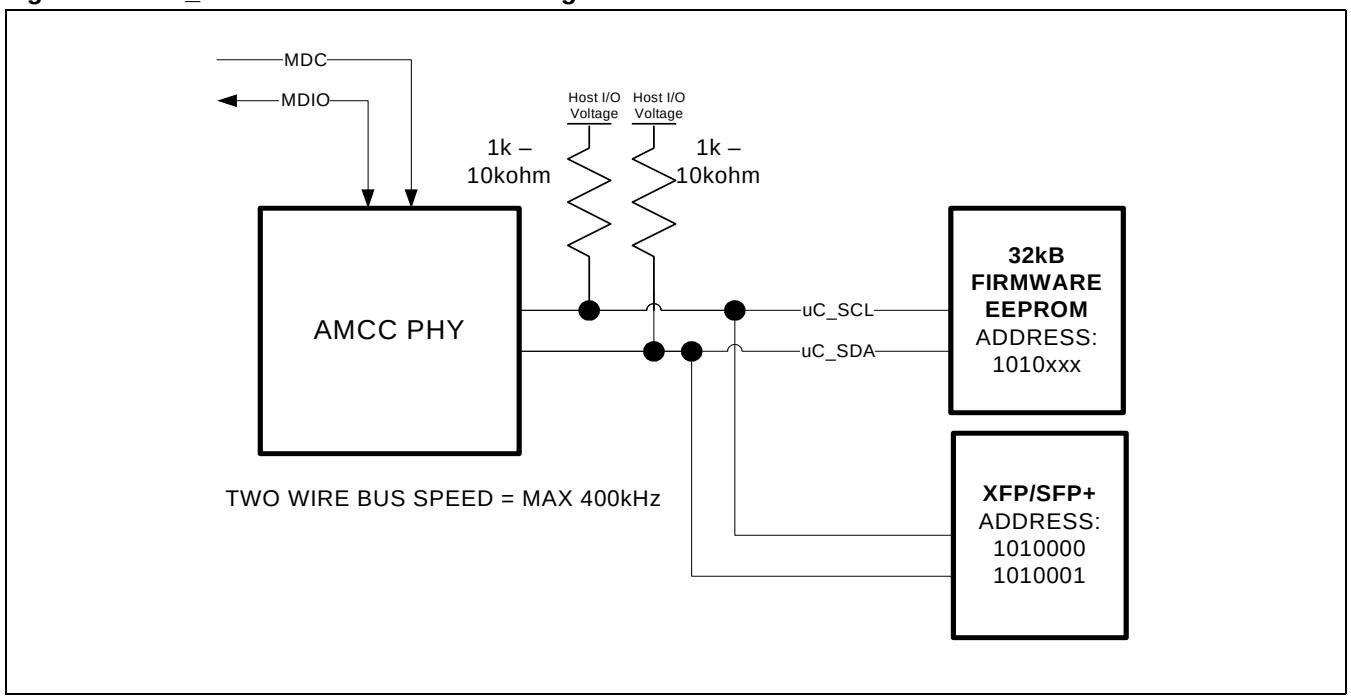
The microcontroller two wire interface consists of pins UC_SCL and UC_SDA. The logic levels for this interface are 0V and 1.2V however both pins are 3.3V tolerant. The UC_SCL output clock is only active when accessing one of the slave devices on the bus. The default clock rate is 400kHz (derived from the microcontroller reference clock of 156.25MHz). The bus frequency can be decreased to 100kHz by configuring register 1.C316h[15:0]=004Dh. Clock stretching is supported on this interface.

Both the UC_SCL and UC_SDA pins are open-drain outputs and therefore require a pullup resistor to a voltage level that is compatible with both the QT2025 and the slave devices. The value of the pullup resistor should be in the range from 1kΩ to 10kΩ. UC_SDA and UC_SCL pins may be wire OR'ed with other open drain two wire devices.

UC_SCL is an output during normal operation. When the UC_SCL clock signal is inactive, it is in a high impedance state.

Figure 54 shows a typical configuration for the UC_I2C two-wire interface.

Figure 54: UC_I2C Two-Wire Interface Configuration



Firmware EEPROM

The Firmware EEPROM is used to store the supplied microcontroller code. Firmware can also be downloaded directly to the QT2025 from the host controller over the MDIO interface, making the Firmware EEPROM optional.

The slave address for the Firmware EEPROM is configurable in register field UC_I2C_SLV_ADDR (1.C318[6:0]). Data is stored in single byte words and addressed using two-byte addressing. On startup or when a manual upload is initiated, each of the external Firmware EEPROM device registers is copied into the internal SRAM code space of the microcontroller.

After the hard reset is released, there are separate parameters that **must be set** in order for the Firmware EEPROM upload to proceed. Consult AMCC firmware-related documentation for details.

On startup, once the QT2025 chip is released from hard reset (by driving the RESETN pin high), the internal microcontroller will remain in reset as long as MDIO register field MICRO_RESETN=0 (1.C300h[1]). Once MICRO_RESETN=1, the microcontroller is released from reset the programmed parameters are used to control the microcode upload from the Firmware EEPROM.

There are two options for programming the boot parameters. The parameters may be set by using a Boot EEPROM on the EEPROM_I2C interface or by writing the registers directly over the MDIO interface.

XFP/SFP/SFP+ Module Two-Wire Access

Read and write access to the module is controlled by firmware on the UC_I2C bus. The entire module address space is automatically read upon firmware startup or module hotplug by detection of the MOD_ABS signal. The firmware implements the following features for module I2C access:

- automatic memory read on firmware startup
- automatic memory read on hotplug
- MDIO-triggered I2C read/write (both single-byte and 256-byte transactions)

The QT2025 detects that a module is present by sensing the level on the Mod_ABS pin. On firmware initialization or a hotplug event, the firmware will automatically copy the contents of the module registers into internal MDIO register space. Modules are always addressed using one-byte addressing. When the module is removed, the register contents are erased to 0.

The slave address for an XFP module address is 1010000 (A0), while the SFP+ module uses memory at addresses 1010000 (A0) and 1010001[1] (A2).

SFP+ hardware address A0 is mapped to MDIO registers 3.D000-3.D0FFh.

DOM Memory Access

The SFP+ DOM memory (A2) is mapped to MDIO registers 1.8007-1.8106h (the NVR address space) or alternatively to 1.A000-1.A0FF (this is firmware load dependent; it may be configurable[2]). If mapped to 1.A000-1.A0FF, DOM-related alarms in the SFP+ module will feed into the LASI alarm tree (see “Link Alarm Status Interrupt Pin (LASI)” on page 74 for details).

Later firmware versions implement a DOM periodic polling feature, where the DOM memory is read at every 1s. Optical alarms will then automatically alert the host system through the LASI interrupt pins. Only a subset of registers containing dynamically changing values are polled on each update. Consult AMCC for details on this feature.

1. This memory space contains Diagnostic Optical Monitoring (DOM) information that dynamically reports parametric information about the optics in the module. It is compliant to SFF-8472 (See “Diagnostics Overview”)
2. Available in firmware load 2.0.1.0 and later.

UC_I2C Bus One-Byte Addressing

This section outlines the command structure for two-wire reads and writes in one-byte addressing mode on the UC_I2C. This mode is used automatically when communicating to attached modules.

Read Cycle Timing

The UC_I2C bus always performs single-byte read transactions in 1-byte addressing mode. Multiple single-byte read transactions are used to read multiple bytes. Two types of read transactions are used. The first transaction is used to specify the word address in the peripheral device, as shown in Figure 55. It is used as the first transaction when reading multiple contiguous bytes. The second transaction type, shown in Figure 56, does not specify the word address and is used to read additional bytes when multiple contiguous bytes are read.

Reading Module Memory

The PHY supports single byte and 256-byte reads from the I2C memory stored in XFP and SFP+ modules. The single byte read uses the transaction shown in Figure 55.

When reading the entire 256 bytes of memory, the first read specifies the word address. Subsequent reads exclude the word address (Figure 56). When word address 128 is reached, the word address is again included in the read transaction. This is done in order to satisfy the requirements in the XFP MSA Clause 4.5.2. All subsequent reads exclude the word address.

Figure 55: UC_I2C Read Cycle Timing for 1-Byte Addressing with Address Frame

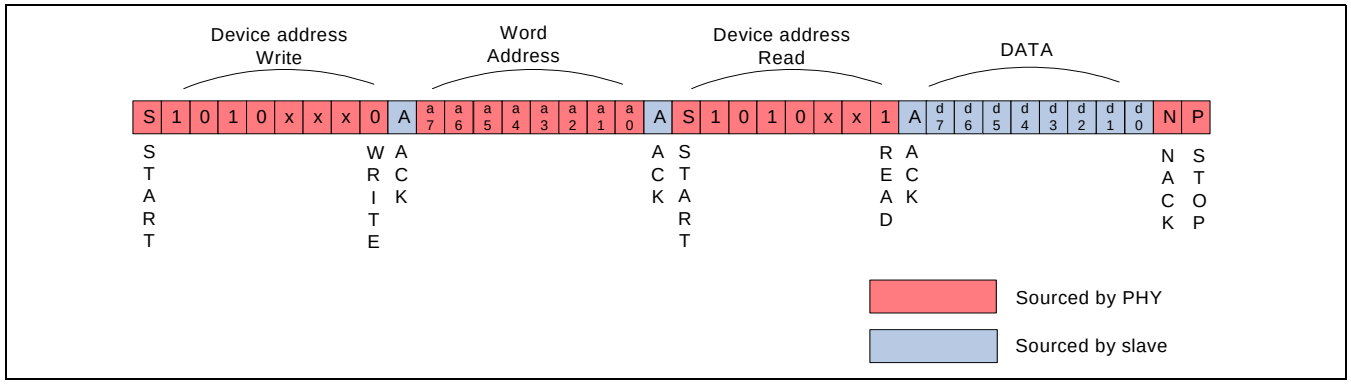
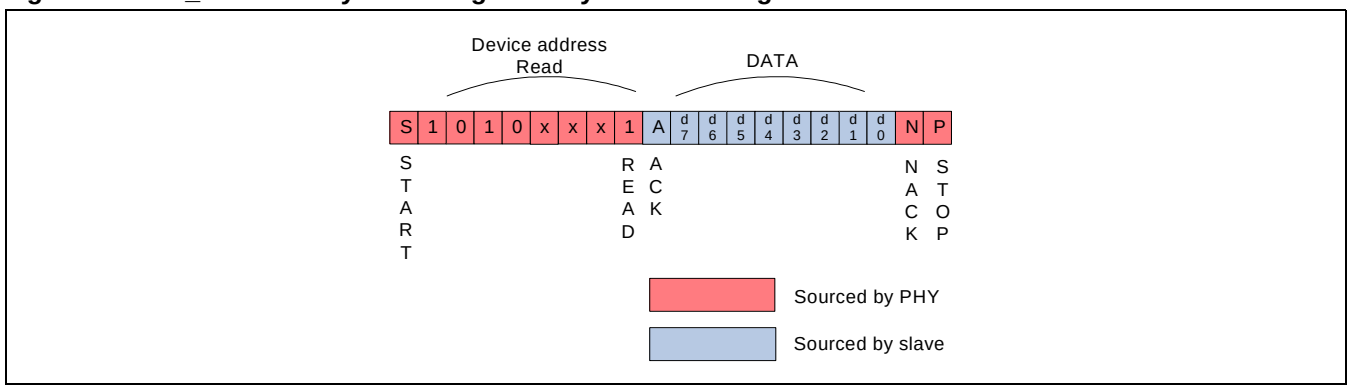


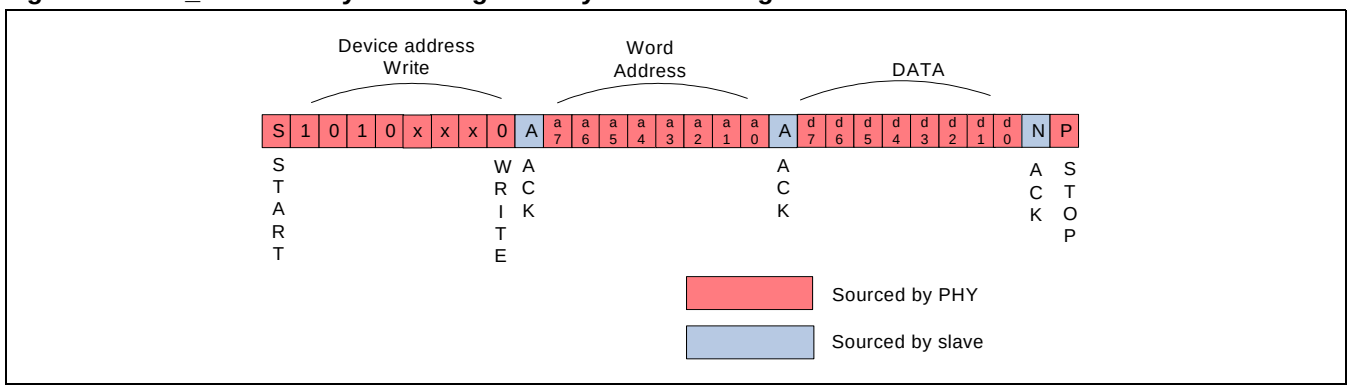
Figure 56: UC_I2C Read Cycle Timing for 1-Byte Addressing without Address Frame



Write Cycle Timing

The write cycle timing in 1-byte address mode is shown in Figure 57. This transaction is used when writing to attached XFP and SFP+ modules. This transaction is called multiple times when performing a multi-byte write.

Figure 57: UC_I2C Write Cycle Timing for 1-Byte Addressing



UC_I2C Bus Two-byte Addressing

To allow a single device on the I2C bus to store the entire firmware image for the internal microprocessor, the QT2025 supports 32kB of memory within a two wire device rather than 256 bytes. This requires 2 byte addressing within the slave peripheral. Two-byte addressing is the default mode.

The read/write cycle contains two 8-bit address bytes. The upper word address is the most significant.

A sample page write transaction to the EEPROM is shown in Figure 63. The PHY uses multiple 64-byte write transactions when writing the firmware to the EEPROM.

A sample page read transaction from the EEPROM is shown in Figure 59. The PHY performs a single 24kB read transaction when reading the firmware from the EEPROM.

Figure 58: UC_I2C Write Cycle Timing for 2-Byte Addressing

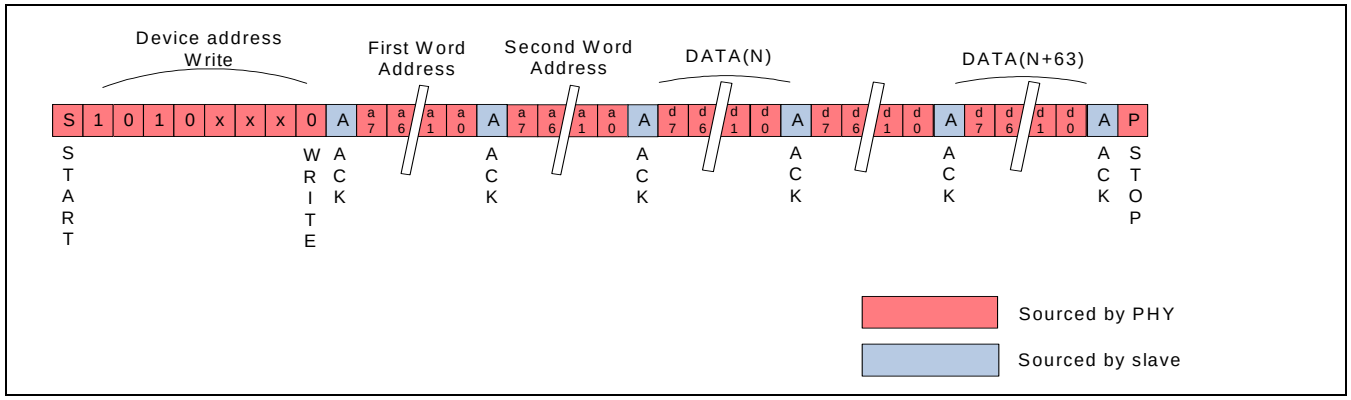
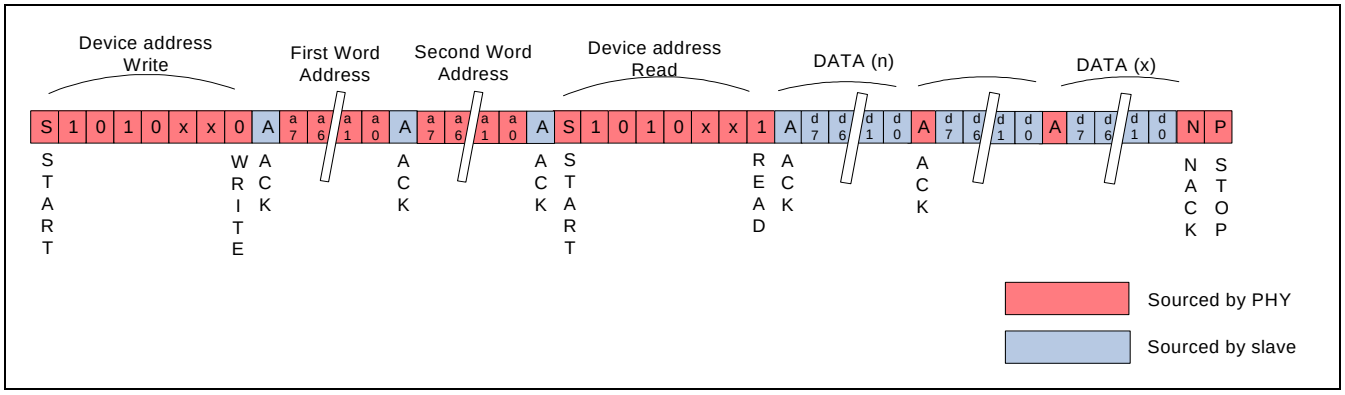


Figure 59: UC_I2C Read Cycle Timing for 2-Byte Addressing



EEPROM_I2C Two Wire Interface

The EEPROM_I2C interface (EEPROM_SCL/SDA) is an industry standard serial two-wire interface that can be used as a master to control peripheral devices or as a slave to allow access to the QT2025 internal registers. The primary applications for this interface are:

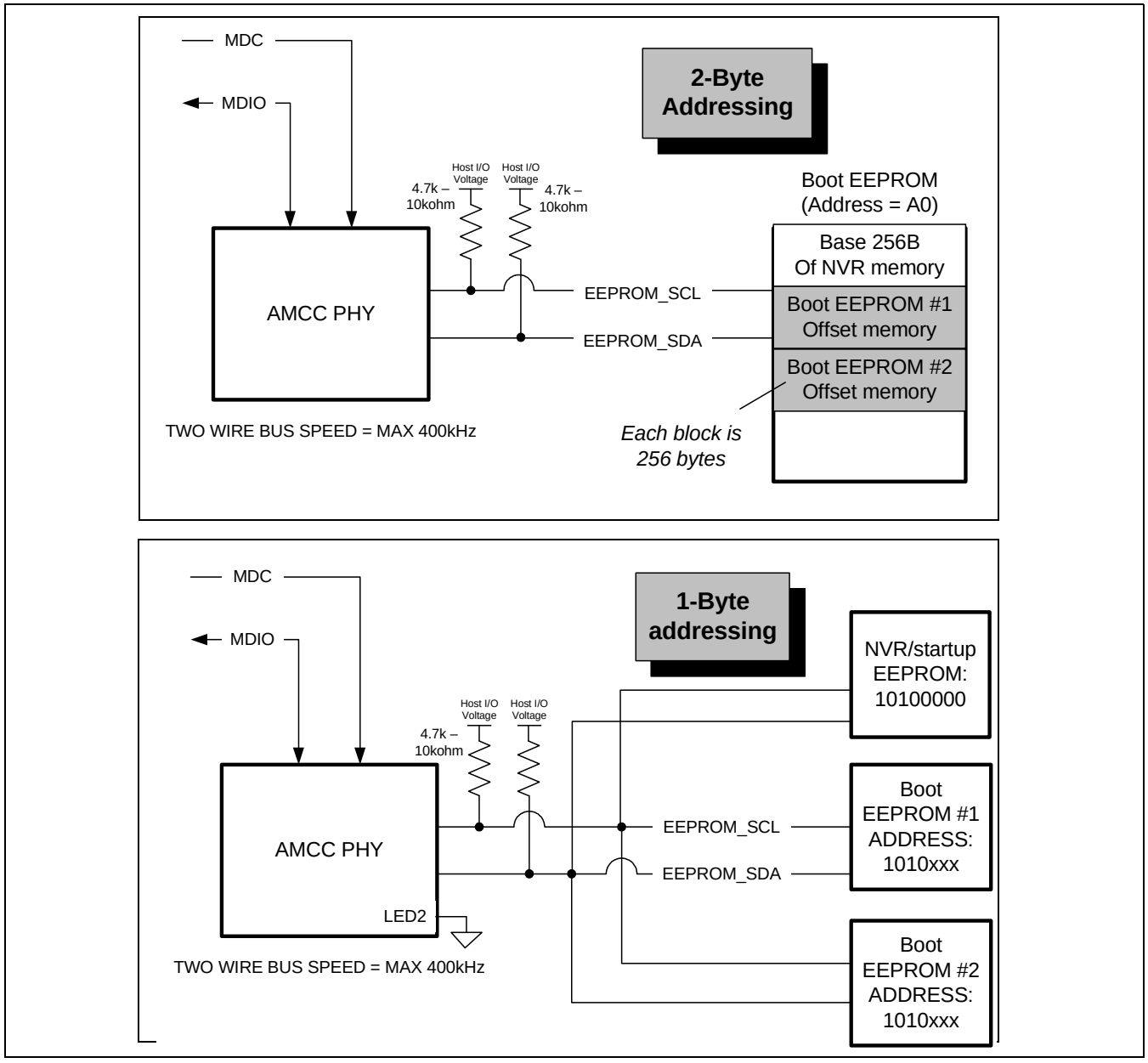
1. Boot EEPROM for MDIO Register Configuration: PHY booting and register configuration on startup
2. XENPAK NVR memory device mirror
3. XENPAK DOM device monitoring[1]

Addressing Modes

The Boot EEPROM interface uses 2-byte addressing by default. The interface will use 1-byte addressing if the LED2 pin is pulled to GND during a hard reset.

1. While the EEPROM_I2C bus is capable of monitoring a DOM device, this feature is implemented in firmware and associated with the UC_I2C bus.

Figure 60: Boot EEPROM Two Wire Interface Configuration Options



The EEPROM serial interface consists of pins EEPROM_SCL and EEPROM_SDA. The logic levels for this interface are 0V and 1.2V however both pins are 3.3V tolerant. The EEPROM_SCL output clock is only active when accessing one of the slave devices on the bus. The default clock rate is 100kHz (derived from the chip reference clock of 156.25MHz). The clock rate can be increased to 400kHz by configuring register bits 1.C003h.15:14. When the chip reference clock is 52.083MHz the EEPROM_SCL frequencies are reduced to 33.33kHz and 133.33kHz depending on the above register setting. Clock stretching is supported on this interface.

Both the EEPROM_SCL and EEPROM_SDA pins are open-drain outputs. Thus, these pins require a pullup resistor to a voltage level that is compatible with both the QT2025 and the slave devices. The value of the pullup resistor should be in the range from 1kΩ to 10kΩ. EEPROM SDA and SCL pins may be wire OR'ed with other open drain two wire devices.

EEPROM_SCL is an output during normal operation. When the EEPROM_SCL clock signal is inactive, it is in a high impedance state. EEPROM_SCL is also bidirectional to allow an external device to control the two-wire bus. Multi-master mode is supported through bus arbitration.

Boot EEPROM: MDIO Register Configuration from External EEPROM

MDIO registers can be configured through an upload from external EEPROM memory at startup. This feature can be used to change the value of any MDIO register from the default without requiring a command on the MDIO interface. The new values are uploaded automatically after chip powerup or reset. This is primarily used to boot the chip.

Bootup Sequence

The bootup sequence followed by the chip is shown in Figure 61. The PHY automatically performs this boot sequence when a hard reset clears (RESETN transitions from '0' to '1') or a soft reset is issued.

The PHY first reads the base NVR memory from the attached EEPROM. The Boot EEPROM memory will then be read, if present. Any MDIO commands contained in the Boot EEPROM space are executed as they are read by the PHY.

The firmware initialization sequence will begin instantly upon the microcontroller reset being cleared. However, the Boot EEPROM read sequence will continue to completion. To prevent a conflict, the last Boot EEPROM command should clear the microcontroller reset.

After the Boot EEPROM instructions are read, the bus will upload memory from an attached DOM device, if present. [1]

Boot EEPROM Format

Up to 512 bytes of Boot EEPROM memory can be used to configure the MDIO registers, divided into two 256 byte blocks. The configuration of each MDIO register requires 5 bytes of EEPROM space. The maximum number of MDIO registers which can be configured is 256/5 = 51 per EEPROM device (maximum of 102 registers with two devices). The data structure in the EEPROM for the MDIO register configuration is shown in Table 28

1. No DOM device is attached to the EEPROM_I2C bus in SFP+ applications, so this step is skipped.

Table 28: MDIO Register Config Data Structure

Locations	Fields
0	Device ID [7:0]
1	Register Address [15:9]
2	Register Address [7:0]
3	Register Data [15:8]
4	Register Data [7:0]

The 5 bytes of contiguous EEPROM memory is used for each MDIO command. The values must be stored in the order shown in Table 28. The EEPROM memory space is logically divided into blocks of 5 bytes each, starting at memory locations 0, 5, 10, 15...250. The 5 bytes of register data must be stored in one of these logical blocks. Any of these 51 logical blocks may be used to store data for any valid register. Unused registers should be set to 00h or FFh. Fields where the Device ID or register address fields do not correspond to a defined register are ignored.

Considerations

Registers associated with the microcontroller cannot be accessed through the Boot EEPROM. This includes registers in the range: 1.Fxxx, 3.Dxxx.

Usage with 2-byte Addressing

In 2-byte addressing mode, a single EEPROM device at address A0 is used for MDIO command storage e.g. AT24C64. Up to two 256 byte blocks of memory are used within the EEPROM to store commands, used to boot and configure the PHY. I2C address 0xC8 stores information about where the data is stored within the EEPROM. The base 256 bytes of memory is read on startup (0x0 - 0x99) and then the boot EEPROM memory is read based on the contents of register 0xC8. Figure 29 on page 101 describes the format of this register.

Three bits are used to specify each memory offset location. The 256 bytes beginning at address n*0x100 are used, where n is the specified offset. Values of n = 0 and n = 7 are ignored. e.g. if n = ‘101’ the chip reads memory addresses 0x500 - 0x599.

Usage with 1-byte Addressing

Up to three logical EEPROMs are required to support this feature with 1-byte addressing. On startup, the chip automatically reads the EEPROM at address A0. Within this EEPROM, address 0xC8 stores the locations of the two additional boot EEPROMs. Figure 29 on page 101 describes the format of this register.

Three bits are used to specify each memory address. The upper 4 device address bits are hardwired to 1010. Addresses A0 and A7 are ignored.

If valid EEPROM addresses are specified, the chip will attempt to read the EEPROM memory and execute the commands stored in them.

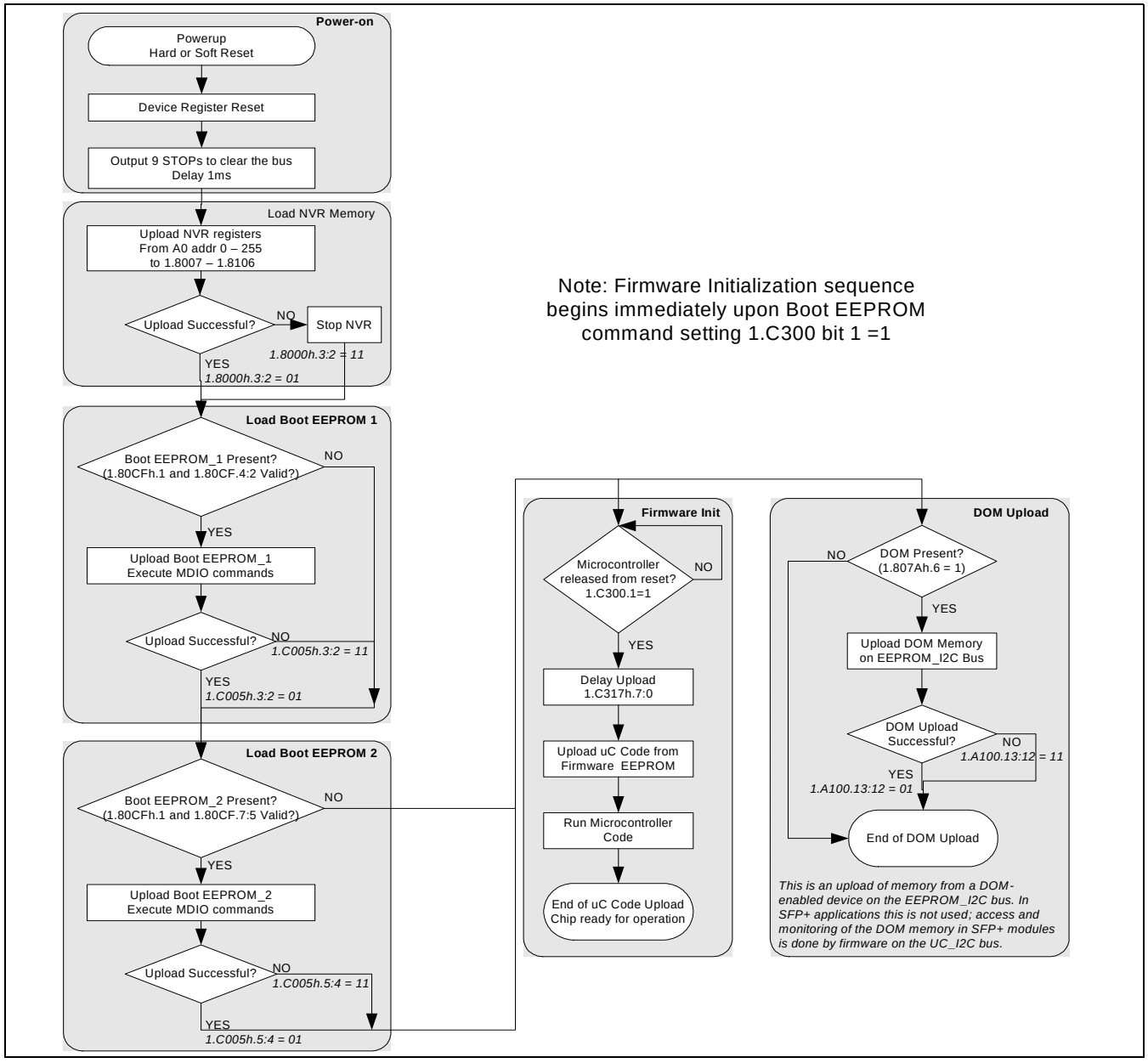
A single physical EEPROM that uses paged memory can be used in 1-byte addressing mode e.g. AT24C08.

Table 29: Boot EEPROM Config Register 0xC8 Definition[1]

Bit	Name	Description
1	Enable	Enable control for reading boot EEPROM instructions 0 = do not read EEPROM memory 1 = read EEPROM memory and execute MDIO cmds
4:2	I2C Memory Address #1	2-byte addressing: EEPROM Memory Address Offset #1 1-byte addressing: EEPROM Memory Address #1 If the value is ‘000’ or ‘111’ then skip read.
7:5	I2C Memory Address #2	2-byte addressing: EEPROM Memory Address Offset #2 1-byte addressing: EEPROM Memory Address #2 If the value is ‘000’ or ‘111’ then skip read.

1. Default uses 2-byte addressing on EEPROM_SDA bus and I2C address is A0. If 1-byte addressing is used, then bits 4:2 and 7:5 store the lower 3 address bits (A2, A1, A0).

Figure 61: Boot EEPROM Startup Flow



EEPROM_I2C One-Byte Addressing

This section outlines the command structure for two-wire reads and writes in one-byte addressing mode on the EEPROM_I2C bus.

1-Byte Read Cycle Timing

The timing for the read cycle is shown in Figure 62. The two-wire internal address counter is first set by a dummy write cycle. This is followed by a read from the first word address from the slave device. The reception of the 8 data bits is followed by an acknowledgement (ACK) from the QT2025. The ACK indicates to the slave that data from the next word address will be read. An ACK is supplied after the reception of each data byte until all bytes have been read. A NACK is given after data byte 255 followed by a STOP (P) to terminate the read cycle.

The slave must provide an acknowledgement (ACK) when presented with its slave address before any reads or writes can occur. Upon reception of the ACK, the sequential read can commence. The slave must also provide an ACK after the address byte field and slave address field are sent. If any of the three expected ACKs is not provided by the slave, the QT2025 will restart the read cycle. If proper ACKs are not received after 16 polling sequences and the read sequence is aborted. This error flag can be accessed at MDIO register address 1.C003h.

The EEPROM_I2C bus can read 256 bytes at a time or a single byte. The 256 byte read transaction occurs in bursts of 1, 8, 16 or 256 (default) bytes. The burst size is controlled by the NVR_READ_BURST_SIZE register field.

Figure 62: EEPROM_I2C Read Cycle Timing (1-byte addressing)

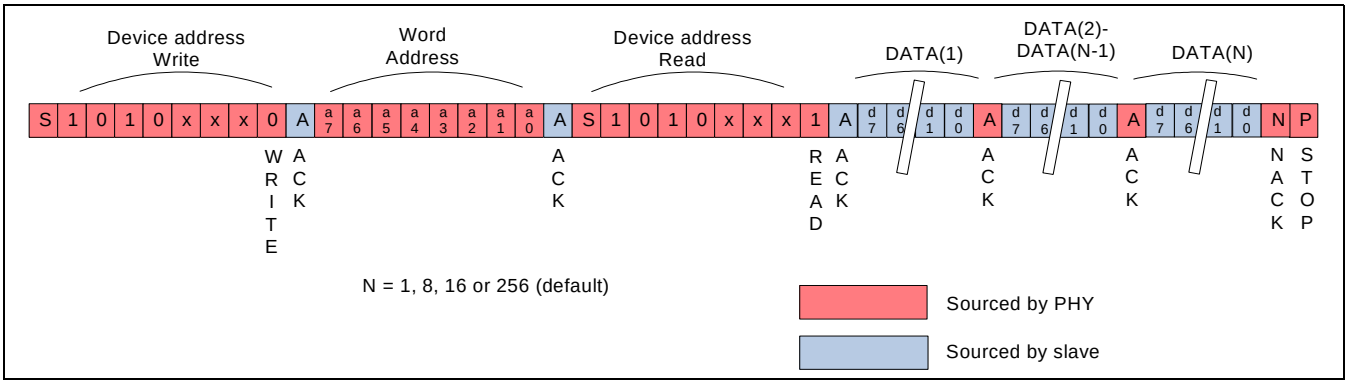


Table 30: Checksum Calculations for EEPROM_I2C Reads

Two-Wire Interface	Checksum Register in Slave	Mirrored Checksum from Slave	Calculated Checksum Register	Checksum Calculation	Checksum Flag Bit
EEPROM	118	1.807Dh	1.C004h[15:8]	8 LSBs of sum of uploaded bytes 0 to 117	1.C003h[7]

EEPROM_I2C Checksum Calculation

The PHY performs a checksum calculation after every successful 256 byte read from address A0 on the EEPROM interface. Table 30 details the checksum registers and the checksum calculation and status flag. The calculated checksum is reported in the NVR_CHECKSUM field. The checksum status is reported in the NVR_CHECKSUM_OK field.

The checksum feature is compliant to the XENPAK MSA Clause 10.10. If the checksum fails it is reported

in the NVR_CHECKSUM_OK field. It is not important for the checksum to pass in non-XENPAK applications.

1-byte Write Cycle Timing

Page write mode is used to transfer 256 bytes of data to the slave. The burst size can be set to 1, 8 (default) or 16 (set by MDIO register field NVR_WRITE_BURST_SIZE). It is done sequentially 256, 32 or 16 times in order to transfer all 256 bytes. In between page writes, the QT2025 polls the NVR for an ACK, which indicates that the NVR internal write cycle is completed. If no ACK is received, the QT2025 waits for 1.7ms and then repeats the poll for an ACK. After 16 tries without an ACK, the write cycle is aborted and the EEPROM_ACK_error flag is set. An ACK must be received after each data word is written or the write cycle is aborted and the EEPROM_ACK_error flag is set. MDIO register 1.8000h[3:2] indicates when the write has been completed.

Single Byte Read or Write Cycle (EEPROM_I2C Interface Only)

An EEPROM Single Byte Read/Write Cycle is initiated by setting MDIO EEPROM control register bits 1.8000h[1:0] to 10b. As with the 256 byte read/write commands, MDIO register 1.8000h[5] determines if a read or a write cycle will be performed. The single byte EEPROM address is read from EEPROM control register bits 1.8000h[15:8]. The data is read to or from the associated MDIO register.

If an NVR command is in progress, then no new NVR command will be accepted. The NVR command register must be in the idle state for any new NVR commands to be accepted.

EEPROM_I2C Two-byte Addressing

The EEPROM_I2C bus defaults to two-byte addressing mode. To enable 1-byte addressing, the LED2 pin must be held low during a hard reset.

The read/write cycle contains two 8-bit address bytes. The upper word address is the most significant. A sample 8 byte page write transaction to the EEPROM space is shown in Figure 60.

In this mode, the QT2025 supports the same read and write commands as with standard 1-byte addressing.

Figure 63: EEPROM_I2C 2-Byte Write Cycle Timing

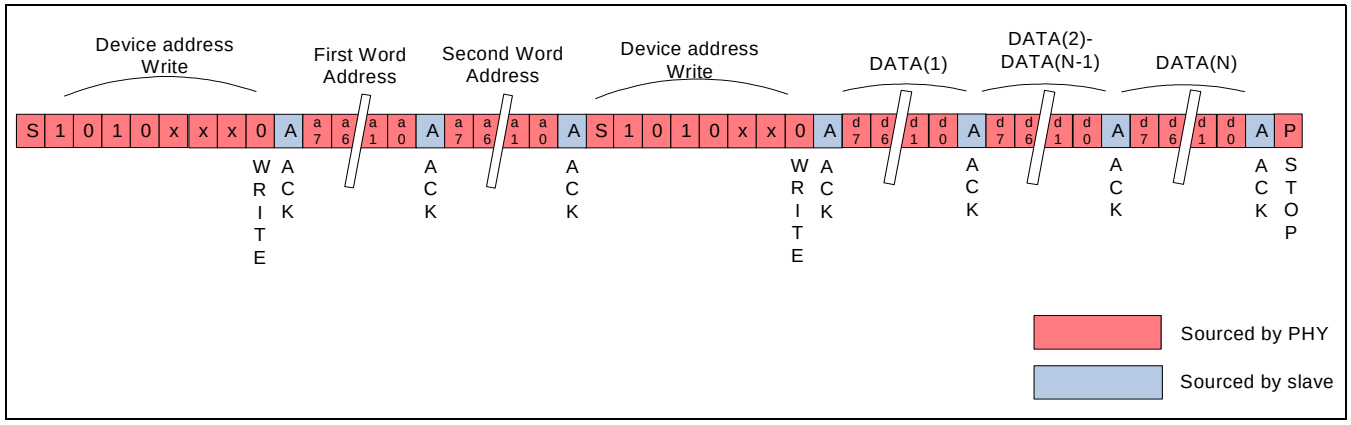
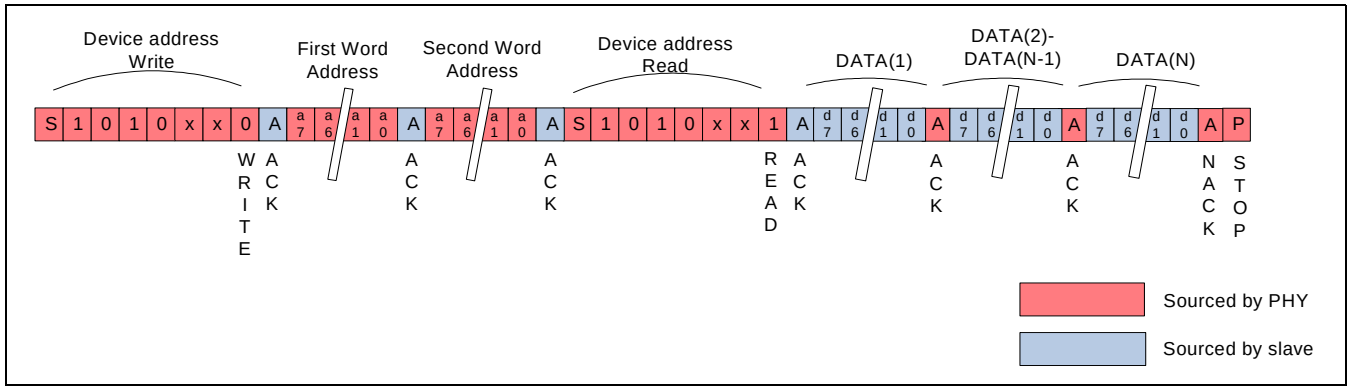


Figure 64: EEPROM_I2C 2-Byte Read Cycle Timing



EEPROM_I2C Slave Mode for Register Configuration

The MDIO register space can be accessed through the EEPROM_SCL/EEPROM_SDA two-wire serial interface bus. This allows the QT2025 to be controlled by an external microprocessor via two-wire as opposed to the MDIO interface. All register reads and writes to the MDIO register space via the two-wire interface are indirect.

(Note: the UC_I2C bus does not support a slave mode.)

Considerations

Registers associated with the microcontroller cannot be accessed through the I2C bus. This includes registers in the range: 1.Fxxx, 3.Dxxx.

Addressing Mode

The I2C Slave mode uses 1-byte addressing only. It does not change with addressing mode when the bus is acting as a master.

Register Address Mapping

The normal 256 byte two-wire address space is divided into lower and upper blocks of 128. The lower block of 128 bytes is directly available and is used for defining the MDIO device ID and MDIO register starting address. Address location 125 (7Dh) stores the MDIO device ID. Address 126 (7Eh) stores the upper byte of the register address to be accessed, while address 127 (7Fh) stores the lower byte. Address locations 0 - 124 are not used (Reserved - RO).

The upper 128 bytes of the two-wire address space are mapped directly to the MDIO registers. The first two bytes in this range are mapped to the QT2025 memory register address defined by the values in two-wire address locations 125 - 127 (above); address 128 is mapped to the upper byte of the register and address 129 is mapped to the lower byte. The following two bytes are mapped directly to the next register in the QT2025 register space. Similarly, each subsequent pair of bytes is mapped to the following QT2025 register. In this way, the two-wire upper 128 bytes are mapped to 64 contiguous QT2025 memory registers. The memory mapping between the I2C address space and the MDIO registers is shown in Figure 65.

For example, if the MDIO address is set to Register 1.C000h (i.e. Device 1, Address C000h), then the two-wire address space 128 - 255 will be mapped to the QT2025 register addresses in the range 1.C000h - 1.C063h.

Many of these memory address locations are not defined in the QT2025. Reads from these address locations will return 0; writes to these address locations will be ignored.

Reading and Writing using the I2C Interface

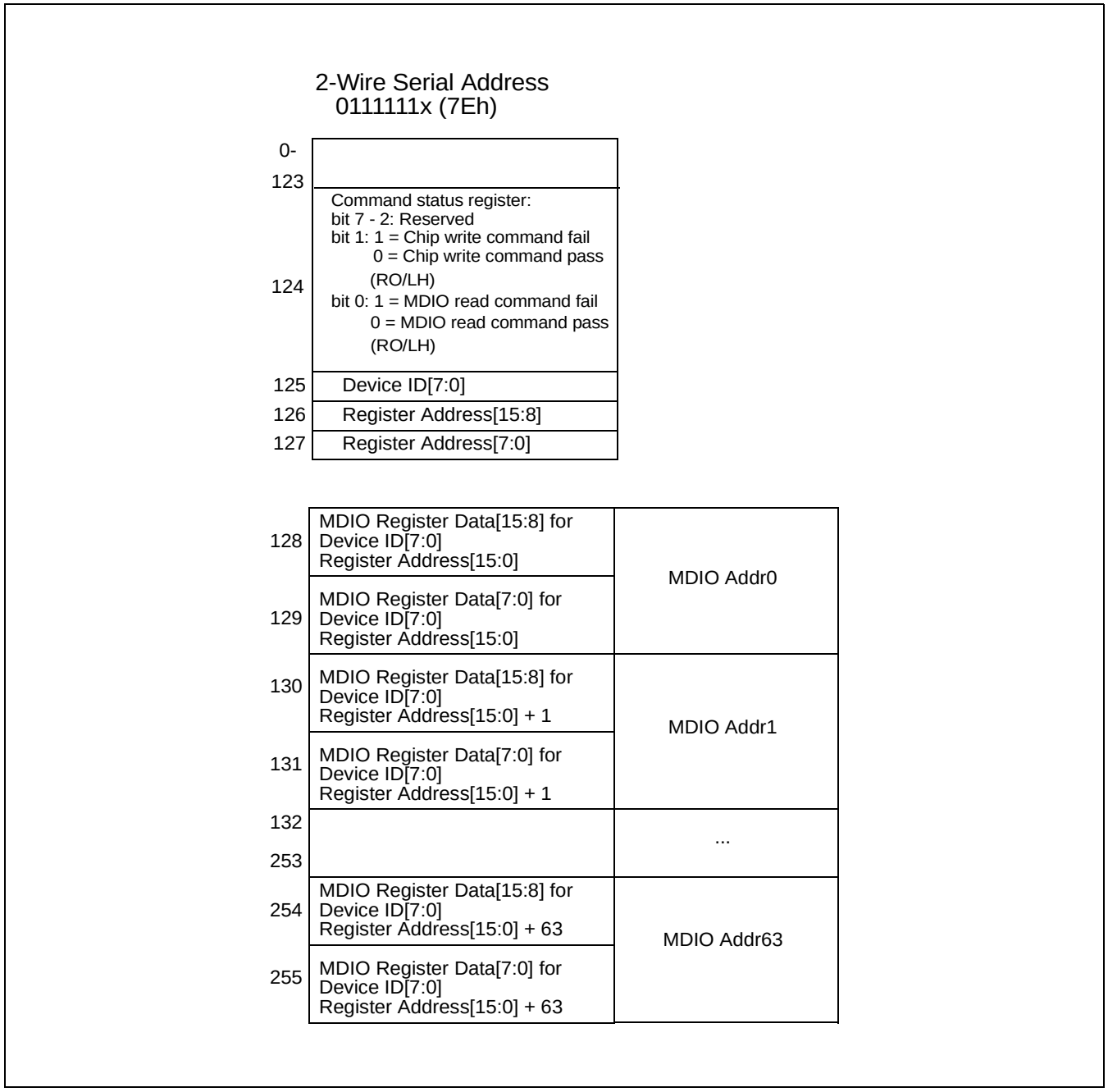
The slave address for two-wire access is hard-wired to 0x7Eh. To initiate read or write transactions to an MDIO register, the Device ID and register address must be set. Three two-wire write commands must be performed to set these values in the correct memory locations 125-127. Burst writing is supported. Memory location 124 is the command status register. When there are simultaneous access requests to the MDIO registers from both the MDIO bus and the two-wire interface (slave mode), the MDIO register access through the two-wire interface may fail since the MDIO bus access always has the highest priority. This failure will cause the command status bit 0 to be set to high. A similar case is when there are simultaneous access requests to the MDIO registers from the MDIO bus and chip configuration. This may cause the chip configuration to fail and the command status register bit 1 to be set. Both register bits are read only and latched high.

Once the register address is fully defined, a two-wire read command to any address in the range 128 - 255 will return the QT2025 register contents, according to the mapping in Figure 65.

For MDIO register read access, the lower byte of the MDIO register data is latched when the upper MDIO register data byte is read i.e. the contents of lower byte are stored until it is read. It is recommended that the upper byte be read first.

For MDIO write access, the MDIO register in the QT2025 will be updated after the lower byte of register data has been written to the I2C register space. This ensures that complete words which represent a single 16 bit MDIO register data value are kept intact. Write to the upper byte memory space first to a guarantee the proper value is set.

Figure 65: MDIO Register Indirect Access Memory Mapping for Two-Wire Access



10Gbps Diagnostic and Test Features

This chapter describes the test features available when using the 10Gbps signal path. None of these features are available on the 1Gbps signal path. 1Gbps test features are listed separately in the 1GbE Mode section.

Loopback Modes

Loopbacks allow the data signal to be internally routed between the transmit and receive data paths. Several loopbacks are available within the chip at various points along the signal path. The loopbacks are categorized into two types. A “System” loopback routes the signal from the transmit path to the receive path. A “Network” loopback routes the signal from the receive path to the network path. The available loopbacks are documented in Table 31 and Table 32 and their locations depicted in Figure 66.

For details on loopbacks in 1GE mode, see “1GE Test Patterns and Loopbacks” on page 51.

System Loopbacks

When in any system loopback mode (PMA, WIS, PCS or XGXS system) the QT2025 accepts data from the transmit path (XAUI input) and returns it on the receive path (XAUI output).

The default signal transmitted on the FTXOUT interface is loopback-dependent and is listed in Table 31.

The FTXOUT data signal can be changed when the associated ‘Loopback Data Override’ is set for the given loopback mode. The override pattern is also listed in Table 31.

XGXS Analog System Loopback

With the XGXS Analog Loopback feature, the clock or data signal from any of the four XAUI CDRs is looped back to the XDRV2 output. There are three enable bits required to turn on this feature (listed in Table 31). There are 8 individual control bits to select the desired lane clock or lane data signal. Select only one signal at a time.

Table 31: 10GE System Loopback Modes and MDIO Control Registers

Loopback name	Loopback Enable	Loopback Data Override	FTXOUT output when Loopback Data Override=0 (default)[1]	FTXOUT output when Loopback Data Override=1
PMA System Loopback[2]	1.0000h[0]	1.C001h[15] [3]	transmit data	all 0’s (0x0000h)
WIS System Loopback	2.0000h[14]	2.C001h[4]	0x00FFh	transmit data
PCS System Loopback	3.0000h[14]	3.C000h[5]	0x00FFh	transmit data
XGXS System Loopback	4.C000h[14]	4.C000h[15]	all 1’s (0xFFFFh)	transmit data
XGXS Analog System Loopback	**Enable Fields** 4.C05Bh[15] 4.C05Fh[9] 4.C05C[10] **Select Fields** *Clock Lane Select* Lane3-Lane 0 = 4.C05Fh[3:0] *Data Lane Select* Lane3-Lane 0 = 4.C05Fh[7:4]	n/a	n/a	transmit data/clk

1. The Loopback Data Override bits are set to 0 by default for all system loopbacks
2. PMA System Loopback is not guaranteed to work when firmware is running in 10GBASE-KR mode.
3. For PMA System Loopback, the Loopback Data Override must be set *before* enabling the loopback. The Override setting is ignored after the loopback is enabled. This loopback is controlled by firmware.

Network Loopbacks

When in any network (PMA or XGXS) loopback mode the QT2025 accepts data from the receive path and returns it on the transmit path.

The chip will not prevent multiple loopbacks from being enabled but the result is undefined and these modes are not supported.

Table 32: 10GE Network Loopback Modes and MDIO Control Registers

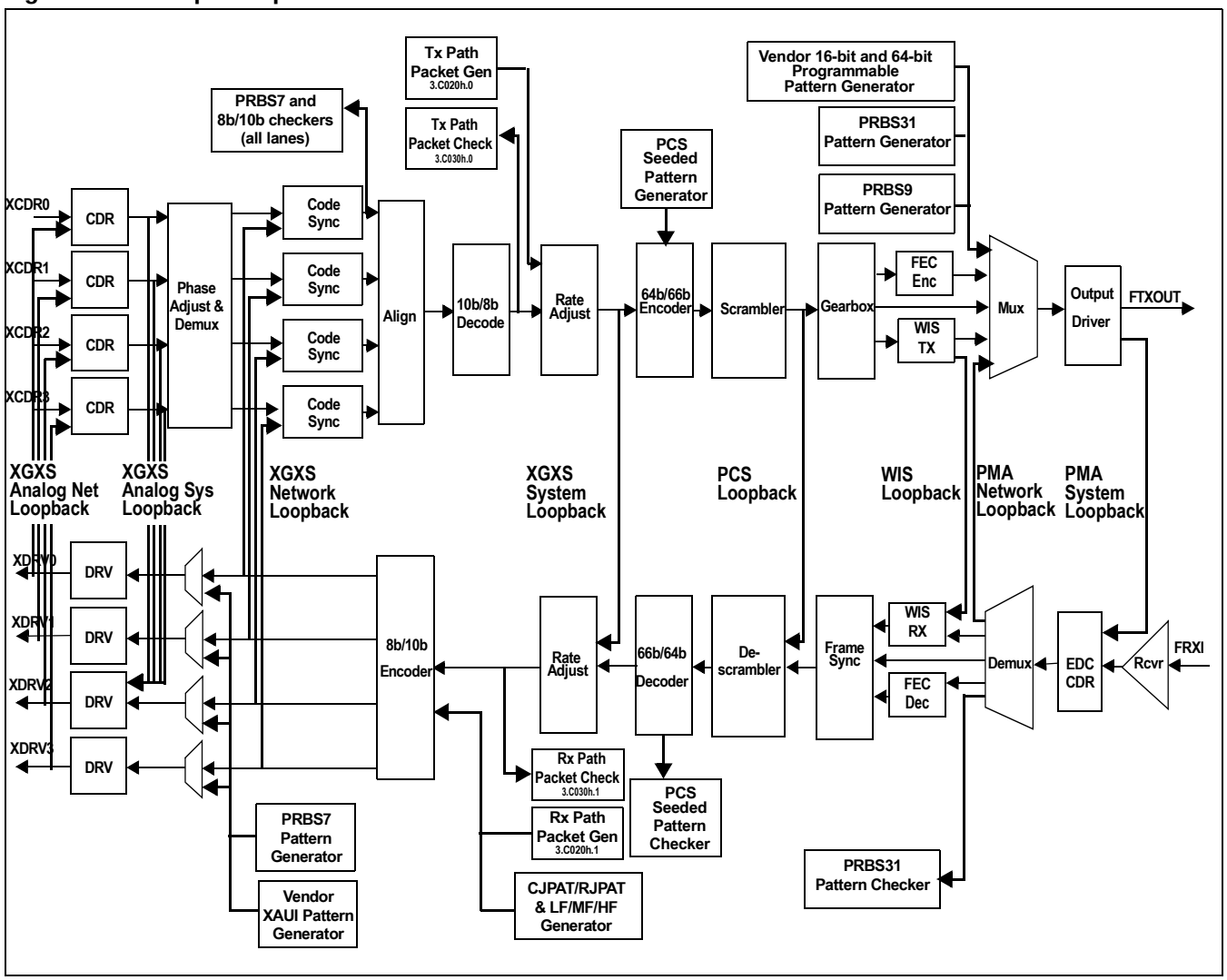
Loopback name	Loopback Enable	Loopback Data Override	XDRV output when data override=0	XDRV output when data override=1 (default)[1]
XGXS Network Loopback	4.0000h[14]	4.C000h[13]	all 0's (0x0000h)	received data
PMA Network Loopback	1.C001h[4] AND 1.C001h[9] [2]	1.C001h[5]	Idle Codes at XDRV	received data
XGXS Analog Network Loopback	4.C05Bh[13] AND 4.C05F[8] [3]	n/a	received data	received data

1. The Loopback Data Override bits are set to 1 by default for all network loopbacks
2. Linetiming must be enabled in order for PMA Network Loopback to function properly. Cannot be used simultaneously when enabling the synchronous ethernet recovered clock (125MHz clock) on any output.
3. The registers must be configured in the order listed for the loopback to function properly. This loopback is also available in 1GE mode.

PMA Network Loopback

When in PMA network loopback mode, the recovered and retimed 10Gbps received data is looped to the transmit driver and output at FTXOUTP/N. In order to ensure proper operation in this mode, the **line timing mode must be enabled**. If not already configured, line timing can be forced on by setting FTX_LTIME_EN to '1' (1.C001h[9]).

Figure 66: 10Gbps Loopback and Test Pattern Generator/Checker Locations



XAUI Interface Test Features

PRBS7 Pattern Generator

XAUI PRBS, or XAUI BIST, test mode enables the 2^7-1 PRBS generator on each XAUI lane output. The PRBS pattern is generated using the polynomial $1+x^6+x^7$. The generator is controlled by MDIO register by 4.C000h[10]. This will cause a PRBS7 pattern to be output on all 4 XAUI output lanes simultaneously.

PRBS7 Pattern Checker

For test purposes, there is a PRBS7 pattern checker for each XAUI input lane. The PRBS7 pattern checker expects data generated using the polynomial $1+x^6+x^7$. The checker is enabled through an MDIO register bit. If a pattern error is detected the error flag is set for that lane (4.C001h[3:0]). The error flag will remain set until cleared by an MDIO read. For each lane, there is a dedicated 8 bit error counter for checking PRBS7 errors on the XAUI input in MDIO registers 4.C030-4.C033h. Each counter works independently. Each register is a read-only, non-rollover counter that is cleared upon read.

If any of the XAUI input CDRs are not in lock, the PRBS7 pattern checkers will not operate properly for all 4 lanes - errors will be reported on all lanes. Check the lock condition for each lane before using this feature.

Jitter Test Pattern Generator

There are 3 patterns defined for XAUI interface jitter testing: low frequency (LF), high frequency (HF) and mixed frequency (MF) test patterns. See Table 33 for details.

CRPAT Test Pattern Generator

The continuous random test pattern (CRPAT) consists of a continuous stream of identical packets separated by minimum IFG. The contents of the packets are as specified in IEEE 802.3 Section 48A.4. The test pattern provides a broad spectral content and minimal peaking. The CRPAT generator is enabled by writing a 1 to MDIO register 4.C000h[9].

CJPAT Test Pattern Generator

The continuous jitter test pattern (CJPAT) alternates repeating low transition density patterns with repeating high transition density patterns. This will expose the receiver's CDR to large instantaneous phase jumps. The detailed description of CJPAT is found in IEEE 802.3 Clause 48A.5. The CJPAT generator is enabled by writing a 1 to MDIO register 4.C000h[8].

8b/10b Error Checkers

For each lane, there is a dedicated 8 bit error counter for checking 8b/10b coding errors on the XAUI input in MDIO registers 4.C030-4.C033h. Each counter works independently. Each register is a read-only, non-rollover counter that is cleared upon read. This counter can be used when testing with CRPAT and CJPAT.

10-bit XAUI Test Pattern Generator

The XAUI output can be configured to transmit a user-defined 10 bit code word or, alternatively, a static output (no transitions). The desired pattern is selected on a per-lane basis in MDIO register 4.C010h, where a 1 selects a user-defined pattern and a 0 selects the static output.

The 10-bit user defined test pattern is set in the MDIO register bit 4.C011h[9:0]. When enabled for a given lane, the programmed pattern will be continuously transmitted on the XDRV output.

Table 33: XAUI Jitter Test Pattern Generator Enable

Pattern Name	Repeated Bit Pattern - each lane	MDIO register	
		Test Pattern Select 4.0019h[1:0]	Test pattern enable 4.0019h[2]
high frequency	10	00	1
low frequency	1111100000	01	1
mixed frequency	11111010110000010100	10	1

PCS/PMA Data Path Test Features

Scrambler/Descrambler Bypass Modes

The PCS scrambler and descrambler can be bypassed by setting the PCS_DESCRAM_BYP and PCS_SCRAM_BYP fields to 1.

Jitter Test Pattern Generator

Specific IEEE-Standard test patterns are enabled through the MDIO interface by setting as described in IEEE 802.3 Clause 49.2.8.

By setting MDIO register 3.002Ah[2] to 1, the output pattern will be a square wave of 8 high cycles followed by 8 low cycles.

If MDIO register 3.002Ah[1] is set to 0, a programmable pseudo-random pattern is generated at the serial output. This pattern is generated by the PRBS58 scrambler using seeds stored in MDIO registers 3.34 to 3.41. The scrambler is loaded with the 58-bit seeds at the start of every 128 blocks in the following order: seed A, seed A Invert, seed B, seed B Invert. The data input to the scrambler is set to either all zeros or local fault (LF) via MDIO register 3.002Ah[0]. A control sync header of 01 is used and the payload is the pseudo random data output from the scrambler.

Jitter Test Pattern Checker

The PCS test pattern checker in the descrambler is enabled via an MDIO register 3.002Ah. When the descrambler output matches the data pattern, or its inverse, a match is declared. Since the descrambler is free running and the scrambler is being loaded with a new seed every 128 blocks, a mismatch will be detected once every 128 blocks. This first mismatch does not increment the counter.

A 16-bit, non-rollover counter, PCS_TSTPAT_ERRCNT, counts the errors and is reflected in MDIO register 3.002Bh. This is a non-rollover counter that is reset when read.

64-Bit Fiber Test Pattern Generator

The fiber output can generate a user-defined 64 bit code word or, alternatively, a static output (no transitions). The user defined test pattern can be programmed across four 16-bit MDIO register fields FTX_TSTPAT0 through FTX_TSTPAT3 (located at addresses 1.C031h - 1.C034h). When enabled, the programmed pattern will be continuously transmitted on the FTXOUT output.

Transmission of the test pattern is enabled by setting MDIO register field FTX_TSTPATGEN_EN to ‘1’. The desired pattern is selected by setting MDIO register field FTX_TSTPATGEN_SEL, where a ‘1’ selects the programmed 64-bit pattern and a ‘0’ selects the static output.

When more than one data pattern is enabled at the same time, only one of the patterns will be output. The truth table listed in Table 34 determines which pattern will be output.

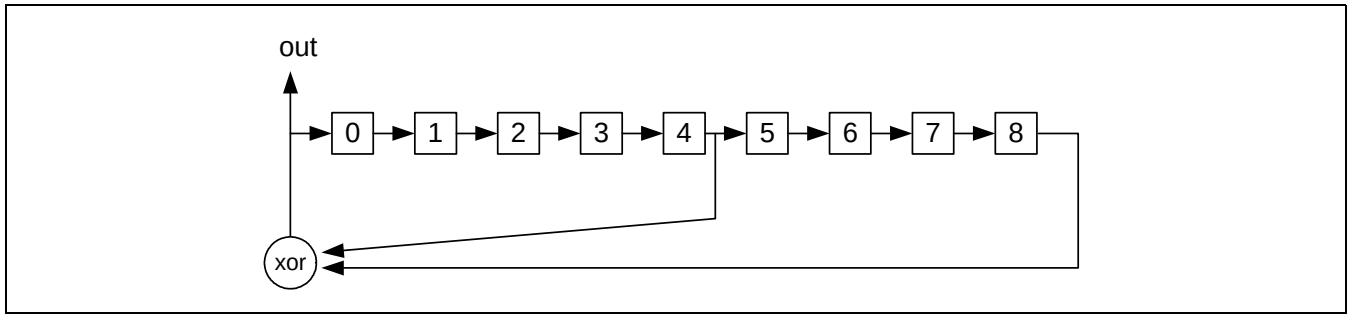
Table 34: Test Pattern Priority

Pattern Name	PCS_JPATGEN_EN 3.2Ah[3]	PCS_JPAT_DATA_SEL 3.2Ah[0]	FTX_TSTPATGEN_SEL 1.C030h[1]
normal chip traffic	0	x	0
64-bit test pattern	1	0	1
	0	x	1
jitter test pattern	1	0	0
square wave pattern	1	1	x

PRBS9 Test Pattern Generator

A PRBS9 pseudo-random pattern generator is available to test the 10Gbps serial transmitter. When enabled, a PRBS9 pseudorandom pattern is output at FTXOUT. The polynomial $1+x^5+x^9$ is used to generate the pattern, as shown in Fig. 67.

Figure 67: PRBS9 Pattern Generator



PRBS31 Test Pattern Generator

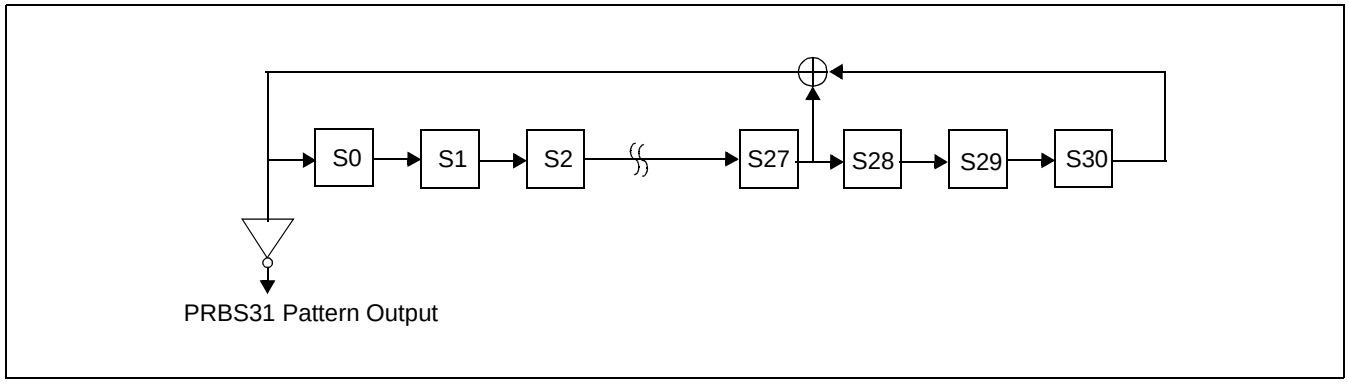
A pseudo-random pattern generator feature is available to test the 10Gbps serial transmitter. When the PRBS31 pattern generator is enabled by setting an MDIO bit register, a 2^{31}-1 pseudorandom pattern is output at FTXOUT. The polynomial $-(1+x^{28}+x^{31})$ is used to generate the pattern. This polynomial produces the same output as the IEEE standard algorithm shown in Fig. 68 (see IEEE 802.3 Clause 49.2.8). The initial seed of this algorithm will not be all zeros.

Note that the PRBS31 output pattern is inverted from the standard pattern generated by most test equipment. To invert the pattern set the register high. Alternatively, configure the test equipment to accept the inverted pattern.

This generator is available in both LAN and WAN operation. It is controlled by a different bit depending on the mode. The control and counter registers are listed in Table 35.

If both the jitter test pattern and the PRBS31 test pattern are enabled, the PRBS31 mode will be chosen (LAN mode).

Figure 68: PRBS31 Pattern Generator



PRBS31 Test Pattern Checker

A pseudo-random pattern error counter feature is available to test the 10Gbps serial receiver. When the PRBS31 error detector is enabled a 2^{31}-1 PRBS pattern is expected on the receive path input. The PRBS31 pattern checker is self-synchronizing and produces the same result as the IEEE standard algorithm shown in Figure 69 (see IEEE 802.3-2005 Clause 49.2.12). Pattern errors are counted by an 16-bit counter and can be observed at MDIO register 3.43 (3.2Bh), which is a non-rollover counter that is cleared on read. When an isolated bit error occurs, it will cause the PRBS31 pattern error output to go high 3 times, once when it is received and once when it is at each tap. Thus, each isolated error will be counted 3 times in the counter.

Note that the expected PRBS31 pattern is inverted from the standard pattern generated by most test equipment. To invert the input to the QT2025, set MDIO register field RXIN_SEL. Alternatively, configure the test equipment to transmit the inverted pattern. The built-in pattern checker is compatible with the built-in generator with no inversion applied to either pattern.

This counter is available in both LAN and WAN operation. It is controlled by a different bit depending on the mode. The same 16-bit counter register is used in both modes. The control and counter registers are listed in Table 35.

If the CDR is not in lock the PRBS31 error counter will read AAAAh. The PRBS31 pattern generator and checker can be used in conjunction with the PMA system loopback.

Figure 69: PRBS31 Pattern Checker

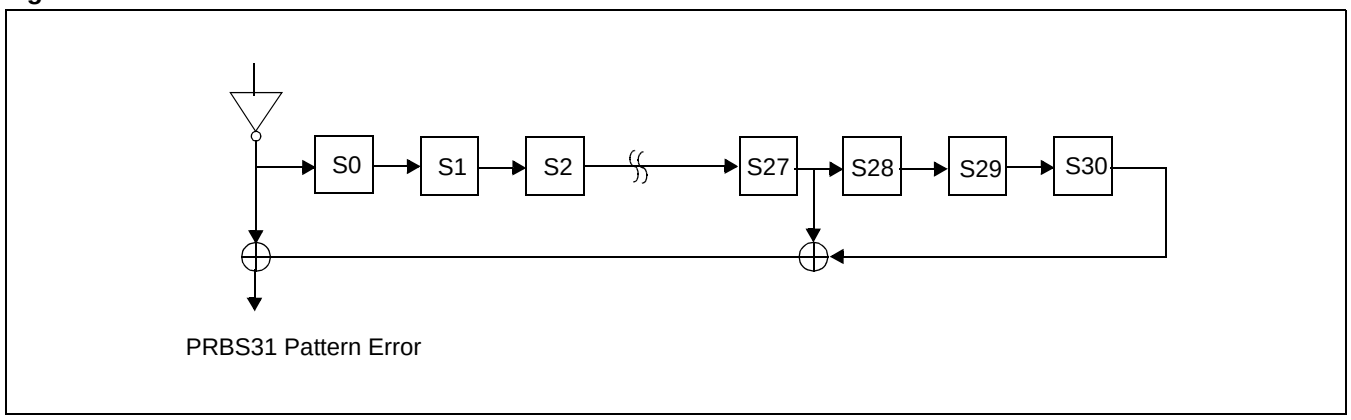


Table 35: 10Gbps PRBS Generator and Checker Control

Item	LAN mode	WAN Mode	Note
PRBS31 Generator Control	PCS_PRBS31GEN_EN 3.002Ah[4]	WIS_PRBSGEN_EN 2.0007h[4]	0 = disabled (default) 1 = enabled
PRBS9 Generator Control [1]	PCS_PRBS9GEN_EN 3.002Ah[6]	WIS_PRBS_9_EN 2.C001h[9]	0 = disabled (default) 1 = enabled
PRBS31 Checker Control	PCS_PRBS31MON_EN 3.002Ah[5]	WIS_PRBSMON_EN 2.0007h[5]	0 = disabled (default) 1 = enabled
Error Counter Select	PCS_FPRBS_VEN_CNT_MODE 3.C000h[13]	WIS_FPRBS_VEN_CNT_MODE 2.C001h[13]	0 = use 16-bit Error Counter 1 = use 32-bit Error Counter
16-bit Error Counter	PCS_TSTPAT_ERRCNT 3.002Bh	WIS_TSTPAT_CNT 2.0009h	16-bit, non-rollover (RO) cleared on read
32-bit Error Counter [2]	PCS_VEN_PRBS_ERR_CNT_LSB 3.C700 (LSB) PCS_VEN_PRBS_ERR_CNT_MSB 3.C701 (MSB)	WIS_VEN_PRBS_ERR_CNT_LSB 2.C700 (LSB) WIS_VEN_PRBS_ERR_CNT_MSB 2.C701 (MSB)	32-bit, non-rollover. Read of LSB latches MSB data. Read of MSB clears counter.

1. There is no PRBS9 checker available for 10Gbps operation.
2. Usable in Timed BER Test only. This applies to both LAN and WAN modes.

Timed BER Test

A timed BER test can be performed on the FRXI receive signal. The 2^{31}-1 PRBS test pattern checker is used to count detected errors within a specified time period. The time period, in seconds, is programmed in the PCS_BERTIMER_START register field. The errors are reported in the selected MDIO test pattern error counter register. Once the PRBS test pattern checker has been enabled, the BER test is enabled by writing a 1 to MDIO register field PCS_BERTST_EN. The PCS_BERTST_BUSY field will be 1 while the BER test is in progress. The completion of the BER test is indicated by the PCS_BERTST_DONE field. At this point the error count can be read. The error count should not be read until the completion of the BER test, as this will clear the error counter and give incorrect results.

Table 36: BER Test Procedure

Step #	Step
1	Enable PRBS31 Checker Control by setting PCS_PRBS31MON_EN to 1 (Set WIS_PRBSMON_EN to 1 in WAN mode).
2	Program the PCS_FPRBS_VEN_CNT_MODE field (3.C000h[13]) to select between the 16-bit and 32-bit error counters. (In WAN mode set WIS_FPRBS_VEN_CNT_MODE field (2.C001[13]) 0 = 16 bit counter 1 = 32 bit counter
3	Set the timed BER test period, in seconds in PCS_BERTIMER_START field (3.C001h). The same timer field is used in both WAN and LAN modes.
4	Stop any previously running timed BER tests and clear counter by setting PCS_BERTST_EN to 0 (3.C000h[12])
5	Clear the counter by reading the contents.
6	Start timed BER test by setting PCS_BERTST_EN to 1.
7	Wait at least the timeout period. After the timeout period has passed, check PCS_BERTST_DONE to see if the test has finished (3.C000h[15], where 1 means test completed). **Note that this bit cannot be polled until the timeout period is over,** since polling it while the test is running may cause that bit not to be set. If the test has not completed before the polling, the test results should be discarded for that test period. The Timed BER Test will always complete as expected.
8	If test has finished, read the appropriate counter selected in Step 2.
9	Repeat steps 4 to 8 for multiple BER tests.

WIS Test Features

The WIS implements three serial test patterns for testing the PMA and PMD layers. These include a square wave test pattern, an unframed PRBS31 pattern, and a framed mixed frequency test pattern. These patterns are implemented in accordance with IEEE 802.3-2005 Clause 50.3.8.

WIS Square Wave Test Pattern

When the WIS square wave test pattern is enabled, the WIS Transmit block will output a continuous square wave pattern to the PMA. The square wave pattern is 00FFh (8 consecutive 1s followed by 8 consecutive 0s). Transmission is enabled by first setting the 'transmit test pattern enable' bit 2.0007h[1] to a 1. Then the square wave pattern is chosen by setting the 'test pattern select' bit 2.0007h[3] to a 1.

There is no pattern checker feature on the receive path for the square wave test pattern.

WIS Mixed Frequency Test Pattern

The mixed frequency test pattern consists of a framed WIS signal with a PRBS23 payload, plus a CID section (consecutive identical digits). The PRBS23 pattern is substituted for the payload data that would normally be sent in the WIS frame. The CID section is selected to stress the lock range of the receiver circuitry, and is placed in the Z0 octet locations as these are not scrambled. The complete Test Signal Structure of the signal is described in IEEE 802.3 Clause 50.3.8.3.

When transmission of the mixed frequency test pattern is enabled, the WIS Transmit block will continuously output the Test Signal Structure to the PMA. Transmission is enabled by first setting the 'transmit test pattern enable' bit 2.0007h[1] to a 1. Then the mixed frequency test pattern is chosen by setting the 'test pattern select' bit 2.0007h[3] to 0.

When the mixed frequency test pattern is received at the fiber input, errors are detected using the Line BIP Error Counter registers 2.0057h and 2.0058h (2.0039h and 2.003Ah), the Path Block Error Counter Register 2.0059h (2.003Bh) and the Section BIP Error Counter Register 2.0060h (2.003Ch).

The 'receive test pattern enable' bit 2.0007h[2] does not need to be set to 1 to enable error checking.

Ethernet Packet Generator/Checker

The QT2025 has the ability to generate data packets for test purposes. There is one such generator in the TX path and one in the RX path. To complement the generators, a packet checker is placed in the TX path and another one in the RX path.

Disabling the Idle Decode Process

The XGXS block of the chip converts the incoming XAUI signal from a 10 bit-encoded signal to an 8-bit encoded signal. The chip also decodes all the K28.0, K28.3 and K28.5 idle codes to the same 8-bit code, /I/ = 0x07h, as specified in IEEE 802.3-2005 Table 48-3. These idle codes will typically be transmitted to a far-end SerDes (such as another QT2025). The far-end SerDes will convert the 8-bit idle codes into 10-bit encoded K28.0, K28.3 and K28.5 codes, following the rules specified by the idle randomization process (as per IEEE 802.3 Clause 48.2.4.2). The original idle code order will not be preserved.

The XGXS idle decode process can be disabled by setting MDIO register bit 4.C007h[8] = 1. In this test mode, the K28.0, K28.3 and K28.5 codes are decoded to their native 8-bit code as given in IEEE 802.3 Table 49-1 (K28.0 -> 0x1C, K28.3 -> 0x7C, K28.5 -> 0xBC). There will be no idle codes, 0x07h, generated in the signal.

When this modified signal is passed through the receive path of the QT2025, the idle codes will pass through the chip unmodified. The idle randomization process will not operate on them. The 8b/10b encoder will convert them to their original 10-bit code words, thereby preserving the original order of the signal.

This feature is useful when testing the XAUI interface using an external pattern generator & error detector that is not protocol-aware and cannot handle the idle randomization normally. Note that the receive 8b/10b encoder process will choose one of two running disparities, depending on the signal. If the disparity does not match that expected by the external error detector, errors will be reported. Therefore, it is important to check for both possible disparities. For more information on disparity, consult IEEE-802.3 Clause 36.2.4.4; also review Clause 36.2.4.7.1 for 8b/10b valid code-groups. For information on disparity as it relates to CJPAT, consult IEEE 802.3 Clause 48A.5.1.

When the idle decode process is disabled, the rate compensation capability of the chip will fail to function properly. It fails because the rate compensation block operates on standard 8-bit idle codes, 0x07h, which are absent from the signal. Therefore, this feature should not be used during normal operation. To use this feature properly, supply a reference clock to the chip that is synchronous to the incoming signal. If an asynchronous reference clock is supplied and the chip must perform a rate compensation, error codes will be generated.

Test Access Port and Boundary Scan

The QT2025 has a test-access port (TAP) and a boundary scan (BSCAN) chain compliant with IEEE standards 1149.1 and 1149.6 (JTAG).

BSCAN chain

The following pins are on the BSCAN chain:

- AC pins: all XAUI I/O
- DC pins: all low-speed digital I/O

The following pins are *not* in the BSCAN chain:

- all supplies and grounds
- all lab test I/O (MONCVP/N, XPLLOUTP/N, FPLLOUTP/N)
- all 10G I/O (FRXIP/N, FTXOUTP/N)

TAP Port

Table 37 lists the supported BSCAN instructions while Table 38 lists the unsupported BSCAN instructions.

Table 37: Supported BSCAN Instructions

BSCAN Instruction	Value	Description
BYPASS	5'b11111	bypasses the bscan register
EXTEST	5'b00000	DC test of external connectivity to I/O
IDCODE	5'b00001	allows reading the device ID register
SAMPLE/PRELOAD	5'b00010	captures and updates data
RUNBIST	5'b00011	runs BIST on internal memories
DEBUGBIST	5'b00100	debug mode of memory BIST
SCAN	5'b01001	SCAN test on digital core
EXTEST_TRAIN	5'b00110	AC test of external connectivity to I/O
EXTEST_PULSE	5'b00101	AC test of external connectivity to I/O

Table 38: Unsupported BSCAN Instructions

BSCAN Instruction	Description
CLAMP	allows outputs to be forced to specific states during BYPASS
HIGHZ	allows outputs to be forced into high-z state
INTEST	allows testing of internal circuitry using BSCAN chain
USERCODE	allows a user-programmable ID code

Device ID Register

Table 39: Device ID Register

Field	Value
Manufacturer's ID code (11bits)	11'b0101_0110100
Part-number code (16 bits)	16'h2025 (16'b0010_0000_0010_0101)
Version code (4 bits)	4'hB (4'b1011)

Table 40: BSCAN Chain Implementation

Pins on BSCAN Chain	BSCAN Order	BSCAN Cell Captures/Drives	Pins on BSCAN Chain	BSCAN Order	BSCAN Cell Captures/Drives
RDCC	0	output	UC_SDA	36	output
RDCC_CLK	1	output	UC_SDA	37	input
TDCC	2	input	PRTAD0	38	input
TDCC_CLK	3	output	TXFAULT	39	input
EEPROM_PROT	4	input	RXLOSB_I	40	input
EEPROM_SCL	5	enable	LOSOUTB	41	output
EEPROM_SCL	6	output	RESETN	42	input
EEPROM_SCL	7	input	MDC	43	input
EEPROM_SDA	8	enable	MDIO	44	enable
EEPROM_SDA	9	output	MDIO	45	output
EEPROM_SDA	10	input	MDIO	46	input
XCDR3N	11	Input	LED3	47	enable
XCDR3P	12	Input	LED3	48	output
XCDR2N	13	Input	LED3	49	input
XCDR2P	14	Input	LED2	50	enable
XCDR1N	15	Input	LED2	51	output
XCDR1P	16	Input	LED2	52	input
XCDR0N	17	Input	LED1	53	enable
XCDR0P	18	Input	LED1	54	output
XDRV2	19	Output	LED1	55	input
XDRV2	20	AC/DC Select	GPIO2	56	enable
XDRV3	21	Output	GPIO2	57	output
XDRV3	22	AC/DC Select	GPIO2	58	input
XDRV1	23	Output	GPIO1	59	enable
XDRV1	24	AC/DC Select	GPIO1	60	output
XDRV0	25	Output	GPIO1	61	input
XDRV0	26	AC/DC Select	GPIO3	62	enable
TXENABLE	27	output	GPIO3	63	output
PRTAD2	28	input	GPIO3	64	input
PRTAD3	29	input	LTIMEOK	65	output
UC_SCL	30	enable	TXON	66	enable
UC_SCL	31	output	TXON	67	output

Table 40: BSCAN Chain Implementation (Continued)

Pins on BSCAN Chain	BSCAN Order	BSCAN Cell Captures/Drives	Pins on BSCAN Chain	BSCAN Order	BSCAN Cell Captures/Drives
UC_SCL	32	input	TXON	68	input
PRTAD1	33	input	LASI	69	output
PRTAD4	34	input	LASI_INTB	70	input
US_SDA	35	enable			

Ball Assignment and Description

Ball Arrangement

The QT2025 comes in a 13 x 13 mm^2 CABGA package with 1.0 mm ball pitch. This corresponds to a 12 x 12 (144) array of pins. The ball arrangement is shown in Figure 70 and the pin assignments are described in Table 41.

Table 41: QT2025 Ball Assignment & Signal Description

Ball	Signal Name	Dir.	Type	Description
CML OUTPUTS				
M4 M6	FTXOUTP FTXOUTN	O	CML	10Gbps mode: 9.95 - 10.5 Gbps transmit differential data outputs. 1.25 Gbps mode: 1.25 Gbps transmit differential data outputs 100Ω differential impedance. Must be externally AC coupled.
K12 J12	AOUTP AOUTN	O	CML	AGC/EDC inverted and non-inverted data output. For test purposes only. Leave unconnected when not used
E11 D11	XDRV0P XDRV0N	O	CML	10Gbps mode: 3.125 Gbps, 3.1875 Gbps differential output data; XAUI interface - lane 0 1Gbps mode: 1.25 Gbps transmit differential data outputs to MAC/switchΩ 100Ω differential impedance. Must be externally AC coupled.
C12 B12	XDRV1P XDRV1N	O	CML	3.125 Gbps, 3.1875 Gbps differential output data; XAUI interface - lane 1 100Ω differential impedance. Must be externally AC coupled. (Unused in 1.25Gbps mode)
A11 A10	XDRV2P XDRV2N	O	CML	3.125 Gbps, 3.1875 Gbps differential output data; XAUI interface - lane 2 100Ω differential impedance. Must be externally AC coupled. (Unused in 1.25Gbps mode)
B9 B8	XDRV3P XDRV3N	O	CML	3.125 Gbps, 3.1875 Gbps differential output data; XAUI interface - lane 3 100Ω differential impedance. Must be externally AC coupled. (Unused in 1.25Gbps mode)
J6 K6	FPLLOUTP FPLLOUTN	O	CML	Programmable sub-rate clock output. Can output a clock that is synchronous to the serial transmit signal or the serial receive signal. Available Options: 1. Tx div-by-64 (used in XFP applications as module reference clock) 2. Tx div-by-66 3. Rx div-by-66 (in 10GE mode) or Rx div-by-64 (in WAN mode) 100Ω differential impedance. Must be externally AC coupled.
C6 C7	XPLLOUTP XPLLOUTN	O	CML	Programmable sub-rate clock output. Can be programmed to output: 156.25MHz clock derived from EREFCLK (local reference clock) 125MHz clock (div-by-82.5) derived from receive recovered clock (from FRXI input). This clock is intended for use in Synchronous Ethernet applications. It is not intended for use in WAN applications. 100Ω differential impedance. Must be externally AC coupled.

Table 41: QT2025 Ball Assignment & Signal Description

Ball	Signal Name	Dir.	Type	Description
F1 F2	VCXOCTLP VCXOCTLN	O	CML	Phase-frequency detector output control voltage which drives the external loop filter as part of the VCXO control.
CML INPUTS				
M1 M2	EREFCLKP EREFCLKN	I	CML	LAN reference clock input for fiber-side TXPLL and XAUI PLL. 156.25 MHz or 52.083 MHz Internal on-chip 50 terminations to 1.2V. Must be externally AC-coupled.
K2 K1	SREFCLKP SREFCLKN	I	CML	SONET reference clock input for fiber-side TXPLL in WAN-mode. 155.52 MHz or 51.84 MHz Internal on-chip 50Ω terminations to 1.2V. Must be externally AC-coupled. May be used as a second LAN reference clock input
H2 H1	VCXOIP VCXOIN	I	CML	VCXO Clock input when an external VCXO is used for the fiber side reference clock input Internal on-chip 50Ω terminations to 1.2V. Must be externally AC-coupled.
M9 M11	FRXIP FRXIN	I	CML	10Gbps mode: 9.95 -10.5 Gbps serial receive data input. 1.25 Gbps mode: 1.25 Gbps serial receive data input, 100Ω differential impedance. Must be externally AC coupled.
B6 B5	XCDR0P XCDR0N	I	CML	10Gbps mode: 3.125 Gbps, 3.1875 Gbps differential input data; XAUI interface - lane 0 1.25 Gbps mode: 1.25 Gbps serial receive data in from MAC/switch 100Ω differential impedance. Must be externally AC coupled.
A4 A3	XCDR1P XCDR1N	I	CML	3.125 Gbps, 3.1875 Gbps differential input data; XAUI interface - lane 1 100Ω differential impedance. Must be externally AC coupled. (Unused in 1.25Gbps mode)
A1 B1	XCDR2P XCDR2N	I	CML	3.125 Gbps, 3.1875 Gbps differential input data; XAUI interface - lane 2 100Ω differential impedance. Must be externally AC coupled. (Unused in 1.25Gbps mode)
C2 D2	XCDR3P XCDR3N	I	CML	3.125 Gbps, 3.1875 Gbps differential input data; XAUI interface - lane 3 100Ω differential impedance. Must be externally AC coupled. (Unused in 1.25Gbps mode)
DC MONITOR POINTS				
K7 J7	MONCVP MONCVN	O	analog	Monitor test point for the transmit XAUI (XCDR) interface (DC signal). EDC DAC testport. Used for monitoring only. Leave unconnected.
CONNECTION POINTS FOR EXTERNAL COMPONENTS				
A7	BIAS		analog	Chip bias resistor Place an external 10kΩ resistor to XV1P2
K4 J4	FTXFP FTXFN		analog	Fiber Tx PLL. Place a 10 nF cap between FTXFP and FTXFN pins
J8 K8	FRXFP FRXFN		analog	Fiber Rx PLL. Place a 100 nF cap between FRXFP and FRXFN pins

Table 41: QT2025 Ball Assignment & Signal Description

Ball	Signal Name	Dir.	Type	Description
CMOS INPUTS (note all CMOS inputs are 3.3V tolerant and all CMOS inputs with internal pullups are to 1.2V				
E4	TDCC	I	CMOS	WIS Mode Transmit data communication channel input for both section and line SONET overhead data; clocked in using the TDCC_CLK output.
E10	RXLOSB_I (RXLOS)	I	CMOS with internal 50kΩ pullup to 1.2V	Receive loss of signal indicator input (can be driven directly by LOSOUTB or by an external source) RX_LOS input from XFP module or SFP+ module For external modules: High = insufficient optical power. For XENPAK: Low = insufficient optical power.
D6	EEPROM_PROT (MODABS)	I	CMOS with internal 50kΩ pullup to 1.2V	MOD_ABS input for XFP module or SFP+ module. High level indicates module absent
F10	MDC	I	CMOS with hysteresis (min=100 mV)	MDIO interface clock
E2	LASI_INTB (XFPINTB)	I	CMOS with internal 50kΩ pullup to 1.2V	Module Interrupt input. Active low interrupt input indicates XFP module fault condition.
D10	TXFAULT (XFPMODNR)	I	CMOS with internal 50kΩ pullup to 1.2V	Mod_NR Status input for XFP module, or TX_Fault input for SFP+ module High level indicates XFP module fault
C10 C9 C8 D8 D9	PRTAD0 PRTAD1 PRTAD2 PRTAD3 PRTAD4	I	CMOS no pullup or pulldown	Port Address Field for MDIO transactions.
F12	RESETN	I	CMOS with internal 50kΩ pullup to 1.2V	reset, active low logic low = reset condition logic high = normal operation Note: the TAP port controller is only reset by the TRST_N pin and is unaffected by RESETN
			CMOS	Test pins for Test Access Port (*or internal scan testing when SCAN instruction written to TAP*).
C5 E3 D3	TDI TCK TRST_N	I I I	50kΩ pu (no pu/dn) 50kΩ pu	Test data input (*scan in*) Test clock input (*scan clock*) Test reset, active low (*hold high for scan*). Hold TRST_N low when boundary scan not in use.
C4	TMS	I	50kΩ pu	Test mode select, active low (*hold high for scan*)

Table 41: QT2025 Ball Assignment & Signal Description

Ball	Signal Name	Dir.	Type	Description
CMOS OUTPUTS (note: all CMOS outputs are 3.3V tolerant open drain)				
G4	LTIMEOK	O	CMOS open drain[1]	Line-timing internal enable indication. logic high = conditions are valid for line-timing operation and it is internally enabled. A logic low level can be used to center the external VXCO in a VXCO-only application.WIS Mode
D4	RDCC	O	CMOS open drain[1]	WIS Mode Receive data communication channel output for both section and line SONET overhead data; timed from the RDCC_CLK clock output.
D5	RDCC_CLK	O	CMOS open drain[1]	WIS Mode Gapped clock used for timing RDCC output.
E5	TDCC_CLK	O	CMOS open drain[1]	WIS Mode Gapped clock used for timing TDCC input.
C3	TDO	O	CMOS open drain[1]	Test data output (*scan out when SCAN instruction written to TAP).* Requires external pullup.
E1	LASI	O	CMOS open drain	Link Alarm Status Interrupt (LASI) logic low = Interrupt asserted logic high =No alarm interrupt asserted
D7	TXENABLE (XFPTXDIS)	O	CMOS open drain	Drives TX_DIS input of XFP module, or TXDISABLE input of SFP+ module
E12	LOSOUTB (XFPPDN)	O	CMOS[1] open drain	drives P_DOWN/RST input of XFP module
E8	UC_SCL	O	CMOS. Open Drain	Microcontroller I2C clock Connect to SCL of the external EEPROM when used to store microprocessor firmware Connect to SCL of XFP/SFP+ module
BIDIRECTIONAL CMOS IO (note: all CMOS I/O are 3.3V tolerant & outputs are open drain)				
E7	EEPROM_SCL	I/O	CMOS[1] bidirectional open drain with hysteresis	EEPROM_I2C clock Connect to NVR/DOM devices and boot EEPROMs.
E6	EEPROM_SDA	I/O	CMOS[1] bidirectional open drain with hysteresis	EEPROM_I2C data Connect to NVR/DOM devices and boot EEPROMs.
E9	UC_SDA	I/O	CMOS. Open Drain bidirectional	Microcontroller I2C data Connect to SDA of the external EEPROM when used to store microprocessor firmware Connect to SDA of XFP/SFP+ module

Table 41: QT2025 Ball Assignment & Signal Description

Ball	Signal Name	Dir.	Type	Description
G10	MDIO	I/O	CMOS bidirectional push-pull or Open drain	MDIO Interface serial data signal.
F4	TXON (XFPMODDESEL)	I/O	CMOS output	XFP Module Application: output to drive the MOD_DESEL input of an XFP module SFP+ Module Application: unused.
MISCELLANEOUS				
K11 J11 H4	GPIO1 GPIO2 GPIO3	I/O	CMOS bidirectional open drain with internal 50kΩ pullup to 1.2V	General purpose I/O's SFP+ Applications: Connect GPIO1 to RS0 of SFP+ module Connect GPIO2 to RS1 of SFP+ module
G11 G12 H12	LED1 LED2 LED3	I/O	CMOS input or 10 mA open drain output	LED Drivers and General purpose I/O The outputs can control external LEDs to display link status and activity. Associated path (Tx or Rx) and status/activity display can be individually programmed. Defaults: LED1: Receive path Status/activity LED2: Transmit path Status/activity LED3: Receive path Status only. LED2: when the LED2 pin is pulled to a logic low level when the chip is released from reset, the EEPROM_SDA/EEPROM_SCL I2C bus will use 1-byte addressing. After the chip is released from reset, LED2 can be used for other purposes.
H10	VTERM	I	Supply	MDIO (push/pull) supply voltage. 1.1 -3.3V If there is an external pullup on MDIO, ensure VTERM >= Vpullup
RESERVED PINS				
G1,G2, J10				Reserved. Leave Unconnected

1. All CMOS pins are compatible with 3.3V logic. All CMOS inputs with internal pullups are pulled up to 1.2V. All CMOS outputs are open drain with the exception of MDIO which is a push-pull configuration by default but can configured as an open drain if desired

Table 42: Supply Pad and Ball Assignment and Description

Supply (#)	Description	Balls
FRXV1P2 (4)	1.2V Supply for Receive Fiber Side Circuits	L7,L8,L9,L10
FTXV1P2 (4)	1.2V Supply for Transmit Fiber Side Circuits	L3,L4,L5,L6
GND (38)	Ground [1]	A2,A5,A9,A12,B2,B3,B4,B10,B11,C1,C11,D1, D12,F5,F6,F7,F8,F11,G5,G6,G7,G8,H5,H6,H7,H8,H11,J1,J2,L1,L2,L12, M3,M5,M7,M8,M10, M12
FRXV1P2A (1)	1.2V Supply for Receive PLL	J9
FTXV1P2A (1)	1.2V Supply for Transmit PLL	K3
XV1P2 (2)	1.2V Supply for XAUI Side	A6, A8
XV1P2A (1)	1.2V Analog Supply for XAUI Side (new!)	B7
FRXV1P8 (2)	1.8V Supply for Receive Fiber	K10,L11
FTXVTERM (2)	1.8V Supply for Transmit Fiber	J5,K5
COREVDD (6)	1.2V Supply for CMOS Digital Logic	F3,G3,H3,F9,G9,H9
FRXGNDA (1)	Receive fiber Analog Ground	K9
FTXGNDA (1)	Transmit fiber Analog Ground	J3

1. The following GND pins are also thermal balls (12) that are connected to the back side of the die: F5,F6,F7,F8,G5,G6,G7,G8,H5,H6,H7,H8.

Ball Map Arrangement

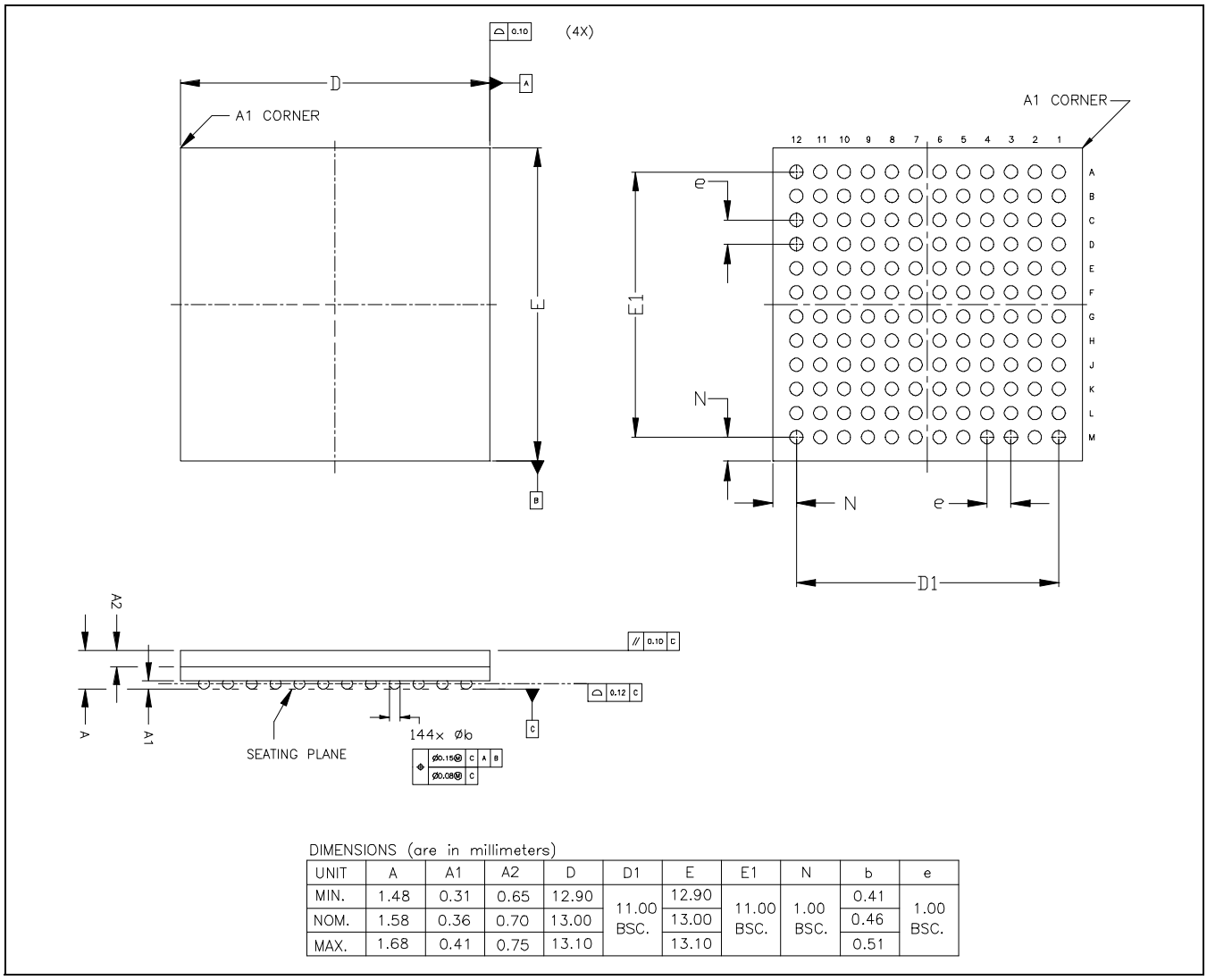
Figure 70: QT2025 Ball Arrangement (TOP VIEW, THROUGH THE PACKAGE)

	1	2	3	4	5	6	7	8	9	10	11	12
A	XCDR2P	GND	XCDR1N	XCDR1P	GND	XV1P2	BIAS	XV1P2	GND	XDRV2N	XDRV2P	GND
B	XCDR2N	GND	GND	GND	XCDR0N	XCDR0P	XV1P2A	XDRV3N	XDRV3P	GND	GND	XDRV1N
C	GND	XCDR3P	TDO	TMS	TDI	XPLLOUTP	XPLLOUTN	PRTAD2	PRTAD1	PRTAD0	GND	XDRV1P
D	GND	XCDR3N	TRST_N	RDCC	RDCC_CLK	EEPROM_PROT	TXENABLE	PRTAD3	PRTAD4	TXFAULT	XDRV0N	GND
E	LASI	LASI_INTB	TCK	TDCC	TDCC_CLK	EEPROM_SDA	EEPROM_SCL	UC_SCL	UC_SDA	RXLOSB_I	XDRV0P	LOSOUTB
F	VCXO CTLP	VCXO CTLN	COREVDD	TXON	GND	GND	GND	GND	COREVDD	MDC	GND	RESETN
G	UNUSED	UNUSED	COREVDD	LTIMEOK	GND	GND	GND	GND	COREVDD	MDIO	LED1	LED2
H	VCXOIN	VCXOIP	COREVDD	GPIO3	GND	GND	GND	GND	COREVDD	VTERM	GND	LED3
J	GND	GND	FTXGNDA	FTXFN	FTX VTERM	FPLLOUTP	MONCVN	FRXFP	FRXV1P2A	RESERVED	GPIO2	AOUTN
K	SREFCLKN	SREFCLKP	FTXV1P2A	FTXFP	FTX VTERM	FPLLOUTN	MONCVP	FRXFN	FRXGNDA	FRXV1P8	GPIO1	AOUTP
L	GND	GND	FTXV1P2	FTXV1P2	FTXV1P2	FTXV1P2	FRXV1P2	FRXV1P2	FRXV1P2	FRXV1P2	FRXV1P8	GND
M	EREFCLKP	EREFCLKN	GND	FTXOUTP	GND	FTXOUTN	GND	GND	FRXIP	GND	FRXIN	GND

Mechanical Specifications

The QT2025 is housed in a cavity up 13x13mm BGA package.

Figure 71: QT2025 – 144 BGA Package Mechanical Drawing



DIMENSIONS (are in millimeters)

UNIT	A	A1	A2	D	D1	E	E1	N	b	e
MIN.	1.48	0.31	0.65	12.90	11.00 BSC.	12.90	11.00 BSC.	1.00 BSC.	0.41	1.00 BSC.
NOM.	1.58	0.36	0.70	13.00		13.00			0.46	
MAX.	1.68	0.41	0.75	13.10		13.10			0.51	

PACKAGE MATERIAL NOTE:
Standard Package: Ball Composition - 63/37 Sn/Pb.
Green / RoHS Compliant Package: Ball Composition- 96.5/3.0/0.5 Sn/Ag/Cu

Table 43: Thermal Management

Device	θjb	θjc	θja with airflow, expressed in linear feet per minute (lfm):		
QT2025	17.7 ℃/Watt	7.2 ℃/Watt	0 lfm: 32.1 ℃/Watt	100 lfm: 26.1 ℃/Watt	200 lfm: 23.8 ℃/Watt

Thermal modelling is based on a 1S2P multilayer JEDEC standard (100x100mm), 1.6mm FR4 PCB.
A heatsink is required for ambient temperatures above 60°C.

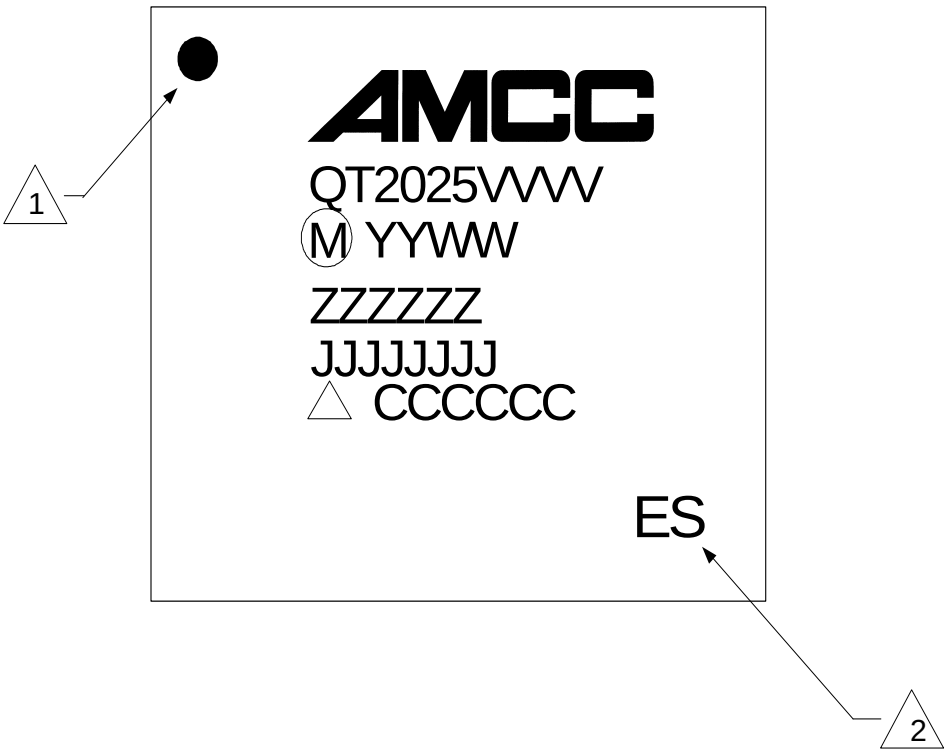
Package Marking Drawing

Figure 72: QT2025 – 144 PBGA Package Marking Drawing

NOTES (Unless Otherwise Specified):

1. Dot Represents PIN1 (A01) Designator

2. ES (Engineering Sample) designator. When present, this signifies pre-production grade material. Pre-production material is not guaranteed to meet the specifications in this document.



LEGEND (in row order - including symbols):

ROW #1:		AMCC Logo
ROW #2:		AMCC Device Part Number VVVVVV. Listed options (See ordering Information)
ROW #3:	(M)	Mask Protection Symbol YY: Assembly Year Code WW: Assembly Week Code
ROW #4:		ZZZZZZ: AMCC 6: Digit Lot Code
ROW #5:		JJJJJJJJ: Assembly Sub-contractor lot code, up to 8 characters
ROW #6:	△	ESD Symbol CCCCCC: Assembly Location (Country of Origin)
ROW #7:		Engineering Sample (ES) Designator (only on Pre-Production Devices).

Performance Specifications

Table 44: Common Serial Transmitter Specifications (FTXOUTP, FTXOUTN)

Description	Min	Typ	Max	Units	Conditions/Notes
Nominal Bit Rate	9.95	10.3125	10.52	Gbps	WAN (SREFCLK=155.52MHz) 10GE (EREFCLK=156.25MHz) 10GFC (EREFCLK=159.375MHz)
Transmitter Coupling		AC			
Output Rise and Fall Time	24		47	ps	20% to 80%
Output Impedance		50		Ω	Single-Ended
		100		Ω	Differential
Zm Termination / Single-ended impedance mismatch Measured at point A from SFF-8431			5	%	Measured as specified in SFF-8431 Appendix D.16
SDD22 Differential Output Return Loss [1] Measured at point A from INF-8077i	12			dB	0.01 - 2.8 GHz
	DORL			dB	DORL = 8.15 - 13.33*Log10 (f/5.5) f is in GHz 2.8 < f < 11.1 GHz
SCC22 Common Mode Return Loss [1] Measured at point A from INF-8077i	9			dB	0.01 - 4.74 GHz
	CRL			dB	CRL = 8.15 - 13.33*Log10(f/5.5) f is in GHz 4.74< f < 11.1GHz
Driver Control Stepsize		10		mV	

1. This Datasheet specification is compliant to the SFP+ Standard (SFF-8431). This is compliant to a draft of the Fibre Channel Physical Interface-3 Standard (INCITS/Project 1647-D/Rev D2.0) but is not compliant to the current published XFP Standard (INF-4077i Revision 4.5). It is expected that these draft specifications will be adopted by the XFP Standard in future. This specification meets or exceeds the requirements for all other applications.

Table 45: SFI 10Gbps Serial Transmitter Specifications

Description	Min	Typ	Max	Units	Conditions/Notes
Output AC Common Mode Voltage Measured at point B from SFF-8431			15	mVrms	
X1,X2,Y1,Y2 Mask Values Measured at point B from SFF-8431			0.14	UI	X1 per Figure 73
			0.35	UI	X2 per Figure 73
	90			mV	Y1 per Figure 73
			350	mV	Y2 per Figure 73
TJ Total Jitter Measured at point B from SFF-8431			0.28	UIpp	Using IEEE 802.3 Clause 52.9 pattern 1, pattern 3 or valid 64/66 data. Measure in accordance with SFF-8431 Section D.5
DDJ Data dependent jitter Measured at point B from SFF-8431			0.10	UIpp	With network driver taps optimized. Measured in accordance with SFF-8431 Section D.3

Table 45: SFI 10Gbps Serial Transmitter Specifications

Description	Min	Typ	Max	Units	Conditions/Notes
DCD Duty cycle distortion Measured at point B from SFF-8431			0.035	UIpp	
DDPWS Data Dependent Pulse Width Shrinkage Measured at point B from SFF-8431			0.055	UI	With network driver taps optimized. Measured in accordance with SFF-8431 Section D.3
UJ Uncorrelated jitter [1] Measured at point B from SFF-8431			0.023	UIrms	Measured in accordance with SFF-8431 Section D.5

1. UJ includes all jitter that is not DDJ.

Table 46: XFI 10Gbps Serial Transmitter Specifications

Description	Min	Typ	Max	Units	Conditions/Notes
Amplitude at maximum drive setting [1]		600		mVpp	Max drive when FTX_DATA_LVL = 0x3F (address 1.C308.5:0)
Differential Eye Opening Measured at point A from INF-8077i	360			mVppd	
Differential Output Swing Measured at point A from INF-8077i			770	mVppd	
Output AC common mode voltage Measured at point A from INF-8077i			15	mVrms	
TJ Total Jitter Measured at point A from INF-8077i			0.30	UIpp	See Figure 73
DJ Deterministic Jitter Measured at point A from INF-8077i			0.15	UIpp	
X1,X2,Y1,Y2 Mask Values Measured at point A from INF-8077i			0.15	UI	X1 per Figure 73
			0.40	UI	X2 per Figure 73
	180			mV	Y1 per Figure 73
			385	mV	Y2 per Figure 73
Telecom Jitter Generation			6.5	mUIrms	WAN mode: 50kHz - 8MHz

1. Amplitude is per side and measured differentially.

Table 47: Backplane (KR) 10Gbps Serial Transmitter Specifications [1]

Description	Min	Typ	Max	Units	Conditions/Notes
Output Voltage			1200	mVppd	Differential
Driver Disabled Output Level			30	mVppd	Differential
Common Mode Voltage	0		1.9	V	

Table 47: Backplane (KR) 10Gbps Serial Transmitter Specifications [1]

Description	Min	Typ	Max	Units	Conditions/Notes
Total Jitter, TJ			0.28	UIpp	BER = 1e-12
Deterministic Jitter, DJ			0.15	UIpp	BER = 1e-12
Duty Cycle Distortion			0.035	UIpp	Duty Cycle Distortion is considered part of the deterministic jitter distribution.
Random Jitter			0.15	UIpp	
Voltage Absolute Stepsize	5	10	20	mV	Measured on the v2 voltage, as defined in Fig. 74. Measured with a main driver amplitude (FTX_DATA_LVL) setting of 54 or less.
Main Driver Output Swing	400		600	mVp	Highest Setting: C(main) at maximum setting for KR applications C(pre)=0 and C(post1)=0 Measured with low frequency pattern.
	220		330	mVp	Lowest Setting: C(main) at minimum setting for KR applications C(pre)=0 and C(post1)=0 Measured with low frequency pattern.
Post-Cursor Ratio (R_{PST})	4				Rpst = v1/v2 With C(post1) and C(main) at minimum and C(pre) disabled
Pre-Cursor Ratio (R_{PRE})	1.54				Rpre = v3/v2 With C(pre) and C(main) at minimum and C(post1) disabled
Waveform Ripple			40	mVpp	For any combination of C(pre), C(main) and C(post1)

1. Transmitter characteristics specified at chip output, equivalent to point TP1 as defined in IEEE 802.3ap-2007 Figure 72-1.

Table 48: SFI 1.25Gbps Serial Transmitter Specifications

Description	Min	Typ	Max	Units	Conditions/Notes
Nominal Bit Rate		1.25		Gbps	1GbE
Output rise and fall times	85		300	ps	20% to 80%, low frequency pattern
Peak to peak output voltage[1] Measured at point A from SFF-8431			1200	mVppd	Differential
Eye opening [2] Measured at point A from SFF-8431	600			mVppd	Differential
X1,X2,Y1,Y2 Mask Values Measured at point A from SFF-8431			0.11	UI	X1. Per Figure 73
			0.23	UI	X2. Per Figure 73
	300			mV	Y1. Per Figure 73
			600	mV	Y2. Per Figure 73
TJ Total Jitter Measured at point A from SFF-8431			0.22	UIpp	Based on 1000BASE-SX/LX TP1 jitter at the SFP+ connector. [3] Jitter is measured with a 637 kHz high pass filter Measured with worst case jitter applied to XCDR input. RJmax = 0.22UI - measured DJ
DJ Deterministic jitter Measured at point A from SFF-8431			0.08	UIpp	
RJ Random jitter Measured at point A from SFF-8431			RJmax	UIpp	

1. SFP MSA allows for a maximum voltage level of 2000 mVpp, however, to save power it also recommends keeping the signal level below 1200mVpp
2. SFP MSA specifies a minimum voltage of 250mVpp at the input to the module. The SFP+ MSA reference channel has up to 8.5dB of loss at 5.5GHz. The loss should scale linear with rate from 5.5 GHz to 1.25/2 GHz to around 1dB loss.
3. In order to guarantee the jitter requirements, the power supply noise must be managed. AMCC recommends maintaining the power supply noise below 10mVpp measured through a bandpass filter with lower and upper corner frequencies of 500kHz and 2000kHz, respectively, and a stop band roll-off of 20dB per decade.

Table 49: Backplane (KX) 1.25Gbps Serial Transmitter Specifications

Description	Min	Typ	Max	Units	Conditions/Notes
Nominal Bit Rate		1.25		Gbps	1GbE
Tx Output Mask			0.125	UI	Based on maximum TJ. X1 per Figure 73
			0.325	UI	X2 per Figure 73
	400			mV	Y1 per Figure 73
			800	mV	Y2 per Figure 73
Output Voltage			1600	mVppd	Differential
Eye Opening	800			mVppd	Differential
Output Rise and Fall Times	60		230	ps	20% to 80%
Common Mode Voltage	-0.4		1.9	V	
Total Jitter			0.25	UIpp	RJmax = 0.25 - measured DJ See footnotes [1] [2] [3] [4]
Deterministic Jitter			0.10	UIpp	
Random Jitter			RJmax	UIpp	

1. Measured with bathtub curve, high pass of 750kHz, crossing times at DC when AC coupled, pattern as defined in IEEE 802.3ap Clause 59.7.1. See Clause 70.7.1.9 for details.
2. Measured with worst case jitter applied to TX path backplane input.
3. DC blocking is required between the transmitter and receiver.
4. In order to guarantee the jitter requirements, the power supply noise must be managed. AMCC recommends maintaining the power supply noise below 10mVpp measured through a bandpass filter with lower and upper corner frequencies of 750kHz and1500kHz, respectively, and a stop band roll-off of 20dB per decade.

Table 50: XAUI 1.25Gbps Serial Transmitter Specifications

Applies to XAUI Lane0 Output (for all 1GbE applications including Backplane and SFP)

Description	Min	Typ	Max	Units	Conditions/Notes
Nominal Bit Rate		1.25		Gbps	1GbE
X1,X2,Y1,Y2 Mask Values Measured at point A from INF-8077i			0.2	UI	X1 per Figure 73
			0.35	UI	X2 per Figure 73
	180			mV	Y1 per Figure 73
			385	mV	Y2 per Figure 73
Output rise and fall times	24 [1]		140	ps	20% to 80%, low frequency pattern
Peak to peak output voltage Measured at point A from INF-8077i			770	mVpp	
Eye opening Measured at point A from INF-8077i	360			mVpp	

Table 50: XAUI 1.25Gbps Serial Transmitter Specifications

Applies to XAUI Lane0 Output (for all 1GbE applications including Backplane and SFP)

Description	Min	Typ	Max	Units	Conditions/Notes
TJ Total Jitter Measured at point A from INF-8077i			0.40	UIpp	Jitter is measured with a 637 kHz high pass filter [2] Measured with worst case jitter applied to FRXI input. RJmax = 0.40UI - measured DJ
DJ Deterministic jitter Measured at point A from INF-8077i			0.16	UIpp	

1. Transition time minimum is the same as for 10G mode since the interface is to be compatible with 10G signals.

2. In order to guarantee the jitter requirements, the power supply noise must be managed. AMCC recommends maintaining the power supply noise below 10mVpp measured through a bandpass filter with lower and upper corner frequencies of 500kHz and 2000kHz, respectively, and a stop band roll-off of 20dB per decade.

Figure 73: Compliance Eye Mask

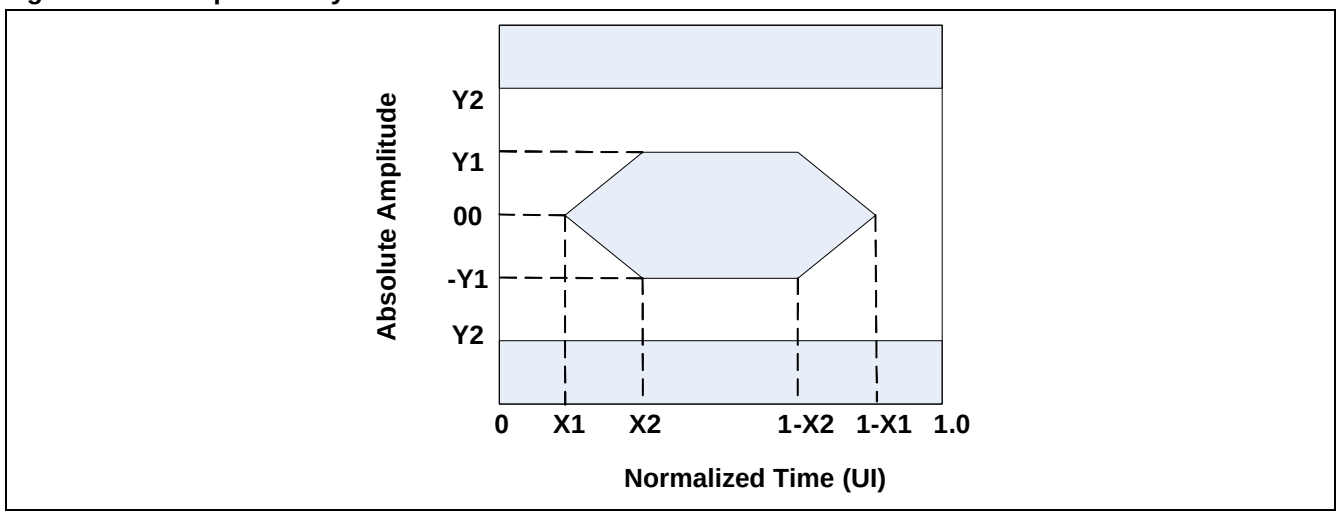


Figure 74: 10G KR Backplane Waveform Definition

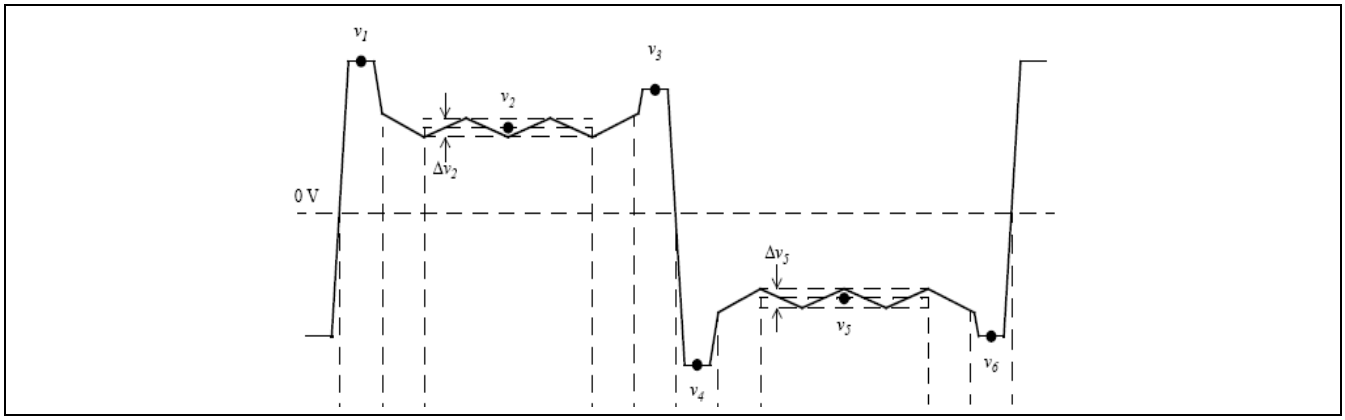


Table 51: Common Receiver Specifications (FRXIP, FRXIN)

Description	Min	Typ	Max	Units	Conditions/Notes
Nominal Bit Rate	9.95	10.3125 1.25	10.52	Gbps	WAN, 10GE & 10GFC 1GE
Baud Rate Tolerance	-100		+100	ppm	
Receiver Coupling		AC			
Zse, Zd Input impedance		50		Ω	Single-ended
		100		Ω	Differential
Rm/Zm Input resistance/impedance mismatch			5	%	
SDD11 Differential input S-parameter [1] Measured at point D from SFF-8431	12			dB	0.01 - 2.8 GHz
	SDIRL			dB	SDIRL = 8.15 - 13.33*Log10(f/5.5) where f is in GHz 2.8 < f < 11.1GHz
SCC11 Common-mode input S-parameter [1] Measured at point D from INF-8077i	6			dB	0.1 - 10 GHz
	4			dB	10 - 15 GHz
SCD11 Differential to common-mode conversion Measured at point D from SFF-8431	15			dB	0.01 - 11.1 GHz
Signal Acquire Time			200	ms	From application of input data and de-assertion of RXLOSB_I

1. This Datasheet specification is compliant to the SFP+ Standard (SFF-8431). This is compliant to a draft of the Fibre Channel Physical Interface-3 Standard (INCITS/Project 1647-D/Rev D2.0) but is not compliant to the current published XFP Standard (INF-4077i Revision 4.5). It is expected that these draft specifications will be adopted by the XFP Standard in future. This specification meets or exceeds the requirements for all other applications.

Table 52: SFI 10Gbps Receiver Specifications Supporting Limiting Modules

The specification assumes the channel from the module output to the receiver input meets SFF-8431 Revision 3.2 Appendix A.

Description	Min	Typ	Max	Units	Conditions/Notes
Input Swing Measured at point C" from SFF-8431			425	mVpp SE	Applied per-side, referenced into an ideal 50Ω load. Signal must be differential.
Eye Opening Measured at point C" from SFF-8431	150			mVpp SE	Applied per-side, referenced into an ideal 50Ω load. Signal must be differential.
Input Rise and Fall time (Tr, Tf) Measured at point C" from SFF-8431		34		ps	20% to 80%
DJ Deterministic Jitter[1] Measured at point C" from SFF-8431			0.42	UIpp	

Table 52: SFI 10Gbps Receiver Specifications Supporting Limiting Modules

The specification assumes the channel from the module output to the receiver input meets SFF-8431 Revision 3.2 Appendix A.

Description	Min	Typ	Max	Units	Conditions/Notes
DDPWS Pulse Width Shrinkage Jitter Measured at point C" from SFF-8431			0.3[2]	UIpp	
TJ[1] Total Jitter Measured at point C" from SFF-8431			0.70	UIpp	
Eye Mask, X1 Measured at point C" from SFF-8431			0.35		X1 per Figure 77
Eye Mask Amplitude Sensitivity, Y1 [3] Measured at point C" from SFF-8431	150			mV	Y1 per Figure 77
Eye Mask Amplitude Sensitivity, Y2 Measured at point C" from SFF-8431			300 [4]	mV	Y2 per Figure 77
Eye Mask Amplitude Overload, Y1 Measured at point C" from SFF-8431	212 [4]			mV	Y1 per Figure 77
Eye Mask Amplitude Overload, Y2 Measured at point C" from SFF-8431			425	mV	Y2 per Figure 77
AC Common Mode Voltage Tolerance	15			mVrms	
Jitter Amplitude Tolerance	Figure 78				Mask applied as per Figure 78

1. DJ specification includes 0.05UI of sinusoidal jitter defined at a frequency well above the reference CDR frequency e.g. 20MHz. For lower SJ frequencies, the receiver tracks additional SJ following the mask in Figure 78, such that, for any given frequency, TJ = 0.7UI - (high frequency SJ) + SJ tolerance mask.
2. In practice the PWS may be traded with other pulse width shrinkage from the sinusoidal interferer.
3. The Amplitude Sensitivity mask is intended to specify the minimum eye size the interface is required to support, while the Amplitude Overload mask is intended to specify the maximum eye size the interface is required to support. It is not the intent that the input eye simultaneously meet the minimum eye opening (150mV) and maximum eye swing (425mV).
4. This value is not yet defined in the SFP+ Standard. The ratio of peak-to-peak voltage to eye opening is expected to be less than a factor of 2x.

Table 53: SFI 10Gbps Receiver Specifications Supporting Linear Modules

The specification assumes the medium meets SFF-8431 Revision 2.0 Appendix A.

Description	Min	Typ	Max	Units	Conditions/Notes
VMA Differential Voltage Modulation Amplitude Measured at point C" from SFF-8431	180		600	mVppd	Signal must be differential, referenced into an ideal 100Ω load
Input Rise and Fall time (Tr, Tf) Measured at point C" from SFF-8431		34		ps	20% to 80%
WDP Waveform Distortion Penalty for host supporting an LRM module [1] Measured at point C" from SFF-8431		4.6			For Pre-Cursor Stressor with Relative Noise (RN) = 0.030 UIrms
		5.2			For Symmetric Stressor with Relative Noise (RN) = 0.0135 UIrms
		4.7			For Post-Cursor Stressor with Relative Noise (RN) = 0.030 UIrms
AC Common Mode Voltage Tolerance	15			mVrms	

1. Compliance stress test conditions. WDP is calibrated with reference receiver with FFE/DFE (14/5) defined in IEEE 802.3aq Clause 68.6.6.2.

Table 54: SFI 10Gbps Receiver Specifications Supporting SFP+ Direct Attach Cables

The specification assumes the medium meets SFF-8431 Revision 2.0 Appendix A.

Description	Min	Typ	Max	Units	Conditions/Notes
VMA Differential Voltage Modulation Amplitude Sensitivity Measured at point C" from SFF-8431	180			mVppd	Signal must be differential, referenced into an ideal 100Ω load VMA is defined in SFF-8431 Section D.7
Differential Peak to Peak Voltage			700	mVppd	Signal must be differential, referenced into an ideal 100Ω load
Receiver Sensitivity Test Conditions [1]					
WDPc Waveform Distortion Penalty [2] Measured at point C" from SFF-8431			9.3	dBe	
Transmitter Qsq	63.1				The noise at the transmitter is white over the 12GHz bandwidth of the measurement.
Post Channel Fixed Noise Source (N_0)			2.14	mVrms	The noise is white over the 12GHz bandwidth of the measurement.

1. The test conditions assume a noise model shown in Fig. 75.
2. WDP is calibrated with reference receiver with FFE/DFE (14/5) defined in IEEE 802.3aq Clause 68.6.6.2.

Figure 75: Block Diagram of Copper Stressor Noise Model

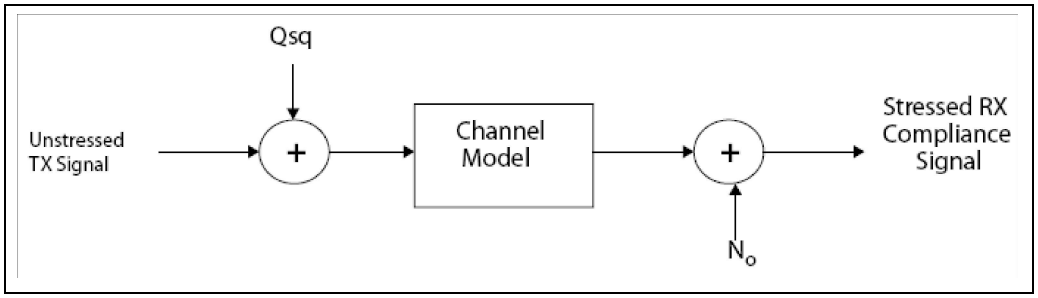


Table 55: Backplane (KR) 10Gbps Receiver Specifications

Description	Min	Typ	Max	Units	Conditions/Notes
Input Amplitude Range			1200	mVppd	Applied differentially, referenced into an ideal 50Ω load
Input Amplitude Tolerance	1600			mVppd	Damage threshold, applied differentially.
IEEE 802.3ap Annex 69A Stress Conditions [1]					
Full Loss Channel (Test 1)					
m_{TC}	1.0				Equation (69A-6) of Annex 69A, IEEE 802.3ap
Amplitude for Broadband Noise	5.2			mVrms	
Transition Time		47		ps	20%-80%
Applied Sinusoidal Jitter	0.115			UIpp	
Applied Random Jitter	0.130			UIpp	Specified at BER of 10^{-12}
Applied Duty Cycle Distortion	0.035			UIpp	
Half Loss Channel (Test 2)					
m_{TC}	0.5				Equation (69A-6) of Annex 69A, IEEE 802.3ap
Amplitude for Broadband Noise	12			mVrms	
Transition Time		47		ps	20%-80%
Applied Sinusoidal Jitter	0.115			UIpp	
Applied Random Jitter	0.130			UIpp	Specified at BER of 10^{-12}
Applied Duty Cycle Distortion	0.035			UIpp	

1. Consult the Errata concerning the test methodology for the Stress Conditions used to characterize the PHY.

Table 56: Backplane (KX) 1.25Gbps Serial Receiver Specifications[1]

Applies to FRXIP/N Input for Backplane Applications

Description	Min	Typ	Max	Units	Conditions/Notes
Nominal Bit Rate		1.25		Gbps	1GbE
Bit Rate Tolerance	-100		+100	ppm	
Input Voltage			1600	mVpp	Differential
Receiver Coupling		AC			
RTT Relative Channel Loss Slope	1.0				

Table 56: Backplane (KX) 1.25Gbps Serial Receiver Specifications[1]

Applies to FRXIP/N Input for Backplane Applications

Description	Min	Typ	Max	Units	Conditions/Notes
RTT Amplitude of Broadband Noise	8.6			mVrms	
RTT Transmitter Transition Time	320			ps	
RTT Applied Sinusoidal Jitter	0.10			UIpp	
RTT Applied Random Jitter	0.15			UIpp	
RTT Applied Duty Cycle Distortion	0			UI	
CDR Lock Time at Start-up			45	ms	from application of data

1. RTT is Receiver Tolerance Test as defined in IEEE 802.3ap Annex 69A. See also Clause 70.7.2.1.
10^{-12} target BER is measured with FEC disabled

Table 57: SFI 1.25Gbps Serial Receiver Specifications

Applies to FRXIP/N Input for SFP Module Applications

Description	Min	Typ	Max	Units	Conditions/Notes
Nominal bit rate		1.25			1GE 8B/10B Encoded
Bit rate tolerance	-100		+100	ppm	Relative to nominal bit rate
Receiver Coupling		AC			
Peak to peak input voltage Measured at point D from SFF-8431			2000	mVppd	Per INF-8074i With eye opening > 1Vppd [1]
Eye Opening [2] Measured at point D from SFF-8431	300			mVppd	With peak-to-peak input voltage <600mVppd
X1,X2,Y1,Y2 Mask Values [2] Measured at point D from SFF-8431			0.38	UI	X1 per Figure 73
			0.43	UI	X2 per Figure 73
	150			mV	Y1 per Figure 73
			1000	mV	Y2 per Figure 73
TJ Total Jitter Tolerance Measured at point D from SFF-8431	0.76			UIpp	Based on 1000BASE-SX/LX TP4 jitter at the SFP+ connector (as per IEEE 802.3 Clause 38.2.1) Jitter is measured with a 637 kHz high pass filter RJmin = 0.76 - measured DJ
DJ Deterministic jitter Tolerance Measured at point D from SFF-8431	0.48			UIpp	
RJ Random Jitter Tolerance Measured at point D from SFF-8431	RJmin			UIpp	

1. For the worst case output from a module, the ratio of peak-to-peak voltage to eye opening is expected to be less than a factor of 2x
2. SFP MSA specifies a minimum voltage of 370mVpp at the output of the module. The SFP+ MSA reference channel has up to 8.5dB of loss at 5.5GHz. The loss should scale linearly with rate from 5.5 GHz to 1.25/2 GHz to around 1dB loss.

Table 58: XAUI 1.25Gbps Serial Receiver Specifications

Applies to XAUI Lane0 Input (for all 1GbE applications including Backplane and SFP)

Description	Min	Typ	Max	Units	Conditions/Notes
Nominal bit rate		1.25			1 GE 8B/10B Encoded
Bit rate tolerance	-100		+100	ppm	Relative to nominal bit rate
Receiver Coupling		AC			
Peak to peak input voltage tolerance Measured at point D from INF-8077i			850	mVppd	See eye mask.
Eye Opening	330			mVppd	See eye mask.
X1,X2,Y1,Y2 Mask Values Measured at point D from INF-8077i			0.16	UI	X1 per Figure 73
			0.41	UI	X2 per Figure 73
	165			mV	Y1 per Figure 73
			425	mV	Y2 per Figure 73
TJ Total Jitter Tolerance Measured at point D from INF-8077i	0.32			UIpp	Jitter is measured with a 637 kHz high pass filter
DJ Deterministic jitter Tolerance Measured at point D from INF-8077i	0.20			UIpp	
RJ [1] Random jitter Tolerance Measured at point D from INF-8077i	0.12			UIpp	
Signal Acquire Time			200	ms	From application of input data

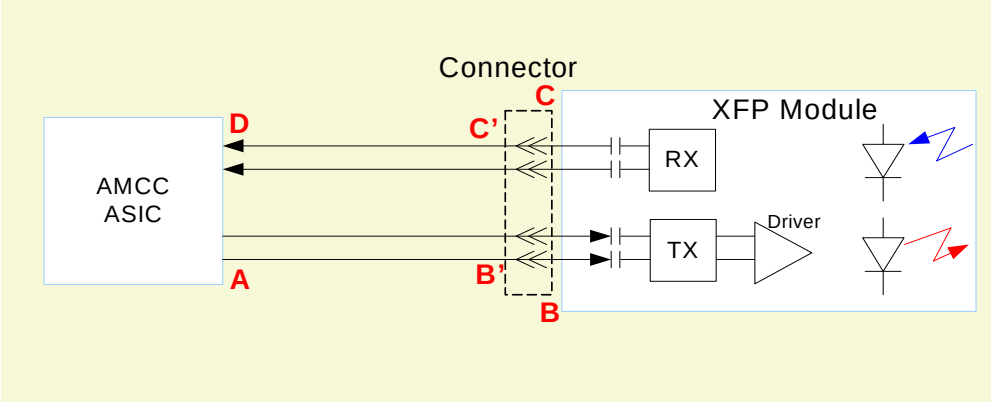
1. The Tx path (XFI input to SFI output) provides very little filtering of RJ applied to the XFI input, due to narrowband nature of the RJ. The Tx path also adds a small amount of RJ. To ensure that the RJ on the SFI output meets the TP1 requirement of 0.14 UIPP, it is necessary that the RJ on the XFI input be smaller than specified here.

Table 59: XFI 10Gbps Receiver Specification

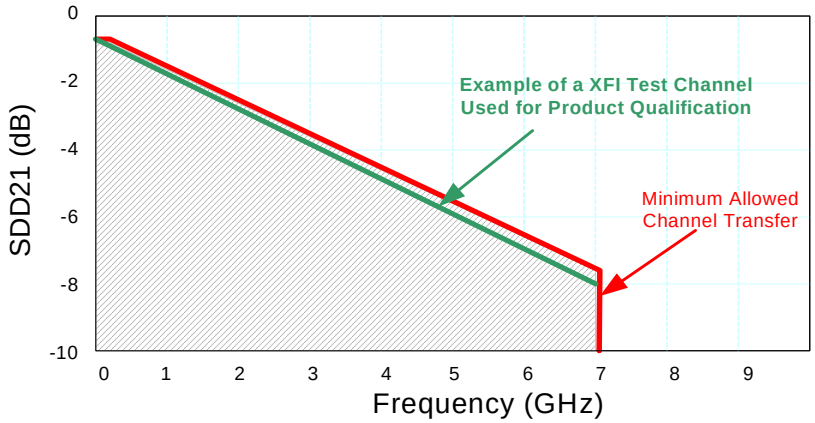
Description	Min	Typ	Max	Units	Conditions/Notes
X1,Y1,Y2 Mask Values Measured at point D from INF-8077i			0.325	UI	X1. Per Figure 77
	55			mVpp	Y1. Per Figure 77
			525[1]	mV	Y2. Per Figure 77
TJ [2 3] Total Jitter amplitude tolerance	0.65			UIpp	$TJ = TJ_{C'} + TJ_{XFI\_channel}$ Sinusoidal Jitter (SJ) is applied in addition to TJ.
Sinusoidal Jitter Tolerance	Fig. 79				

1. Out of 525mV, 100mV is allocated for multiple reflections.
2. Total Jitter Tolerance is measured with the worst-case electrical output from the XFP module at point C' (from Table 19 of INF-8077i) plus degradation due to the worst case XFI-compliant channel (from Figure 6 of INF-8077i). The jitter at point C' consists of 0.34UIpp of total jitter (TJ), of which 0.18UIpp is deterministic jitter (DJ). The degradation from the channel adds sufficient DDJ so that the total jitter (TJ) at the chip input (point D) equals or exceeds the minimum requirement. SJ is applied in addition to the TJ as per the template given in Figure 79. Measured with a PRBS31 unframed pattern for both LAN and WAN applications. See Fig. 76 for the channel definition.
3. Refer to AMCC Application Note (pending) for details on jitter tolerance measurement methodology.

Figure 76: XFP Application Reference Model



a) Application diagram showing the definitions of points C' and D that define the host compliance channel.



b) XFI host compliance channel loss, defined between points C' and D.

Figure 77: Receiver Compliance Mask

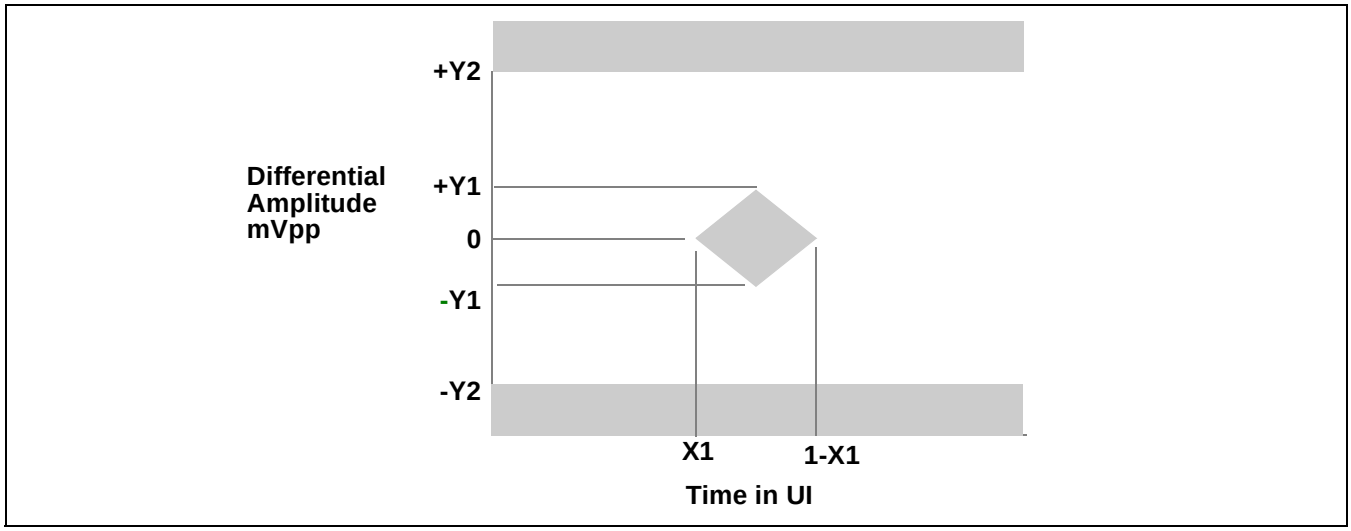


Figure 78: 10Gbps Receiver Sinusoidal Jitter Tolerance Mask for SFI Limiting Applications

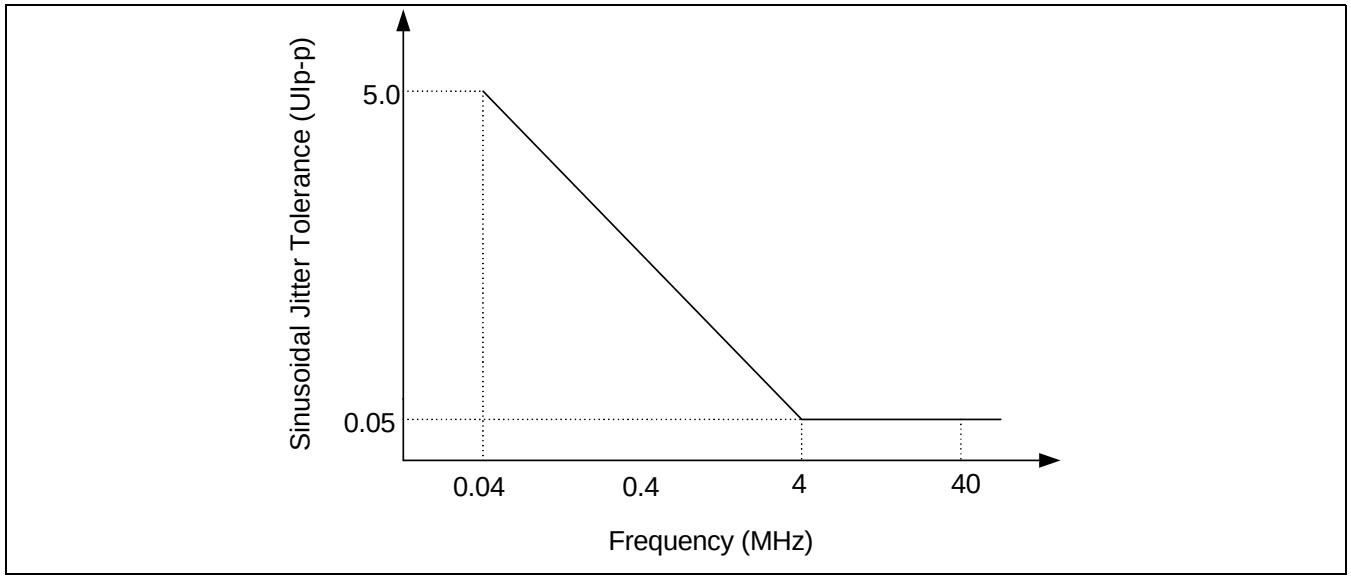


Figure 79: 10Gbps Receiver Sinusoidal Jitter Tolerance Mask for XFI Applications

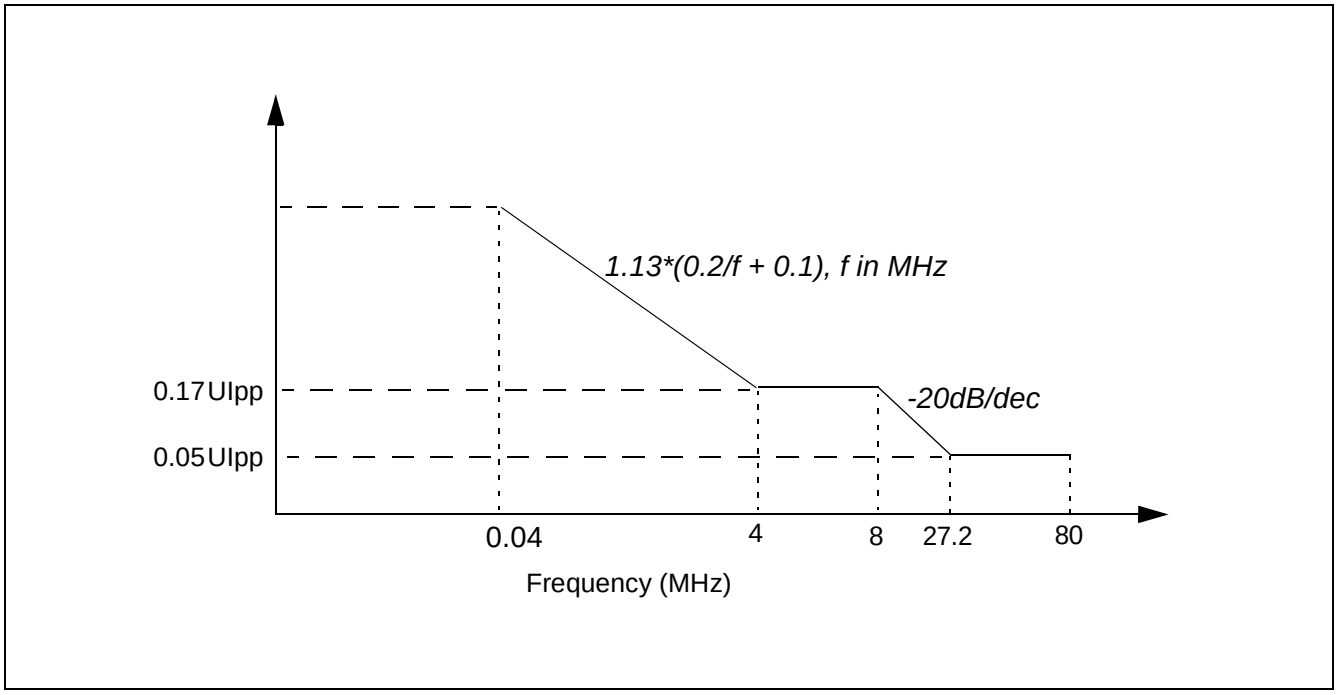
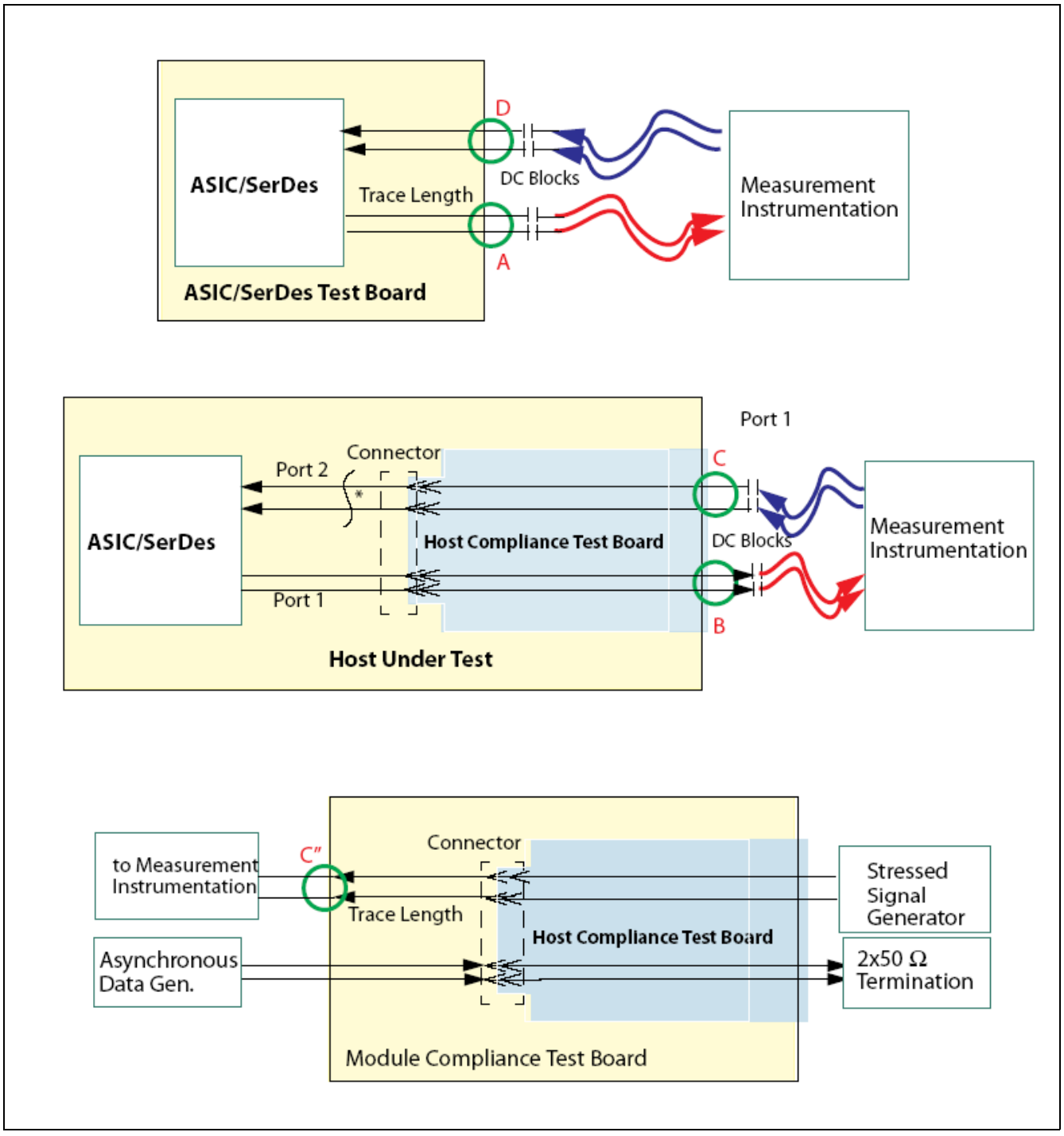


Figure 80: 10Gbps Transmitter & Receiver SFI Interface Test Points per SFF-8431 and INF-8077i [1]



1. Although AMCC has validated all SFI measurements mentioned in this document, system level factors pertaining to board design and layout may alter final SFI compliance results. Due to these factors, AMCC does not guarantee or imply system level SFI compliance in this specification. It is the responsibility of the end user to design and validate their system for SFI compliance.

Table 60: XAUI 3.125Gbps Driver Parallel Interface Specifications

Applies to XDRV0..3P/N Signals in 10GE Mode

Description	Min	Typ	Max	Units	Conditions/Notes
Bit Rate[1]	3.01	3.125	3.19	Gbps	
XAUI Output Near-end Mask [2 3]			0.175	UI	X1 per Figure 81
			0.390	UI	X2 per Figure 81
	365			mV	Y1 per Figure 81
			800	mV	Y2 per Figure 81
Output Amplitude Range	365		800	mVpp	Per Side. Output level set per lane by XAUI_AMP_0 to XAUI_AMP_3 fields (see Registers 4.C056 and 4.C057) Stepsize ~ 9mV
Output Rise and Fall Time	40		100	ps	20% to 80%
Output Impedance		100		Ω	Differential
Pre-emphasis Level	0		10	dB	Maximum pre-emphasis level with respect to output amplitude. Pre-emphasis level set by XAUI_DEEMP_0 to XAUI_DEEMP_3 fields (see Registers 4.C058 and 4.C059) Resolution ~ 9mV
Output Differential Skew			15	ps	measured from the eye crossings for P vs. N outputs
Differential Output Return Loss	10			dB	Referenced to 100Ω 50 MHz to 3.125 GHz
Output Total Jitter [2 4]			0.42	UIpp	
Output Deterministic Jitter [2 4]			0.27	UIpp	

1. Bit rate is specified relative to the reference clock frequency
2. Although this parameter does not meet the IEEE requirement for near-end mask, it does meet all far-end mask requirements when the driver settings are optimized. Note that IEEE Clause 47.3.3.5 specifies that, "The driver shall satisfy either the near-end eye template and jitter requirements, or the far-end eye template and jitter requirements."
3. Measurements of the XAUI output eye height, were performed using AMCC's standard process, voltage and temperature variations testing. The worst case measured eye height was 765mV differential. The new specification above for minimum XAUI eye height was chosen to allow additional margin.
4. AMCC has characterized the near-end XAUI output TJ and DJ using AMCC's standard process, voltage and temperature variation testing. The worst-case measured TJ was 0.341 UIpp, which meets the IEEE 802.3-2005 requirements. The worst case measured DJ was 0.211 UIpp. The new specification above for TJ and DJ was selected to allow additional margin.

Table 61: XAUI Input Parallel Interface Specifications

Applies to XCDR0..3P/N Signals in 10GE Mode

Description	Min	Typ	Max	Units	Conditions/Notes
Bit Rate[1]	3.01	3.125	3.19	Gbps	
Baud Rate tolerance	-100		+100	ppm	
Input Impedance		100		Ω	Differential
Input Amplitude Range	50		800	mVpp	Per side, referenced into an ideal 50Ω load. Standard equalization.
Differential Input Return Loss	10			dB	Referenced to 100Ω 50MHz to 2.5GHz
Common Mode Return Loss	6			dB	Referenced to 25Ω 50MHz to 2.5GHz
Input Differential Skew Tolerance	75			ps	at crossing point
Jitter Tolerance[2]	Fig. 82				Sinusoidal Jitter (SJ)
	0.37			UIpp	Deterministic Jitter (DJ)
	0.55			UIpp	Deterministic + Random Jitter (DJ + RJ)

1. Bit rate is specified relative to the reference clock frequency
2. The total jitter applied to the receiver is the sinusoidal jitter (applied according to the mask in Fig. 82) + DJ + RJ. Example: at 20MHz, TJ = (DJ+RJ) + SJ = 0.55UI + 0.1UI = 0.65UI.

Figure 81: XAUI Parallel Driver Near End Eye Mask

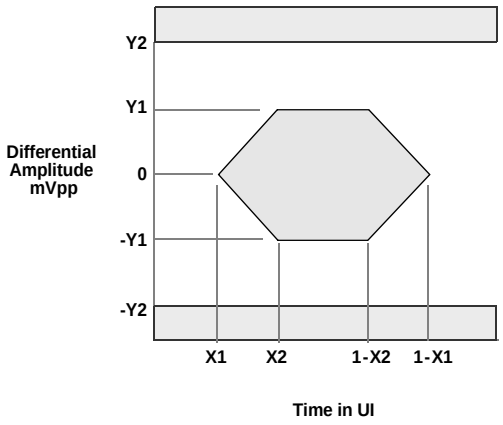


Figure 82: XAUI Receiver Sinusoidal Jitter Tolerance Mask

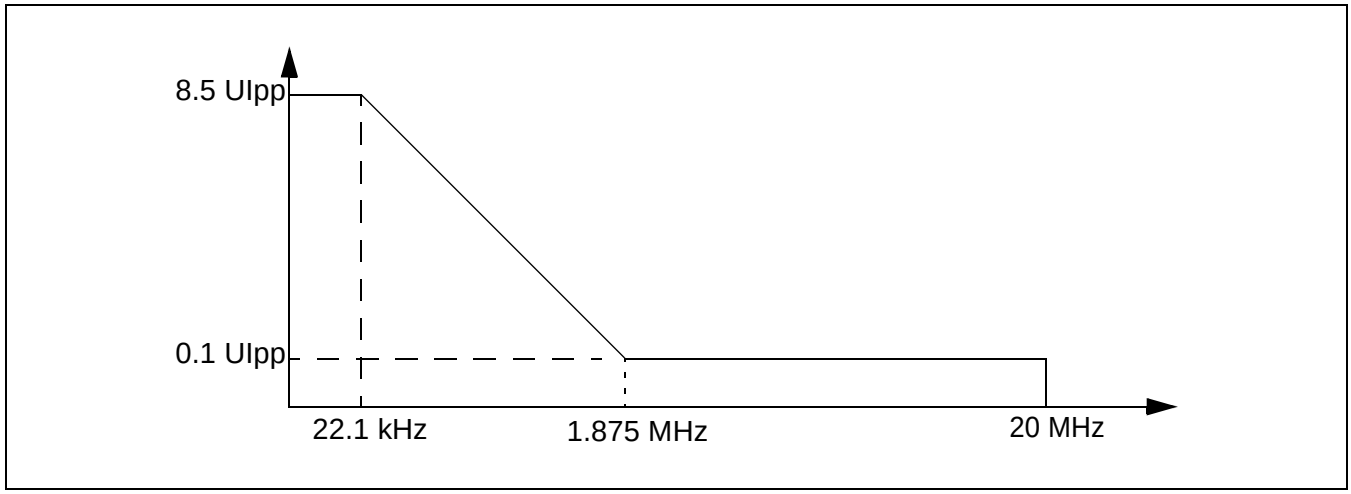


Table 62: VCXO Performance Specifications

Description	Min	Typ	Max	Units	Conditions/Notes
PFD Gain		400		mV/2π rad	
PFD Differential Output Swing		+-400		mVpp	
VCXO characteristics					Please see VCXOI input specifications in Table 64.
PFD differential R_{out}		2		kΩ	

Table 63: Latency Performance Specifications [1]

Description	Min	Typ	Max	Units	Notes
XGXS & XAUI Sublayer Round-Trip Time			400	ns	Includes 20” of FR4 in each direction (~7ns)
PCS Sublayer Round-Trip Time			160	ns	
WIS Sublayer Round-Trip Time			2500	ns	Default round-trip delay. Does not meet IEEE 802.3-2005 specification. Required for jumbo frame support (10kB).
			1350		Requires modification of default register values. Meets IEEE 802.3-2005 specification. Does not support jumbo frames.
Serial PMA & PMD Sublayer Round-trip Time			76	ns	Excludes optical fiber patch cord.
KR Training Time		400	500	ms	
Propagation Delay, 1GbE Mode (Rate Adaptation Mode)	65	100	135	ns	Tx path only Rate adaptation buffer size based on 200ppm clock frequency difference and two consecutive 9600 byte frames without excess intermediate IDLE ordered sets.
	65	100	135	ns	Rx path only Rate adaptation buffer size based on 200ppm clock frequency difference and two consecutive 9600 byte frames without excess intermediate IDLE ordered_sets.
	130	200	270	ns	Round trip
	163	249	337	bits	

1. All round-trip times in this table are based on simulation.

Table 64: CML Clock Input Performance Specifications: EREFCLKP/N, SREFCLKP/N, VCXOIP/N

Description	Min	Typ	Max	Units	Conditions
Input Frequencies		52.0833 [1]		MHz	Associated REFCLK 10GE application Div-by-198 and div-by-66
		156.25			
		53.1265		MHz	Associated REFCLK 10GFC application Div-by-198 and div-by-66
		159.38			
		51.84 [2]		MHz	Associated REFCLK WIS application Div-by-64 and div-by-192
		155.52			
Clock Input Impedance	40	50	60	Ω	Single-Ended internal on-chip termination
	80	100	120	Ω	Differential internal on-chip termination
Clock Input Amplitude Tolerance	400		1600	mVppd	Externally AC coupled. Measured differentially.
Input Duty Cycle Tolerance	40		60	%	
Input Rise/Fall Time Requirement	200		1250	ps	20-80%
Input Frequency Tolerance [3]	-100		+100	ppm	

1. Exact frequency is calculated by the equation 10.3125GHz / 198.
2. Cannot meet SONET jitter generation requirements with this clock frequency.
3. The device will work properly in WAN mode with +-100ppm frequency tolerance, however, SONET compatible applications require a +-20ppm tolerance.

Table 65: CML Clock Output Performance Specifications: FPLLOUT and XPLLOUT

Description	Min	Typ	Max	Units	Conditions/Notes
Output Frequencies		156.25		MHz	Associated REFCLK 10GE application div-by-66
		125		MHz	Synchronous Ethernet Clock 10GE application Div-by-82.5 [XPLLOUT only]
		159.38		MHz	Associated REFCLK 10GFC application div-by-66
		155.52		MHz	Associated REFCLK WIS applications only Div-by-64
		312.5		MHz	MAC Clock [XPLLOUT only]
Output Impedance	40	50	60	Ω	Single-Ended internal on-chip termination
	80	100	120	Ω	Differential internal on-chip termination
Output Amplitude (Swing)	640		1200	mVppd	Externally AC coupled. Measured differentially.
Output Duty Cycle		60/40		%	Synchronous Ethernet Clock (125MHz) MAC Clock (312.5MHz)
	40	50	60	%	Other clocks
Output Rise/Fall Times	200		1250	ps	20-80%, FPLLOUT
	160		1250		20-80%, XPLLOUT
BAUD rate variation	-100		+100	ppm	tracks reference clock tolerance.
Random Jitter		150		ps pp	Synchronous Ethernet Clock (125MHz) MAC Clock (312.5MHz)
			10	ps rms	Other clocks. Jitter in bandpass up to 100MHz

Table 66: Reference Clock Jitter Specifications (EREFCLK and SREFCLK)

Description	Min	Typ	Max	Units	Conditions/Notes
Line Rate Div-by-66 and Div-by-64 Reference Clock Covers SFP+, Ethernet, and XFP applications, except XFP applications required to meet Telecom Jitter Generation (see below)					
Random Jitter			0.73	ps rms	Jitter and Spurious Noise are measured after applying the following filters: 4MHz 1st order high-pass filter 3.6MHz 1st order low-pass filter
Spurious Noise			-75	dBc [1]	
Line Rate Div-by-198 Reference Clock Covers SFP+, Ethernet, and XFP applications, except XFP applications required to meet Telecom Jitter Generation (see below)					
Random Jitter			0.64	ps rms	Jitter and Spurious Noise are measured after applying the following filters: 4MHz 1st order high-pass filter 2.2MHz 1st order low-pass filter
Spurious Noise			-75	dBc [1]	
XFP applications required to meet Telecom Jitter Generation specification in XFP standard [2] Line Rate Div-by-64 SREFCLK					
Random Jitter			0.35	ps rms	Jitter and Spurious Noise are measured after applying the following filters: 50kHz 1st order high-pass filter 3.6MHz 1st order low-pass filter
Spurious Noise			-75	dBc [1]	

1. dBc is decibels referenced to the spectral energy at the carrier frequency e.g. 156.25MHz or 155.52MHz.
2. The WAN clock jitter specifications must be met in order to satisfy the XFP specification for telecom jitter generation applications (INF-8077i). This requirement is listed in the Datasheet in Table 46.

Electrical Specifications

Table 67: Absolute Maximum Ratings

The following are the absolute maximum stress ratings for the QT2025 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only, and operation of the device at the maximums stated, or any other conditions beyond those indicated in the “Recommended Operating Conditions” of the document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Description	Min	Typ	Max	Units	Conditions
Storage Temperature	-40		150	°C	
Supply Voltage Limits	-0.6		1.5	V	1.2V Supplies FRXV1P2/A, FTXV1P2/A, XV1P2/A, COREVDD
	-0.6		2.1	V	1.8V Supplies FRXV1P8, FTXVTERM
Voltage on any CML input pin	-0.6		1.85	V	Applies to the following pins only: EREFCLKP, EREFCLKN, SREFCLKP, SREFCLKN, VCXOIP, VCXOIN
			1.5		All other CML pins
Voltage on any LVCMOS pin	-0.6		3.6	V	
Electrostatic Discharge (ESD) Exposure[1]: Human Body Model			2000	V	All pins pass except those listed below
			1000	V	FRXIP, FRXIN FRXV1P8 (all pins associated with this power supply)
			1C		Device JESD22-A114B Class Rating

1. The QT2225 is rated to the listed ESD voltages based upon JEDEC standard JESD22-A114-B. Adherence to standards for ESD protection should be taken during the handling of the devices to ensure that the devices are not damaged. The standards to be used are defined in ANSI standard ANSI/ESD S20.20-1999, “Protection of Electrical and Electronic Parts, Assemblies, and Equipment.” Contact your local FAE or sales representative for applicable ESD application notes.

Table 68: Recommended Operating Conditions

The device will operate at a junction temperature of 125°C but part lifetime and reliability may be reduced. It is recommended that prudent thermal management techniques are used to maximize device lifetime.

Description	Min	Typ	Max	Units	Conditions
Operating Temperature Limits *Applies to 10GBASE-SR, 10GBASE-LR, 10GBASE-KR and 1000BASE-X operation*	0		80	°C	Ambient
			100	°C	Case
			110	°C	Junction
Operating Temperature Limits *Applies to 10GBASE-LRM and Passive Direct Attach Copper Cable operation*	0		70	°C	Ambient
			90	°C	Case
			100	°C	Junction
Operating Supply Voltage Limits	1.14	1.2	1.26	V	1.2V Supplies FRXV1P2/A, FTXV1P2/A, XV1P2/A, COREVDD
	1.71	1.8	1.89	V	1.8V Supplies FRXV1P8, FTXVTERM
SFP+ Applications: Total Power Consumption (10GBASE-LRM, -SR and -LR)		1.53	1.67	W	Typical Condition: 10GBASE-SR/LR Fast process, nominal voltage, 100C junction, low drive levels
		1.55	1.70	W	Typical Condition: 10GBASE-LRM Fast process, nominal voltage, 100C junction, low drive levels
		1.67	1.900	W	Worst Case Condition: High voltage, high temp, uc_clk_sel=1 XAUI outputs = 960 mVpp differential Fiber output = 450 mVpp differential No monitor outputs or loopbacks enabled
SFP+ Applications: Worst Case Operating Currents (10GBASE-LRM, -SR and -LR)		0.170	0.202	A	FRXV1P2
		0.215	0.272	A	FTXV1P2
		0.016	0.023	A	FRXV1P2A
		0.016	0.020	A	FTXV1P2A
		0.279	0.308	A	XV1P2
		0.016	0.024	A	XV1P2A
		0.202	0.236	A	FRXV1P8
		0.017	0.030	A	FTXVTERM
		0.302	0.368	A	COREVDD
Backplane Application: Worst Case Total Power Consumption (10GBASE-KR)		1.592	1.883	W	Worst Case Condition: High voltage, high temp, uc_clk_sel=3 XAUI outputs = 960 mVpp differential Fiber output = 1150 mVpp differential No monitor outputs or loopbacks enabled

Table 68: Recommended Operating Conditions

The device will operate at a junction temperature of 125℃ but part lifetime and reliability may be re duced. It is recommended that prudent thermal management techniques are used to maximize device lifetime.

Description	Min	Typ	Max	Units	Conditions
Backplane Application: Worst Case Operating Currents (10GBASE-KR)		0.187	0.211	A	FRXV1P2
		0.212	0.277	A	FTXV1P2
		0.020	0.023	A	FRXV1P2A
		0.014	0.020	A	FTXV1P2A
		0.265	0.312	A	XV1P2
		0.016	0.024	A	XV1P2A
		0.209	0.244	A	FRXV1P8
		0.026	0.035	A	FTXVTERM
		0.263	0.340	A	COREVDD
Additional Power Consumption Numbers		0.07		W	WIS Block Power Consumption Additional power consumed when WIS block is enabled. Extra current draw is on COREVDD supply.
		0.03		W	FEC Block Power Consumption Additional power consumed when FEC block is enabled. Extra current draw is on COREVDD supply.
		1.0		W	**1GE Application:** Total Power Consumption
Power Supply Noise Tolerance[1] [2]			0.3	mVrms	FRXV1P2A Integrated value over all frequencies: 75kHz < f < 4MHz
			0.22	mVrms	FTXV1P2A Integrated value over all frequencies: f < 2.45MHz f > 4MHz
			0.7	mVrms	XV1P2A Integrated value overall frequencies:[3] f < 10.8MHz f > 1.0MHz f > 1.875MHz
			60	mVpp	Remaining 1.2V Supplies: FRXV1P2, FTXV1P2, COREVDD, XV1P2
			90	mVpp	Remaining 1.8V Supplies: FRXV1P8, FTXVTERM

1. Frequencies represent 3dB roll-off frequency for a single-pole filter with 20dB/decade roll-off. Value is what may be tolerated at device input.
2. Noise tolerance recommendations based on simulation only.
3. The LPF corner frequency is higher than the HPF corner frequencies. Because these represent 3dB roll-off frequencies, the resultant filter function does provide some filtering. The noise tolerance is specified with two High Pass Filters.

Table 69: LVCMOS Input/Output Characteristics

Description	Min	Typ	Max	Units	Conditions
LVCMOS Input Specifications					
Input High Voltage Level	0.84			V	3.3V tolerant
Input Low Voltage Level			0.40	V	
Input Rpullup/Rpulldown Resistance	30	50	95	kΩ	
Hysteresis	100			mV	
LVCMOS Output Specifications					
Output High Voltage	Vpu-0.1			V	Ioh = -100µA
Output Low Voltage			0.2	V	Iol = 4mA
Ioff Open-drain output off-state leakage			2.5	µA	Measured at 2.5V
Output Low Current	4			mA	Vol = 0.2V, all pins (except LEDx)
	10			mA	Vol = 0.2V, LED1, LED2, LED3 only
LVCMOS General Specifications					
Input / Output Capacitance		3.5	5	pF	Vio(dc) = 0.6V
Hysteresis	100			mV	

Table 70: MDIO Input/Output Characteristics: MDC, MDIO

Description	Min	Typ	Max	Units	Conditions/Notes
MDIO Input Characteristics					
Input High Voltage Level	0.84			V	
Input Low Voltage Level			0.36	V	
Input Capacitance			5	pF	
MDIO Output Characteristics					
Output High Voltage	1			V	Ioh = -100µA
Output Low Voltage			0.2	V	Iol = 5.5 mA
Bus Capacitance			470	pF	2.5MHz bus speed
			100	pF	25MHz bus speed, max 1.2V pullup
MDIO General Characteristics					
Pullup Resistance	180			Ω	1.2V pullup
	600			Ω	3.3V pullup (open drain mode)

Table 71: MDIO Interface Timing: MDC, MDIO

Description	Min	Typ	Max	Units	Conditions
MDIO Data Input Hold Time			10	ns	wrt MDC rising edge
MDIO Data Input Setup Time			10	ns	wrt MDC rising edge
Operation Under High Capacitive Load (open drain configuration)					
Delay from MDC Rising Edge to MDIO Data Output Edge	0		300	ns	Cload=470pF, Rpu = 400 Ω (Rpu for open drain mode only) Delay is measured from MDC rising edge Vih_min level (0.84V) to MDIO rising edge Vih_min level (0.84V) or MDIO falling edge Vil_max level (0.36V)
MDC Clock Rate			2.5	MHz	Cload=470pF, Rpu = 400 Ω (Rpu for open drain mode only)
MDC High and Low Times	160			ns	Cload=470pF, Rpu = 400 Ω (Rpu for open drain mode only)
Operation Under Low Capacitive Load (open drain configuration)					
Delay from MDC Rising Edge to MDIO Data Output Edge	0		32	ns	Cload=100pF, Rpu = 180 Ω (Rpu for open drain mode only)
MDC Clock Rate [1]			25.0	MHz	Cload=100pF, Rpu = 180 Ω (Rpu for open drain mode only)
MDC High and Low Times	20			ns	Cload=100pF, Rpu = 180 Ω (Rpu for open drain mode only)
Operation Under Low Capacitive Load (push-pull configuration)					
Delay from MDC rising edge to MDIO data output edge	0		32	ns	Cload=100pF, Vterm = 1.14V min
MDC Clock Rate			25.0	MHz	Cload=100pF, Vterm = 1.14V min
MDC high and low times	20			ns	Cload=100pF, Vterm = 1.14V min

1. The maximum bus rate may be limited by the microcontroller clock rate. See “MDIO Bus Speed” on page 86. for details.

Table 72: DCC Interface Timing: RDCC, RDCC_CLK, TDCC, TDCC_CLK

Description	Min	Typ	Max	Units	Conditions
Output Clock Frequency		1.944		MHz	
RDCC Output Data Delay wrt RDCC_CLK Falling Edge			0.1	µs	For an output rising edge, the delay is measured to a crossing level of 0.7*Vpullup. For an output falling edge, the delay is measured to a crossing level of 0.3*Vpullup

Table 72: DCC Interface Timing: RDCC, RDCC_CLK, TDCC, TDCC_CLK

Description	Min	Typ	Max	Units	Conditions
TDCC Input Data Setup Time wrt TDCC_CLK Falling Edge	0.1			µs	Input timing is measured from the point where input signals cross a voltage level equal to COREVDD/2
TDCC Input Data Hold Time wrt TDCC_CLK Falling Edge	0.1			µs	Input timing is measured from the point where input signals cross a voltage level equal to COREVDD/2

Table 73: I2C Input/Output Characteristics: EEPROM_SCL/SDA, UC_SCL/SDA

Description	Min	Typ	Max	Units	Conditions
I2C Input Specifications					
Input High Voltage Level	0.84			V	
Input Low Voltage Level			0.4	V	
Input Capacitance			5	pF	
I2C Output Specifications					
Output High Voltage			Vpu	V	3.3V tolerant Vpu = external resistor termination voltage. Range 1.2-3.3 volts
Output Low Voltage			0.2	V	sinking 5.5mA
External Load Capacitance			400	pF	applies to SDA and SCL
External Pullup Resistance to Vpu	0.600	0.750	22	kΩ	750Ω required with maximum Cload to 3.3V

Table 74: I2C Interface Timing: EEPROM_SCL/SDA, UC_SCL/SDA

Description	Min	Typ	Max	Units	Conditions
Standard Mode					
SCL clock frequency			100	kHz	
SCL low time	4.7			µs	
SCL high time	4			µs	
SDA and SCL rise time			1000	ns	
SDA and SCL fall time			300	ns	
SDA output delay wrt SCL	0			µs	
SDA setup time wrt SCL	250			ns	
SDA hold time wrt SCL	4			µs	
Fast Mode					
SCL clock frequency			400	kHz	
SCL low time	1.3			µs	
SCL high time	0.6			µs	
SDA and SCL rise and fall time			300	ns	
SDA output delay wrt SCL	0			µs	
SDA setup time wrt SCL	100			ns	
SDA hold time wrt SCL	0.6			µs	

Table 75: JTAG Interface Timing: TDI, TDO, TCK, TMS

Description	Min	Typ	Max	Units	Conditions/Notes
TCK operating frequency			10	MHz	
TDI, TMS input setup time requirement			10	ns	wrt TCK rising edge
TDI, TMS input hold time requirement			10	ns	wrt TCK rising edge
TDO output propagation delay[1] [2]			30	ns	[1] [2]Rpu = 250Ω, Vpu=1.2V or Rpu = 750Ω, Vpu= 3.3V, Cload = 50pF.

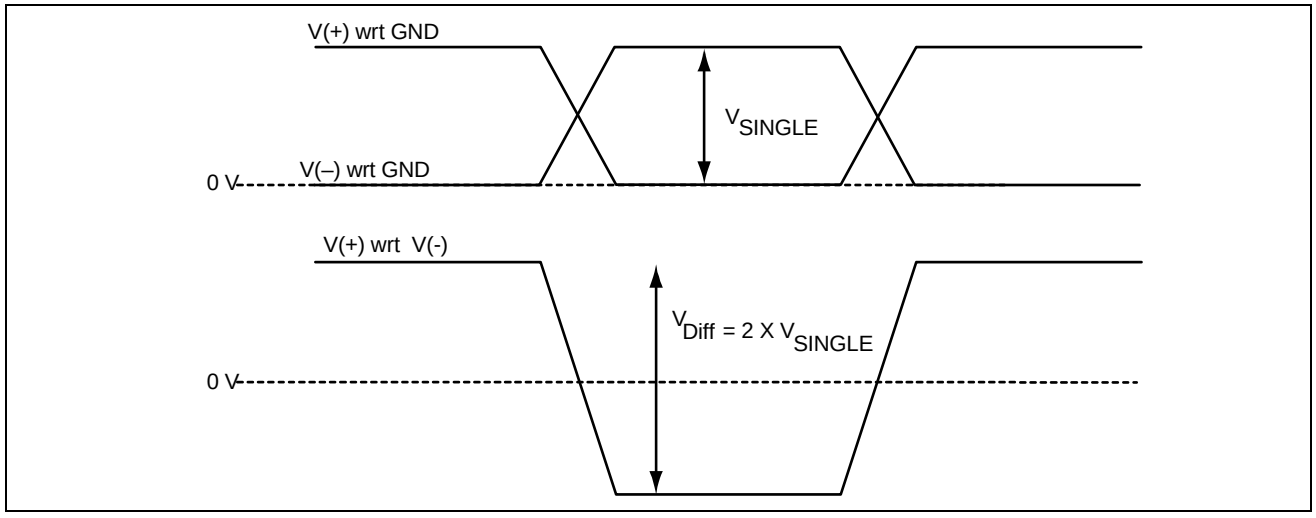
1. Timing is measured from the point where signals cross a voltage level equal to COREVDD/2
2. For a rising TDO output, the delay is measured to a crossing level of 0.7*Vpu. For a falling TDO output, the delay is measured to a crossing level of 0.3*Vpu. TDO is generated on the falling edge of TCK. TDI is clocked in on the rising edge of TCK. Therefore TDO propagation delay must not exceed half a TCK period minus the TDI setup time requirement.

Note: It is assumed that XAUI inputs are always AC coupled with 10nF, permitting implementation of IEEE1149.6 section 6.2.3.1 Rule a, Method 2.

Table 76: Auto-Negotiation DME Page Specifications

Description	Min	Typ	Max	Units	Conditions/Notes
Transmit Differential Peak-Peak Output Voltage	300		1200	mV	
Receive Differential Peak-Peak Input Voltage	200		1200	mV	
Transition position spacing (period)	3.2 -0.01%	3.2	3.2 +0.01%	ns	
Clock transition to Clock transition	6.2	6.4	6.6	ns	
Clock transition to data transition (date = 1)	3.0	3.2	3.4	ns	
Transitions in a DME page	51	-	100	-	guaranteed by differential Manchester encoding
DME page width	338.8	339.2	339.6	ns	
DME Manchester violation (MV) delimiter width	12.6	12.8	13.0	ns	

Figure 83: Differential Voltage Measurement

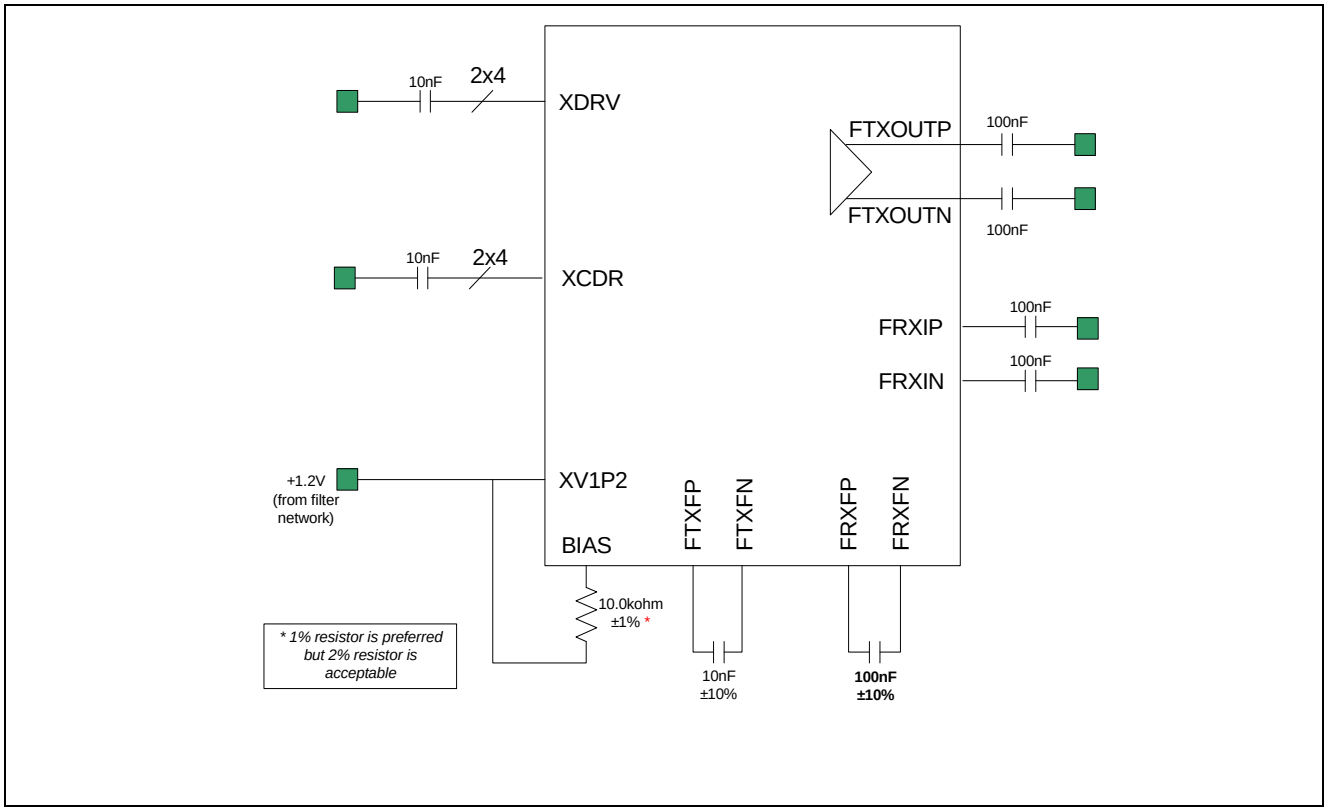


Note: WRT = With Respect To

RECOMMENDED TERMINATIONS AND EXTERNAL COMPONENTS

Figure 84 illustrates external components required to bias or terminate signal pins for proper operation of the QT2025.

Figure 84: External Loop, AC Coupling, and Bias Component Values



SFP+ Layout Recommendations

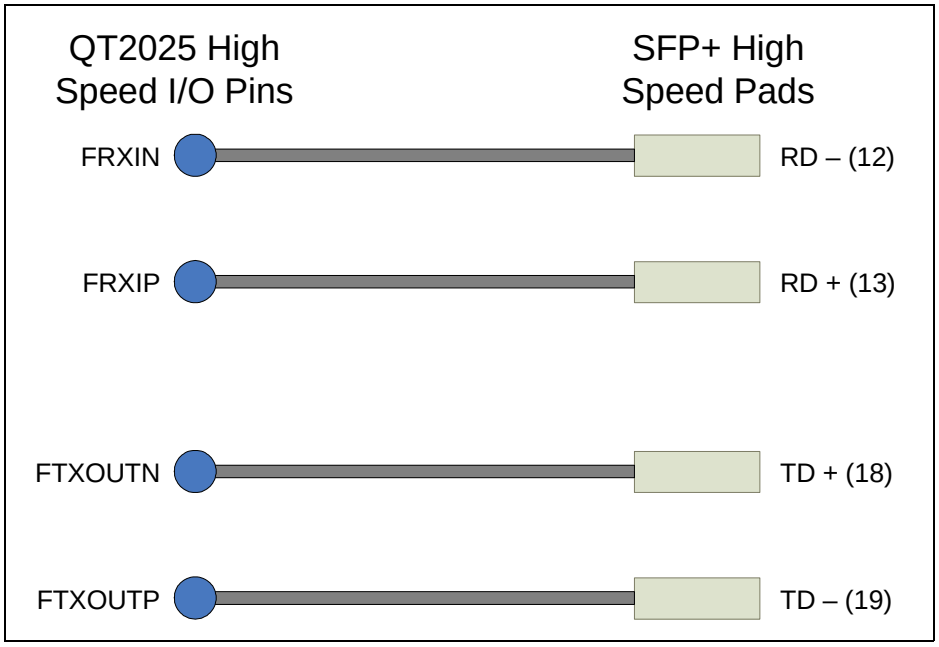
The firmware provided with the PHY assumes the FTXOUTP signal connects to TD- and FTXOUTN connects to TD+ of the SFP+ host PCB pad, as shown in Figure 85. This is done to avoid crossing the traces in the board layout, which optimizes signal integrity. Thus the SFP+ firmware inverts the polarity of FTXOUT by default to correct for this layout inversion.

If the layout is not inverted, the polarity may be flipped by writing to the TXOUT_SEL register field (1.C301 bit 7) after the PHY is initialized.

Designs using SFP+ modules that do *not* have a host controller to access this register field must follow the layout recommendation indicated here.

Figure 85 only specifies the connectivity. It does not provide information about layout dimensions for transmission line design.

Figure 85: SFP+ High Speed Layout Recommendation



Power Supply Sequencing

The chip is biased by a 1.2V supply voltage and a 1.8V supply voltage. There is no required timing relationship for the voltage turn-on between the two voltages for the chip.

The chip supply is broken up into several logical 1.2V supply inputs and 1.8V supply inputs. All of the 1.2V supply inputs must have voltage applied to them at the same time. Similarly, all of the 1.8V supply inputs must have voltage applied to them at the same time.

An external 3.3V voltage is often used to bias external components and pullups. As above, there is no required timing relationship.

Chip Reset Timing

There are two reset inputs to the PHY with specific reset timing requirements on startup.

TRST_N

The TAP circuitry must receive a reset after the power supplies are stable in order to place these circuits in a known state for normal traffic pass. This is done by holding the TRST_N signal low for a minimum of 500µs to reset the TAP circuit. Alternatively, the TRST_N signal can be permanently grounded during normal.

Failure to reset the TAP circuit can result in unpredictable operation including corrupted traffic, so it is important to initialize this circuit properly.

RESETN

The RESETN signal is the main reset signal for the datapath circuitry in the PHY. This must receive a reset after the power supplies are stable and the TRST_N signal has been reset. The RESETN signal must be held low for a minimum of 500µs to reset the datapath circuitry. The RESETN signal may be low or high before the reset is applied. It must be held high afterwards.

The PHY is ready to be programmed after the RESETN reset is complete.

LAN Reference Clock

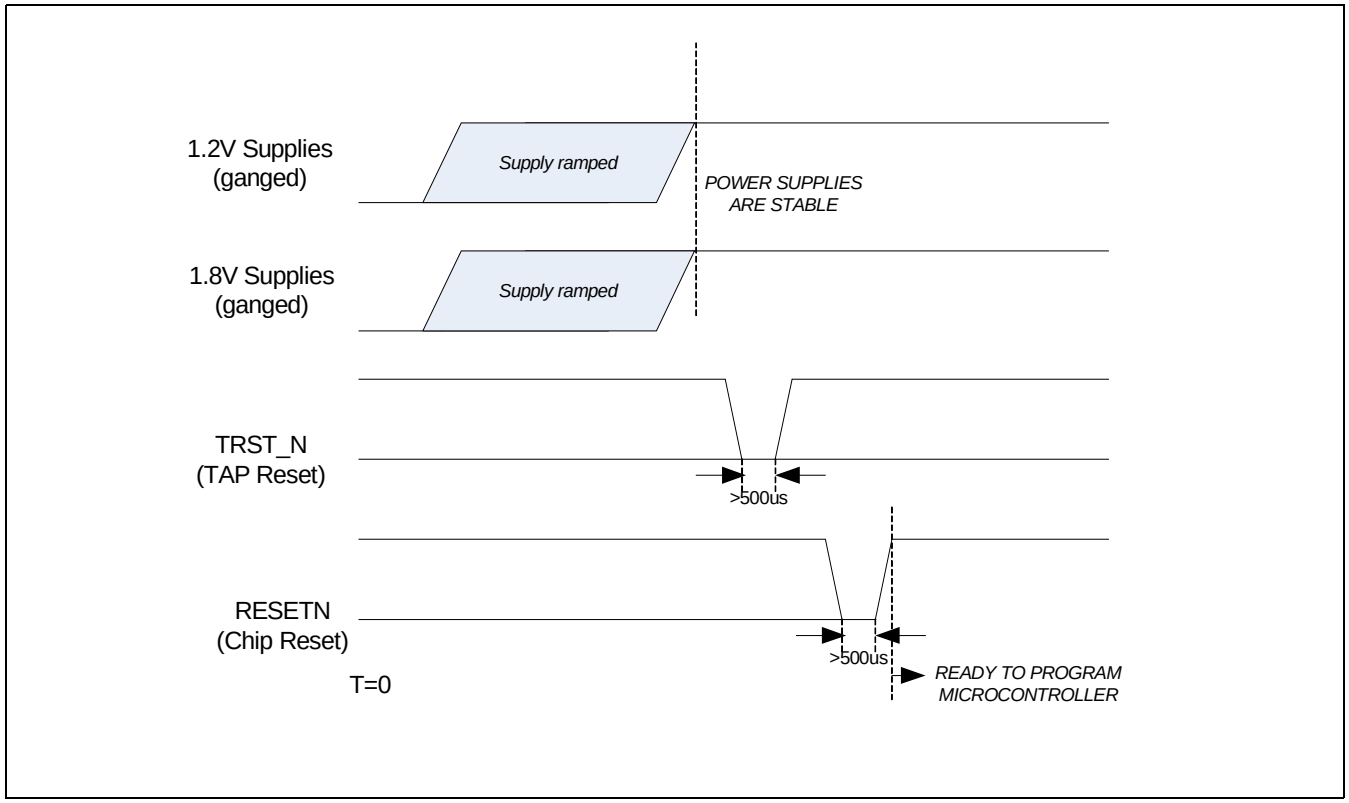
A valid 156.25MHz Ethernet reference clock is required to initialize the MDIO bus. Ensure that this clock is running and stable before the hard reset to RESETN is completed. This clock is applied to the EREFCLK input.

Managing Multi-Port Designs

On boards with more than one port, stagger the turn-on time of each port to avoid voltage droop and ground bounce issues induced by in-rush current effects. This means staggering the rising edge of the RESETN reset pulse for each port, where possible.

The timing of the firmware boot sequence should also be staggered for the same reason.

Figure 86: Power Supply Sequencing Requirements



Recommended Landing Pattern and Reflow

PCB Layout Recommendations

A recommended NSMD (No Solder Mask Defined) pad structure is given in Figure 87. The structure and values are recommendations only, and will vary with manufacturing process.

Baking instructions

To remove moisture, bake at 125℃ for 24 hours usi ng an oven with nitrogen purge per IPC / JEDEC J-STD-033. Baking removes the remote chance of popcorn effects during the reflow process.

Thermal Reflow Profile

The recommended reflow profile for the QT2025 is shown in Figure 88. Peak temperatures are shown for both the leaded and RoHS compliant versions of the products. The lead-free RoHS compliant version has a peak temperature of 260℃. The standard leaded version has a peak temperature of 225℃.

Figure 87: Recommended PCB layout for BGA landing pad for 13x13 mm^2 package.

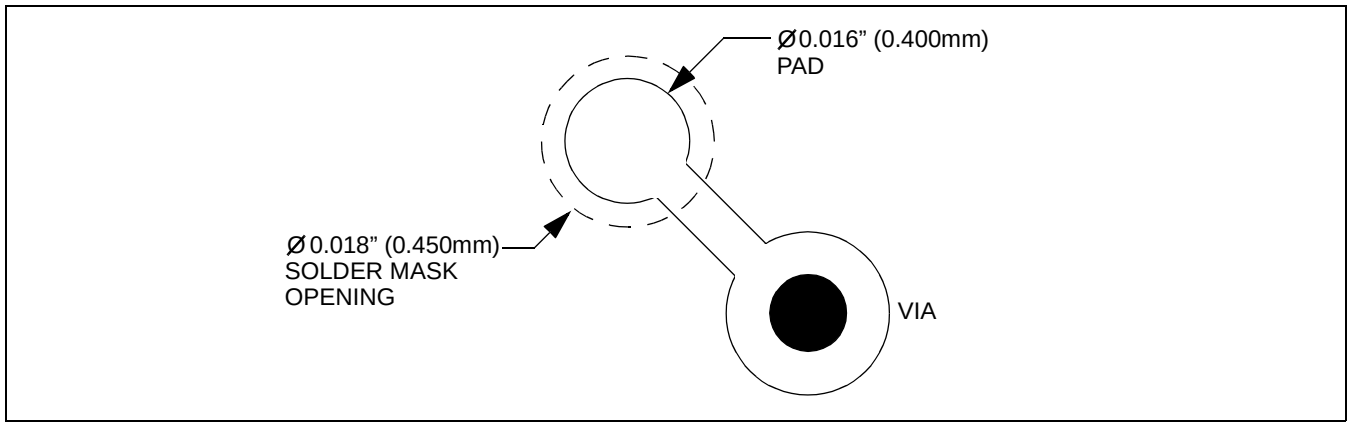
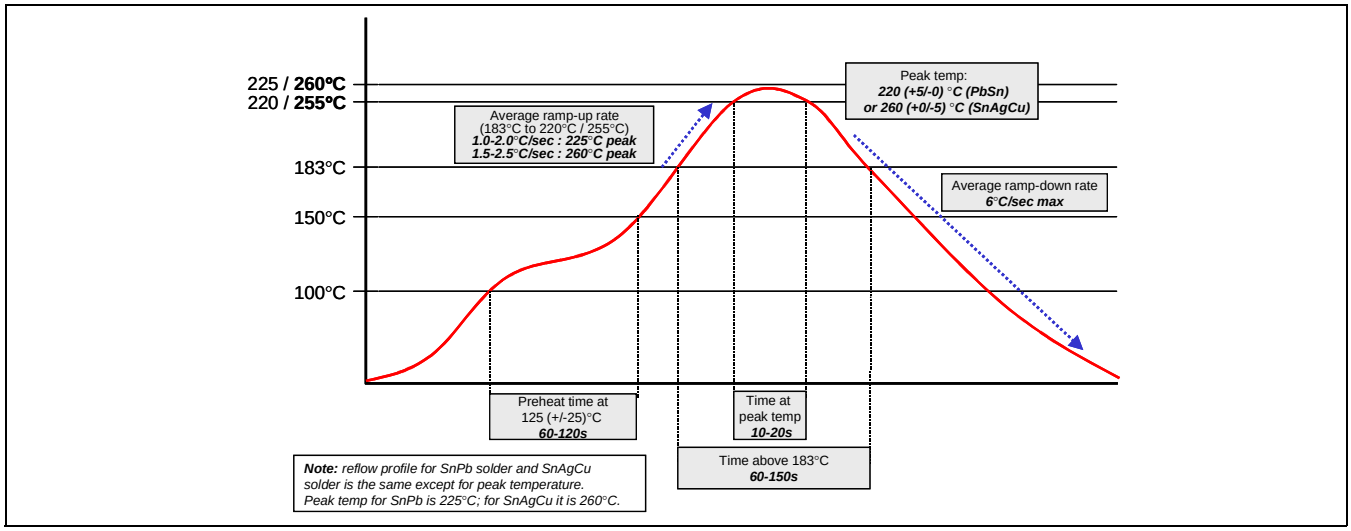


Figure 88: Recommended Reflow Profile



Revision History

Revision	Date	Description
4.00 to 5.00	March 13, 2009	Updated the following: • removed support for 51.84MHz WAN and 52.083MHz LAN reference clocks • removed support for 1GE rate • removed passive direct-attach cable support • removed all LRM specifications from Datasheet • corrected footnote in Table 16 "FPLLOUT Configuration Settings" • removed Driver Control Step Size parameter from Table 35 (parameter is already covered in Table 33). • clarified ESD tolerance by pin in Table 45 • corrected PMA System Loopback FTXOUT default pattern in Table 31 • Removed XFI Telecom Sinusoidal Jitter Tolerance Mask in Fig. 80 because it does not apply • Reduced XAUI Driver inner eye mask opening specification in Table 39. • Increased XAUI Driver DJ and TJ specifications in Table 39. • Updated current and power consumption specifications to reflect measured product distribution in Table 46 • Updated XFI serial driver SDD22 and SCC22 parameters in Table 35 "XFI 10Gbps Serial Transmitter Specifications" • Updated XFI serial receiver SCC11 parameter in Table 38 "XFI 10Gbps Receiver Specification" • Modified FPLLOUT and XPLLOUT driver swing specification in Table 43 on page 99 • Added chapter on LASI alarm interrupt • Added better description of XGXS Analog System Loopback in “System Loopbacks” on page 65. • Updated package thermal parameters in Table 32 "Thermal Management" • Added Section , “Power Supply Sequencing,” on page 110 • Updated description in “Receive Loss-of-Signal Pin (LOSOUTB)” on page 70 • Added section “SFP+ Layout Recommendations” on page 169 • Updated Reference Clock jitter requirements in Table 66 on page 157 • Modified Table 17, “TXENABLE Logic,” on page 71
3.11	September 3, 2008	Updated Power Numbers - Typical Power Configuration added to Table 68 on page 159
3.10	May 14, 2008	- changed order code to product Revision D - removed support for Through-timing Mode on Rx path at 1GE rate - removed LinQStat support - corrected product order code to -1 version for passive direct attach cable support - updated Table 32 - removed low speed clock output specifications from Table 64. Deleted VCXOCTL from table because it does not apply. - corrected footnote in Table 16 - corrected 16-bit error counter location in WAN mode in Table 35
3.01	February 22, 2008	Minor Label Changes and Formatting

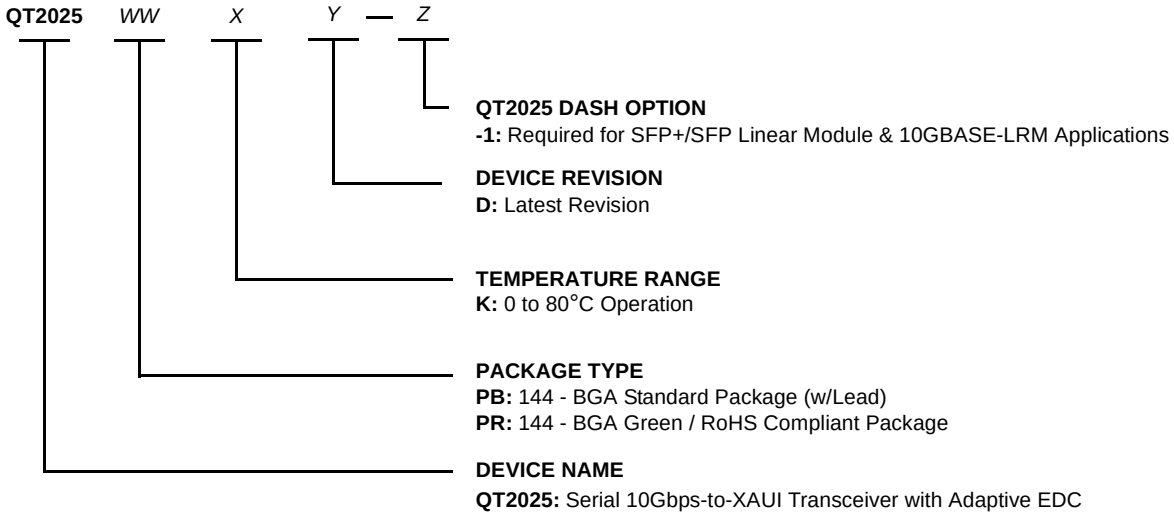
Revision History

Revision	Date	Description
3.00	February 21, 2008	Updated with New Part Numbers and Ordering Information along with the following: - Made a few Labeling and Format Corrections - Updated XPLLOUT & FPLLOUT Config Truth Tables - Updated the DOM Register Space - Updated Laser Fault Control Pin Status Location - Updated LS_ALARM Status Register Locations - Updated LED1/2 Default Settings (RX or TX assignments) - Updated Description & Location of the XFP/SFP+ Module Access through MDIO - Removed Firmware Configuration Table & Directed User to Firmware Documentation - Updated Timed BER Test Error Counter Locations - Added Serial PMA & PMD Sublayer Latency Spec - Added CML Max Amplitude Spec - Updated Power Numbers and Power Supply Noise Tolerance
2.00	November 30, 2007	Reformatted Document Layout. Electrical specs updated and additional information added related to firmware: - Added XV1P2A power supply definition. - Corrected BSDL pin list order for #19-22. - Updated FRXFN/P loop filter value to 100nF (required to support 1GE mode) - Update Timed BER Test Paragraph - Updated BER Test Procedure - Updated Ordering Information for Device Revisions B & C
0.70	May 2007	Generated ‘B’ version of Datasheet: - added 1GbE mode - added FEC encoding Corrected text to indicate XAUI Analog Loopback uses XDRV2 on Section 16.1 on page 112; updated Figure 55 on page 113. Added PRBS9 pattern generator description in Section 16.3.4 on page 116. Added 64-bit pattern generator description in Section 16.3.9 on page 119.
0.61	April 2007	- Added order codes for leaded parts - Corrected description of LOSOUTB in Section on page 53. - Corrected description of TXON in Section on page 54
0.6	November 2006	More information added to all sections
0.5	June 2006	General updates to all sections, final pinout added, register map added
0.4	November 2005	First customer revision

Ordering Information

To order QT2025 product, quote the order number listed in the table below.

Product Description	Product Name	Device Version	Ordering Number
QT2025: 10GBASE-KR & 1000BASE-KX Backplane Applications SFP+/SFP Limiting Module and Passive Direct Attach Cable Applications XFP Module Applications			
RoHS Compliant Package	QT2025	D	QT2025PRKD
Standard Package (w/Lead)	QT2025	D	QT2025PBKD
QT2025-1: SFP+/SFP Linear and Limiting Module and Passive Direct Attach Cable Applications XENPAK/X2 10GBASE-LRM Applications			
RoHS Compliant Package	QT2025-1	D	QT2025PRKD-1
Standard Package (w/Lead)	QT2025-1	D	QT2025PBKD-1



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