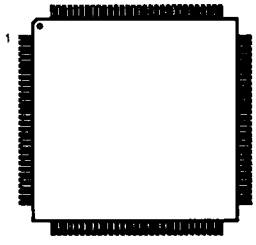
FEATURES

- ☐ Complete logic and interface circuitry, including UART, parallel to serial converter, bus interfaces and DACs
- ☐ Direct interface to IBM PC bus
- ☐ Selects internal or external modem configurations
- ☐ Simplifies layout
- ☐ CMOS technology

120 PIN PQFP PACKAGE



SC11083CQ

GENERAL DESCRIPTION

The SC11083 is part of the ST3201 chip set and includes the logic and interface circuitry required to implement a V.32 modem. The ST3201 and ST3200 chip sets with two PROMs, an SRAM and a USART provide the basic Hayes compatible V.32 modem.

The SC11083 contains a UART, that is the parallel interface between the DSP56001 and the SC11091, a parallel to serial converter, that is the interface between the SC11296 and the DSP56001, a PC bus interface, selection logic and two DACs that can be used to display the constellation.

BLOCK DIAGRAM

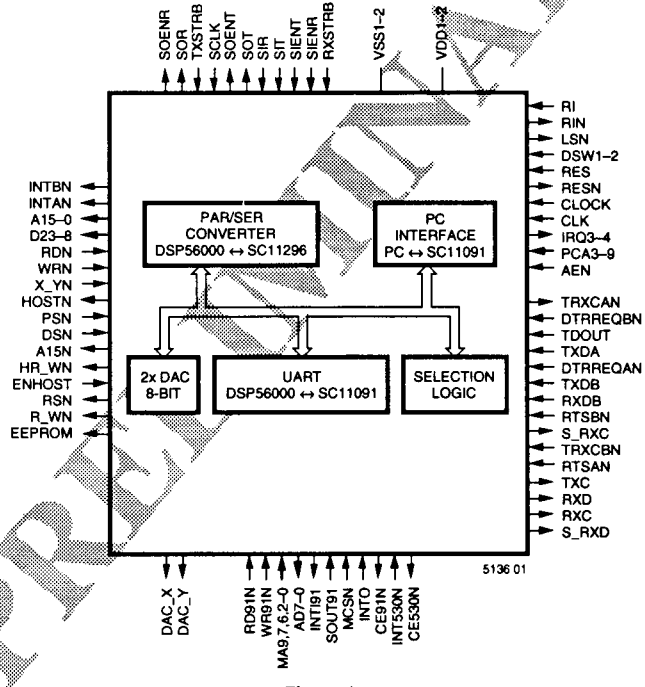


Figure 1.

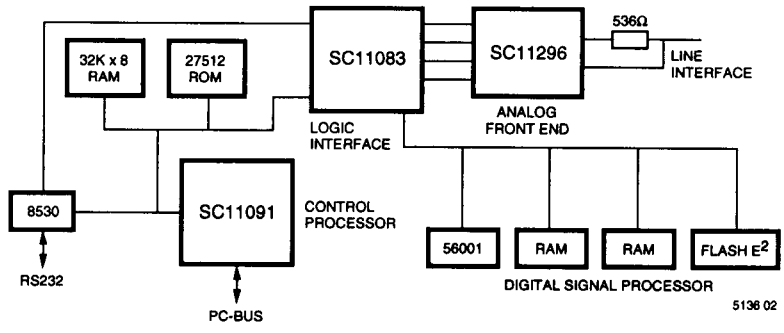
PIN DESCRIPTIONS

PIN NAME	PIN NUMBER	DESCRIPTION
A_0–A_{15}	1–14, 16, 17	**DIGITAL INPUT, TTL.** Address Bus. DSP.
A15N	42	**DIGITAL OUTPUT, TTL2.** A15 inverted.
AD_0–AD_7	55–62	**DIGITAL INPUT/OUTPUT, TTL/TTL8.** Controller.
AEN	120	**DIGITAL INPUT, TTL.** Address enable VUT.
CE530N	86	**DIGITAL OUTPUT, TTL2.** Chip enable 8530 USART.
CE91N	67	**DIGITAL OUTPUT, TTL2.** Chip enable 11091.
CLK	68	**DIGITAL INPUT, TTL.**
CLOCK	46	**DIGITAL INPUT, TTL.**
D_8–D_{23}	21–36	**DIGITAL INPUT/OUTPUT, TTL/TTL8.** Data bus DSP.
DAC_X	101	**ANALOG OUTPUT.** 8 bit "X" output for eye pattern.
DAC_Y	102	**ANALOG OUTPUT.** 8 bit "Y" output for eye pattern.
DSN	41	**DIGITAL INPUT, TTL.** Data select.
DSW_1–DSW_2	107–108	**DIGITAL INPUT, TTL/PD.** COM port selection.
DTRREQAN	96	**DIGITAL INPUT, TTL.**
DTRREQBN	99	**DIGITAL INPUT, TTL.**
EEPROMN	71	**DIGITAL OUTPUT, TTL2.** EEPROM selection.
ENHOST	44	**DIGITAL INPUT, TTL/PD.**
HOSTN	39	**DIGITAL OUTPUT, TTL2.**
HR_WN	43	**DIGITAL OUTPUT, TTL2.** Host R-W DSP.
INT530N	84	**DIGITAL INPUT, TTL/PU.** Interrupt from 8530 USART.
INTAN	20	**DIGITAL OUTPUT, TTL2.** Interrupt for DSP transmit.
INTBN	19	**DIGITAL OUTPUT, TTL2.** Interrupt for DSP receive.
INTI91	63	**DIGITAL OUTPUT, TTL2.** Interrupt to 11091.
INTO	66	**DIGITAL INPUT, TTL.**
IRQ_3–IRQ_4	111–112	**DIGITAL OUTPUT, TTL8.** Sets IRQ of host PC.
LSN	106	**DIGITAL OUTPUT, TTL8.**
MA_0–MA_2	49–51	**DIGITAL INPUT, TTL.** Address bus SC11091.
MA_6–MA_7	52–53	**DIGITAL INPUT, TTL.** Address bus SC11091.
MA9	54	**DIGITAL INPUT, TTL.** Address bus SC11091.
MCSN	65	**DIGITAL INPUT, TTL.**
PCA_3–PCA_9	113–119	**DIGITAL INPUT, TTL.** Address bus PC.
PSN	40	**DIGITAL INPUT, TTL.** Program select (active low).
R_WN	70	**DIGITAL OUTPUT, TTL2.** Read/write VUT.
RD91N	47	**DIGITAL INPUT, TTL.** Read 11091.
RDN	37	**DIGITAL INPUT, TTL.** Read DSP.
RES	109	**DIGITAL INPUT, TTL.** Reset (active high).
RESN	110	**DIGITAL OUTPUT, TTL8.** Reset (active low).
RI	103	**DIGITAL INPUT, TTL/PU.**
RIN	104	**DIGITAL INPUT, TTL2.**

PIN DESCRIPTIONS (continued)

PIN NAME	PIN NUMBER	DESCRIPTION
RSN	69	**DIGITAL OUTPUT, TTL2.**
RTSAN	90	**DIGITAL INPUT, TTL.**
RTSBN	93	**DIGITAL INPUT, TTL.**
RXC	87	**DIGITAL OUTPUT, TTL2.**
RXD	88	**DIGITAL OUTPUT, TTL2.**
RXDB	94	**DIGITAL INPUT, TTL.**
RXSTRB	83	**DIGITAL INPUT, TTL.** Receive strobe AFE.
S_RXC	92	**DIGITAL OUTPUT, TTL2.**
S_RXD	85	**DIGITAL OUTPUT, TTL2.**
SCLK	76	**DIGITAL INPUT, TTL.** SCLK for AFE.
SIENR	82	**DIGITAL INPUT, TTL.** Receive serial input enable.
SIENT	81	**DIGITAL INPUT, TTL.** Transmit serial input enable.
SIR	79	**DIGITAL INPUT, TTL.** Receive input data.
SIT	80	**DIGITAL INPUT, TTL.** Transmit input data.
SOENR	72	**DIGITAL OUTPUT, TTL2.** Receive serial output enable.
SOENT	77	**DIGITAL OUTPUT, TTL2.** Transmit serial output enable.
SOR	73	**DIGITAL OUTPUT, TTL2.** Receive output data.
SOT	78	**DIGITAL OUTPUT, TTL2.** Transmit output data.
SOUT91	64	**DIGITAL INPUT, TTL.**
TRXCBN	91	**DIGITAL INPUT, TTL.**
TXC	89	**DIGITAL OUTPUT, TTL2.**
TXDA	97	**DIGITAL INPUT, TTL.**
TXDB	95	**DIGITAL INPUT, TTL.**
TXOUT	98	**DIGITAL INPUT, TTL.**
TXRCAN	100	**DIGITAL OUTPUT, TTL8.**
TXSTRB	74	**DIGITAL INPUT, TTL.** Transmit strobe AFE.
V_{DD1}, V_{DD2}	75, 105	**DIGITAL POWER.** V_{DD} = +5V.
V_{SS1}, V_{SS2}	15, 45	**DIGITAL GROUND.** V_{SS} = 0V.
WR91N	48	**DIGITAL INPUT, TTL.** Write 11091.
WRN	38	**DIGITAL INPUT, TTL.** Write DSP.
X_YN	18	**DIGITAL INPUT, TTL.** X-Y selection DSP.

SYSTEM BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

UART

The UART is a derivative of the 8530 and functions as the parallel interface between the DSP56001 and the SC11091 controller. The following registers are available via the SC11091.

RBR Receiver buffer register. Address = 0

THR Transmitter holding register. Address = 0

IER Interrupt enable register. Address = 1

IIR Interrupt identification register. Address = 2

MCR Modem control register. Address = 4

MSM Modem status register. Address = 6

Parallel/Serial Converter

This converter is the interface between the SC11296 AFE and the DSP56001. The data must be converted from parallel to serial in order to write to the SC11296 from the the DSP56001. The data must be converted from serial to parallel to write from the SC11296 to the DSP56001. Communication between the SC11296 and the DSP56001 is interrupt driven where INTAN is the transmit interrupt and INTBN is the receive interrupt.

PC INTERFACE

This interface is for the IBM PC bus. DSW1 and DSW2 are the COM port selection signals.

DSW1	DSW2	COM PORT
0	0	1
1	0	2
0	1	3
1	1	4

Selection Logic

This logic directs the communication between the 8530 USART and the other circuits. The configuration of these signals differs for an internal (parallel) and an external (serial) modem.

DACs

The output of these two 8-bit DACs can be connected to the X and Y channels of an oscilloscope to display the received signal constellation without additional hardware.

DIGITAL OUTPUT SPECIFICATIONS

All specifications, unless otherwise indicated, are: V_{DD} = 4.5V to 5.5V, V_{SS} = 0, Junction temperature = 0 to 85°C

CLASS	DESCRIPTION	I_{OL} (mA) @ V_{OL} Max.		I_{OH} (mA) @ V_{OH} Min.		V_{OL} (V) @ I_{OH} Min.		V_{OH} (V) @ I_{OH} Min.		ITRI (µA) $V_O = V_{DD}, V_{SS}$	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
TTL2	2 mA TTL	2		2			0.4		2.4		10
TTL8	8 mA TTL	8		8			0.4		2.4		10

DIGITAL INPUT SPECIFICATIONS

All specifications, unless otherwise indicated, are: V_{DD} = 4.5V to 5.5V, V_{SS} = 0, Junction temperature = 0 to 85°C

CLASS	DESCRIPTION	V_{IH} (V)		V_{IL} (V)		I_{IH} (µA)		I_{IL} (µA)		VHYS (V)	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
TTL	Standard TTL	2			0.8		10		10		
CMOS	Standard CMOS	3.9			0.9		10		10		
PU								22	110		
PD						32	160				

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