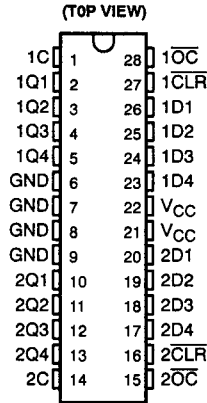


54ACT11873, 74ACT11873 DUAL 4-BIT D-TYPE LATCHES WITH 3-STATE OUTPUTS

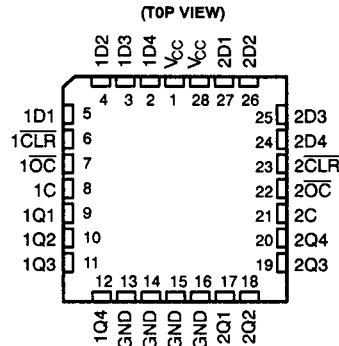
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- Inputs are TTL-Voltage Compatible
- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1- μ m Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

54ACT11873 . . . JT PACKAGE
74ACT11873 . . . DW OR NT PACKAGE



54ACT11873 . . . FK PACKAGE



FUNCTION TABLE

INPUTS				OUTPUT	
OC	CLR	C	D	Q	Q
L	L	X	X	L	L
L	H	H	H	H	H
L	H	H	L	L	L
L	H	L	X		Q_0
H	X	X	X		Z

description

These dual 4-bit registers feature 3-state outputs designed specifically for bus driving. This makes these devices particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The dual 4-bit latches are transparent D-type. When the latch enable input (1C or 2C) is high, the (Q) outputs will follow the data (D) inputs in true form, according to the function table. When the latch enable input is taken low, the outputs will be latched. When CLR goes low, the Q outputs go low independently of enable C. The outputs are in a high-impedance state when OC (output control) is at a high logic level.

The 54ACT11873 is characterized for operation over the full military temperature range of -55°C to 125°C. The 74ACT11873 is characterized for operation from -40°C to 85°C.

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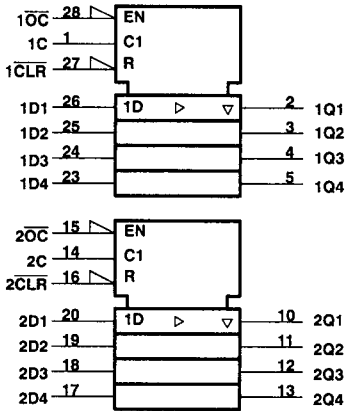


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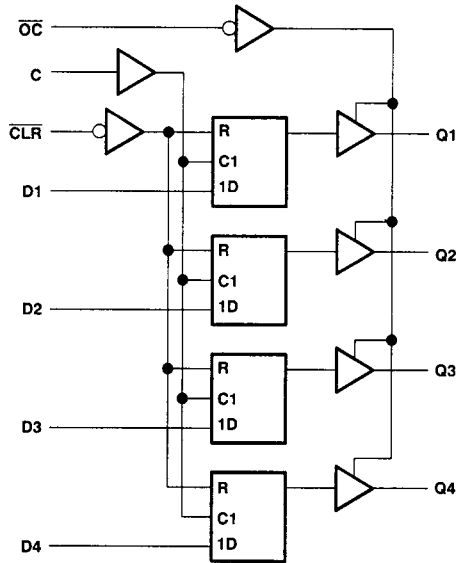
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, or NT packages.

logic diagram (positive logic)

each quad latch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	- 0.5 V to 7 V
Input voltage range, V_I (see Note 1)	- 0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Note 1)	- 0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 50 mA
Continuous current through V_{CC} or GND pins	± 200 mA
Storage temperature range	- 65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



**54ACT11873, 74ACT11873
DUAL 4-BIT D-TYPE LATCHES
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recommended operating conditions

		54ACT11873		74ACT11873		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-24	mA
I _{OL}	Low-level output current		24		24	mA
Δt/Δv	Input transition rise or fall rate	0	10	0	10	ns/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			54ACT11873		74ACT11873		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 μA	4.5 V	4.4			4.4	4.4		V	
		5.5 V	5.4			5.4	5.4			
	I _{OH} = -24 mA	4.5 V	3.94			3.7	3.8			
		5.5 V	4.94			4.7	4.8			
		5.5 V				3.85				
V _{OL}	I _{OL} = 50 μA	4.5 V			0.1	0.1	0.1		V	
		5.5 V			0.1	0.1	0.1			
	I _{OL} = 24 mA	4.5 V			0.36	0.5	0.44			
		5.5 V			0.36	0.5	0.44			
	I _{OL} = 50 mA [†]	5.5 V				1.65				
		5.5 V					1.65			
I _{OZ}	V _O = V _{CC} or GND	5.5 V		±0.5		±10	±5	μA		
I _I	V _I = V _{CC} or GND	5.5 V		±0.1		±1	±1	μA		
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			8	160	80	μA		
ΔI _{CC} [‡]	One input at 3.4 V, Other inputs at GND or V _{CC}	5.5 V			0.9	1	1	mA		
C _i	V _I = V _{CC} or GND	5 V		4.5				pF		
C _o	V _O = V _{CC} or GND	5 V		13.5				pF		

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V to V_{CC}.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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 WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Note 2)

PARAMETER			$T_A = 25^\circ\text{C}$		54ACT11873		74ACT11873		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLR low	5		5		5		ns
		Enable C high	5		5		5		
t_{su}	Setup time, data before C \downarrow	Data high	6				6		ns
		Data low	3				3		
t_h	Hold time, data after C \downarrow	Data high	0				0		ns
		Data low	0		0		0		

switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54ACT11873		74ACT11873		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	4.4	7.2	8.8	4.4	10.9	4.4	10	ns
t_{PHL}			3	6.6	9.1	3	10.9	3	10.2	
t_{PLH}	C	Q	4.7	8.1	10	4.7	12.3	4.7	11.3	ns
t_{PHL}			5.2	8.9	10.9	5.2	13.3	5.2	12.3	
t_{PHL}	CLR	Q	2.9	6.5	9	2.9	10.7	2.9	10	ns
t_{PZH}	\overline{OC}	Q	1.9	4.9	7.1	1.9	8.5	1.9	8	ns
t_{PZL}			2.7	6.4	9.1	2.7	11.1	2.7	10.3	
t_{PHZ}	\overline{OC}	Q	5.7	8	9.5	5.7	10.6	5.7	10.2	ns
t_{PLZ}			5.2	7.8	9.1	5.2	10.2	5.2	9.8	

NOTE 2: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per latch	Outputs enabled	$C_L = 50\text{ pF}$, $f = 1\text{ MHz}$		40	μF
		Outputs disabled			7	