Signetics

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Status	Product Specification
FAST Products	

FAST 74F841/842/843/844/845/846
Bus Interface Latches

'F841/'F842 10-Bit Bus Interface Latches, NINV/INV (3-State)
'F843/'F844 9-Bit Bus Interface Latches, NINV/INV (3-State)
'F845/'F846 8-Bit Bus Interface Latches, NINV/INV (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F841, 74F842	5.5ns	60mA
74F843, 74F845	5.5ns	75mA
74F844, 74F846	6.2ns	60mA

FEATURES

- **High speed parallel latches**
- **Extra data width for wide address/data paths or busses carrying parity**
- **High impedance NPN base input structure minimizes bus loading**
- **I_{IL} is 20μA vs 1000μA for AM29841 series**
- **Buffered control inputs to reduce AC effects**
- **Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors**
- **Positive and negative over-shoots are clamped to ground**
- **3-state outputs glitch free during power-up and power-down**
- **48mA sink current**
- **Slim Dip 300 mil package**
- **Broadside pinout**
- **Pin-for-pin and function compatible with AMD AM29841-846 series**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F841N, N74F842N, N74F843N, N74F844N, N74F845N, N74F846N
24-Pin Plastic SOL	N74F841D, N74F842D, N74F843D, N74F844D, N74F845D, N74F846D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_n	Data inputs	1.0/0.033	20μA/20μA
LE	Latch Enable input	1.0/0.033	20μA/20μA
$\overline{OE}$, $\overline{OE}_n$	Output Enable input (active-Low)	1.0/0.033	20μA/20μA
$\overline{MR}$	Master Reset input (active-Low)	1.0/0.033	20μA/20μA
$\overline{PRE}$	Preset input (active-Low)	1.0/0.033	20μA/20μA
Q_n	Data outputs	1200/80	24mA/48mA
$\overline{Q}_n$	Data outputs	1200/80	24mA/48mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20μA in the High state and 0.6mA in the Low state.

DESCRIPTION

The 'F841-'846 bus interface latch series are designed to provide extra data width for wider address/data paths of busses carrying parity.

The 'F841-'F846 series are functionally and pin compatible to the AMD AM29841-AM29846 series.

The 'F841 consists of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is Low. When $\overline{OE}$ is High the output is in the High-impedance state.

The 'F842 is the inverted output version of 'F841.

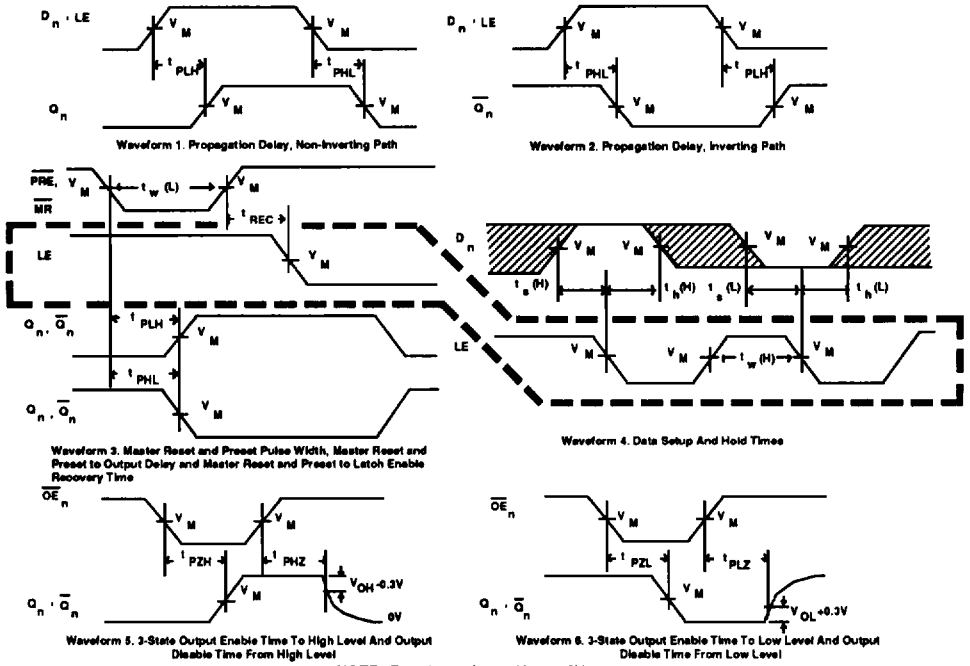
The 'F843 consists of nine D-type latches with 3-state outputs. In addition to the LE and $\overline{OE}$ pins, the 'F843 has a Master Reset ($\overline{MR}$) pin and Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs are Low if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered into the latch. When $\overline{PRE}$ is Low, the outputs are High, if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$.

The 'F844 is the inverted output version of 'F843.

The 'F845 consists of eight D-type latches with 3-state outputs. In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 'F845 has two additional $\overline{OE}$ pins making a total of three Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) pins. The multiple Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$.

The 'F846 is the inverted output version of 'F845.

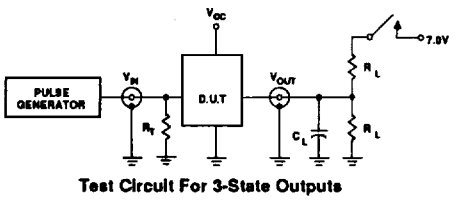
AC WAVEFORMS



NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

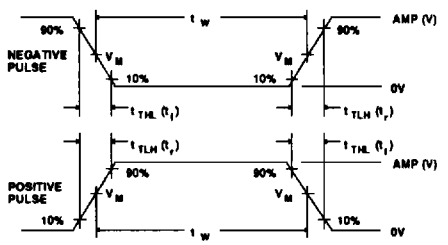
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



$V_M = 1.5V$

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns