

3071

T-49-12-05

CMOS LSI

Audio-Use Digital Signal Processor

©3124

Overview

The LC8301A is a digital signal processor suitable for digital audio processing. It incorporates independent left and right signal processing units and a common control unit that allow simultaneous processing of a stereo signal in each instruction cycle. This effectively doubles processing speed compared to a conventional single-processing unit processor. Each processing unit contains a multiplier, ALU, accumulator, working registers, data RAM, coefficient RAM and constant ROM. The high speed of the LC8301A makes it ideal for a wide range of advanced audio signal processing applications with a single chip. These include

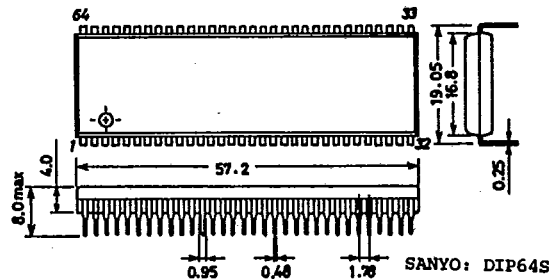
- Stereo graphic equalizers
- Stereo audio filters
- Spectrum analyzer power calculations
- Sound field creation (using external DRAM)

The LC8301A operates from a single 5V supply, and is available in 64-pin shrink DIPs. An evaluation device, the LC83EV01, is also available in 100-pin PGAs.

Features

- Single-chip stereo audio digital signal processor
- 108ns cycle time (at 48kHz sampling rate)
- Up to 256K bytes of external DRAM provide high storage capacity.
- 64-pin shrink DIP
- Single 5V supply

Case Outline 3071-D64IC
(unit: mm)



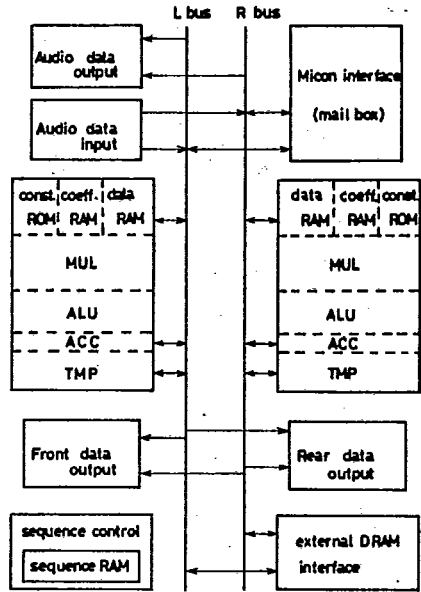
5229TA,TS No.3124-1/3

LC8301A

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Pinout and Block Diagram

P0	1	64	SRDY
P1	2	63	SIK
P2	3	62	SIR0
P3	4	61	SICK
P4	5	60	SI
P5	6	59	SOAK
AOTDF 1	7	58	SOR0
AOTDF 2	8	57	SOCK
DFBCK	9	56	SO
DFWCK	10	55	AOWCK
RAS	11	54	ASO
CAS	12	53	AOBCK
DREAD	13	52	TEST 4
DWRT	14	51	TEST 3
VDD1	15	50	TEST 2
OSC 1	16	49	TEST 1
OSC 2	17	48	VSS 2
VSS1	18	47	INT
FS3840	19	46	RES
D0	20	45	VDD 2
D1	21	44	TEST 5
D2	22	43	SELC
D3	23	42	LRCKI
D4	24	41	LRCKO
D5	25	40	ASI 2
D6	26	39	ASI 1
D7	27	38	BCK 2
A0	28	37	BCK 1
A1	29	36	A8
A2	30	35	A7
A3	31	34	A6
A4	32	33	A5



Pin Description

Pin Name	I/O	Pin Number	Description
VDD 1, 2	I	15, 45	Positive +5V supply. Both pins must be connected.
VSS 1, 2	I	18, 48	Supply ground. Both pins must be connected.
ASI 1	I	39	Serial audio data input 1.
ASI 2	I	40	Serial audio data input 2.
BCK 1	I	37	Bit clock for ASI 1.
BCK 2	I/O	38	Bit clock for ASI 2. This pin 3 selected to be input or output under program control.
LRCKI	I	42	Left/right channel select input clock High : left channel Low : right channel
LRCKO	O	41	Left/right channel select output clock.
ASO	O	54	Serial audio data output.
AOBCK	O	53	ASO bit clock, Clock frequency is 32fs or 48fs.
AOWCK	O	55	ASO word clock.
AOTDF 1	O	7	Auxiliary audio data output 1. Used for presence output signal.
AOTDF 2	O	8	Auxiliary audio data output 2. Used for presence output signal.
DFBCK	O	9	AOTDF 1 and AOTDF 2 bit clock. Clock frequency is 32fs or 48fs.
DFWCK	O	10	AOTDF 1 and AOTDF 2 word clock.
RAS	O	11	RAS output for external DRAM
CAS	O	12	CAS output for external DRAM
DREAD	O	13	Data read signal for external DRAM
DWRT	O	14	Data write signal for external DRAM
A0 to 8	O	28 to 36	Address outputs for external DRAM. A0 to A7 are used for 64K x 4 DRAMs, A0 to A8 are used for 256K x 4 DRAMs.
D0 to 7	I/O	20 to 27	Data inputs/outputs for external DRAM. D0 to D3 are used for a single DRAM, D0 to D7 are used for two DRAMs.

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Pin Name	I/O	Pin Number	Description
SI	I	60	Serial data input from the controlling microprocessor. 8-bit data format.
SICK	I	61	Bit clock for SI.
SIRQ	I	62	Acknowledge to request for serial input data transfer.
SIACK	O	63	Acknowledge to request for serial input data transfer.
SRDY	I	64	Serial input data transfer complete.
SO	O	56	Serial data output to controlling microprocessor. 8-bit data format.
SOCK	I	57	Bit clock for SO.
SORQ	I	58	Request for serial output data transfer.
SOACK	O	59	Acknowledge to request for serial output data transfer.
P0 to 5	I/O	1 to 6	General-purpose input/output port. All pins have internal pull-up resistors.
OSC 1	I	16	Crystal oscillator pin. Connect an external crystal, or input a 384fs external clock.
OSC 2	O	17	Crystal oscillator pin. Connect an external crystal, or leave open if an external clock is used.
FS3840	O	19	384fs reference clock output.
INT	I	47	Interrupt request.
RES	I	46	Reset input
SELC	I	43	Reference clock source select High : internal oscillator Low : external clock
TEST 1 to 4	I	49 to 52	Connect to ground.
TEST 5	O	44	Leave open.

Functional Description**[Signal processing units]**

Each of the left- and right-channel signal processing units contains the following elements.

- 24×16-bit multiplier
- Arithmetic-logic unit capable of 32-bit arithmetic operations and 24-bit arithmetic/logic operations
- 32-bit accumulator (ACC)
- Eight, 32-bit working registers (TMP)
- Internal memory :
 128×4-bit data RAM 256×16-bit coefficient RAM 256×24-bit constant ROM

[Sequence control]

The LC8301A program is stored in the internal 320×32-bit program memory. Subroutine calls can be nested up to four levels.

An interrupt request pin provides a vectored interrupt function. An 12-bit interval timer is included.

[Audio data interface]

Audio input and output data are serial. the single input port is configurable for a variety of audio data formats. The three output ports are configurable for four different data formats.

[External DRAM interface]

External DRAMs can be used to provide high-capacity data storage for applications such as echo and reverberation processing, where internal data RAM is insufficient.

The LC8301A provides all interface signals required for up to 256K bytes of external DRAM. One or two 64K×4-bit or 256K×4-bit DRAMS can be used. Up to 16 DRAM accesses per sample period.

[Microprocessor interface]

Input and output to the controlling microprocessor is through an 8-bit synchronous serial interface.

The LC8301A contains an 8×16-bit mailbox for incoming data.

A general-purpose 6-bit I/O port allows construction of a simple interface to other devices.

[Timing]

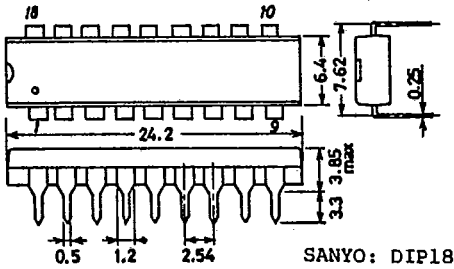
The reference clock can be generated by the internal crystal oscillator or input from an external source. The clock frequency is 384 times the sampling frequency. Instruction cycle time is two clock cycles.

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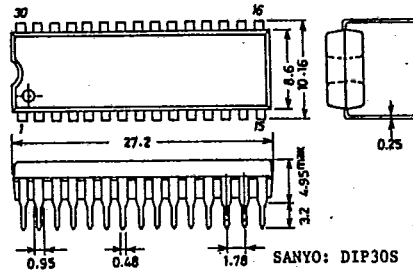
CASE OUTLINES OF 8/4-BIT MICROCOMPUTERS, GATE ARRAYS

- All of Sanyo microcomputer case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.

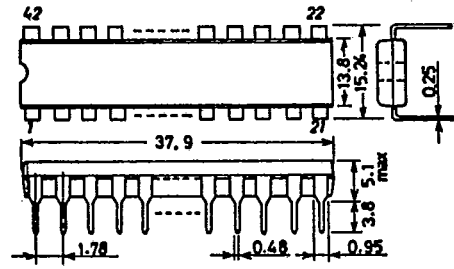
Case Outline—[3007A] unit: mm



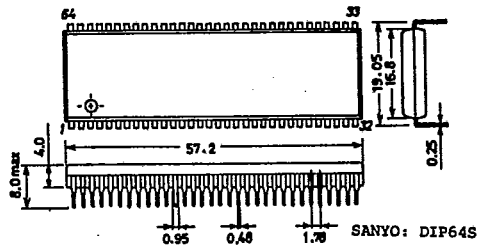
Case Outline—[3061] unit: mm



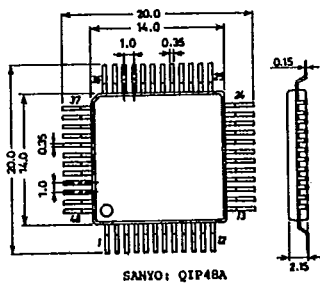
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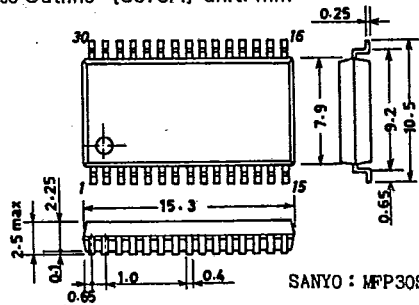
Case Outline—[3071] unit: mm



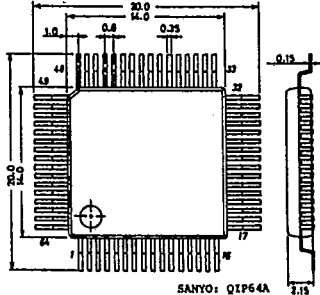
Case Outline—[3052A] unit: mm



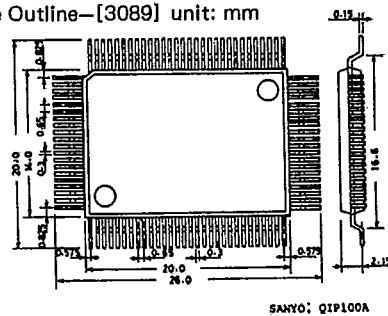
Case Outline—[3073A] unit: mm



Case Outline—[3057] unit: mm

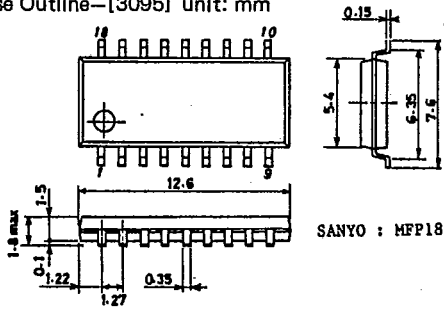


Case Outline—[3089] unit: mm

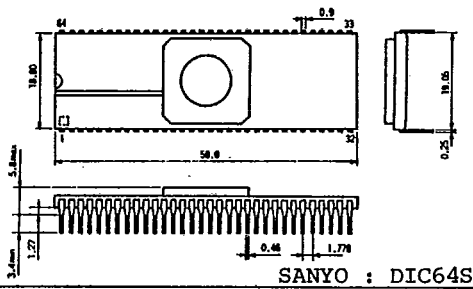


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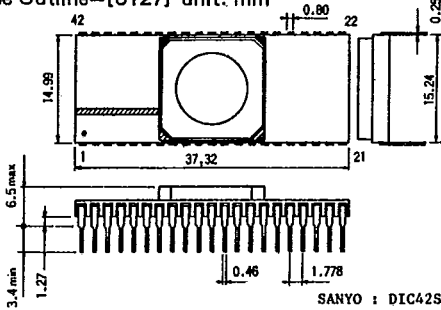
Case Outline-[3095] unit: mm



Case Outline-[3126] unit: mm



Case Outline-[3127] unit: mm



Case Outline-[3128] unit: mm

