VLSI Technology

Preliminary

ARM7TDMI

Enhanced High Performance Low Cost 32-Bit RISC Processor Core

OVERVIEW

VLSI's ARM7TDMI family of high-performance core just got better. We not only have the fastest 0.35µm implementation in the industry today, but we continue to lead the trend by introducing our new ARM7TDMI at 0.25µm and 0.20µm process. The ARM7TDMI is fully static, and supports both the 32-bit ARM and the 16-bit THUMB instruction sets. It is ideal for cost sensitive, high performance embedded applications.

THE THUMB CONCEPT

In the THUMB mode, the ARM7TDMI executes 16-bit instructions. This optimizes performance when using 16- or 8-bit memory interfaces, while maintaining the richness of the 32-bit architecture. THUMB's 16-bit instruction length allows it to gain 30% improvement in code density over standard ARM code, resulting in less memory usage, thereby lowering product cost.

DEVELOPMENT TOOLS

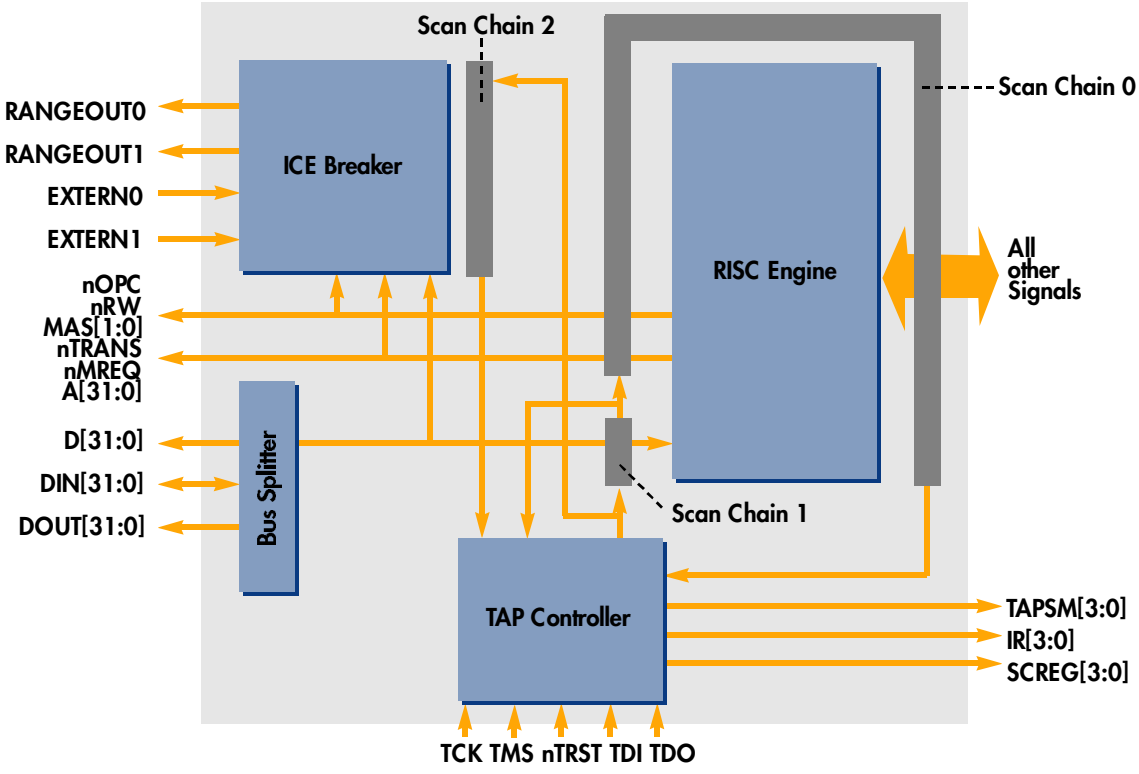
For your development needs, VLSI offers the JumpStart™ ARM software development environment with full support for the ARM/THUMB instruction sets. This suite of graphical tools includes libraries and performance utilities for building, debugging, and optimizing your ARM application. The PID7T development platform enables early hardware evaluation and prototyping. The PID board includes the processor, memory, FPGA, JTAG debug, serial and parallel interfaces, and logic analyzer headers. VLSI offers software tools, evaluation boards, test chips, and technical support to help your product get to market faster.

APPLICATIONS

The ARM7TDMI is ideal for embedded applications requiring high performance within cost and power constraints:

- Portable telecom
- Data communications
- Hand-held computing
- Consumer multimedia
- Powerful real-time control
- Automotive control

ARM7TDMI Core Block Diagram

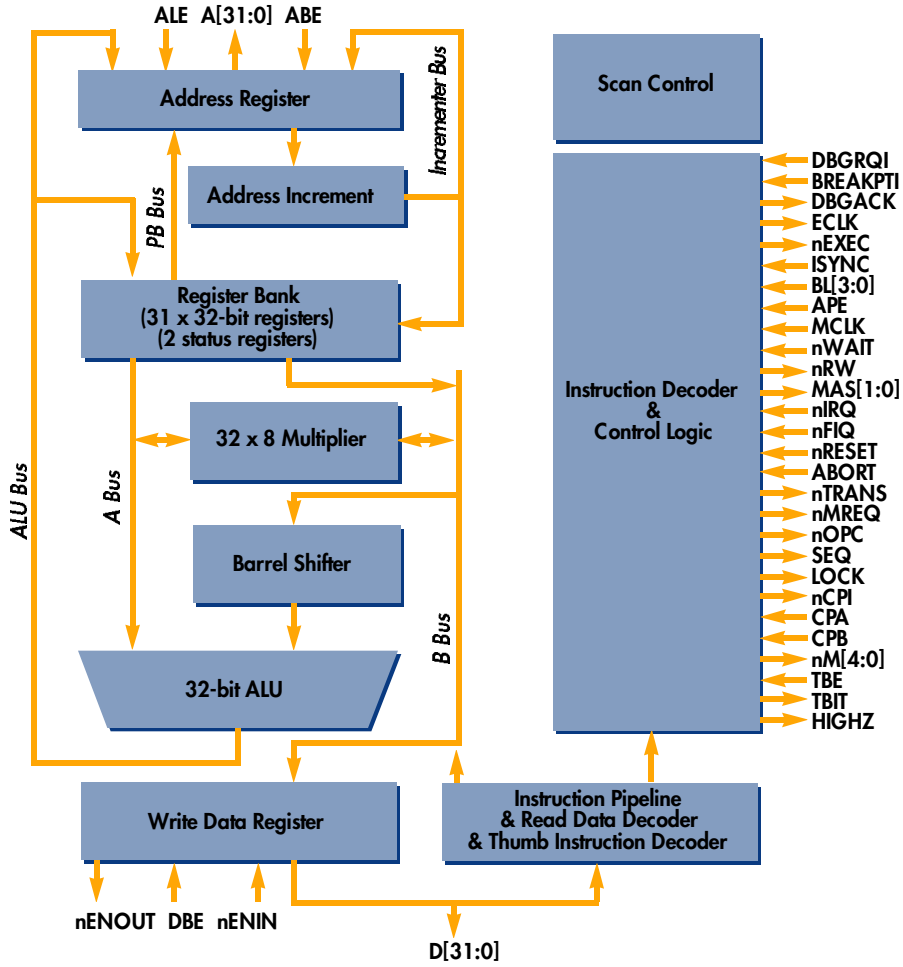


SPECIFICATIONS ARM7TDMI

Core Part Number	VVF7101	VVF7102	VVF7103
Technology (µm)	0.35	0.25	0.20
Die Size (mm^2)	2.2	1.1	0.90
Clock Frequency (MHz) WC*/TYP**	70/105	115/180	110/185
Voltage (V)	3.0 - 3.6	2.25 - 2.75	1.62 - 1.98
MIPS (Dhrystone 2.1) WC/TYP	63/95	103/162	99/167
mA/mHz	0.27	TBD	TBD
Cache	None	None	None
Write Buffer	None	None	None

*WC = Worst Case = -10% VDD, Slow Silicon, 125ºCj **TYP = Typical = Nominal VDD, Typical Silicon, 25ºCj

Risc Engine Block Diagram



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