BIPOLAR HIGH-SPEED 8-BIT FLASH A/D CONVERTER

DESCRIPTION

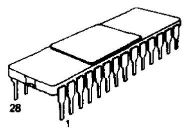
The TS 83048 is a monolithic bipolar 8-bit parallel flash analog-to-digital converter designed for applications requiring very high-speed conversion.

The TS 83048 is an alternate source of the TDC 1048, TDC 1038, AD 9048 but offers enhancements over its predecessors, mainly in terms of dynamic performance.

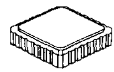
The TS 83048 uses 256 parallel comparators to digitize fast moving analog input signals without external sample-and-hold circuits or input buffers.

With encode rates up to 60 MHz, the TS 83048 is able to operate from commercial to military temperature range with an analog input frequency of 30 MHz, making it ideal for a variety of applications and environments.

The TS 83048 is packaged in hermetic ceramic 28-pin DIL configuration, in LCCC 28 and is also available in die form.



C
DIL 28
(Ceramic package)



E
LCCC 28
(Leadless Ceramic Chip Carrier package)

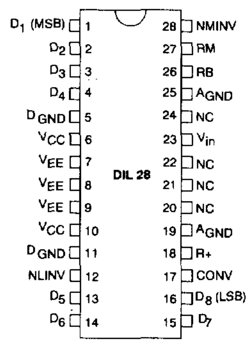
MAIN FEATURES

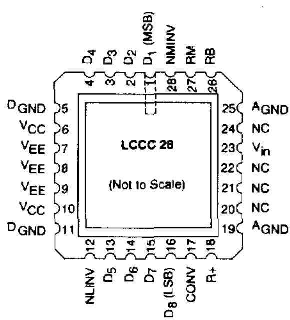
- 8-bit resolution.
- 60 MHz sampling rate.
- Excellent SNR.
- Low power : 0.46 W.
- Dual power supply : 5 V and – 5.2 V.
- – 55°C / + 125°C specified.
- Guaranteed monotonicity.
- High slew rate of input stages.
- Compatible with TDC 1038, TDC 1048, AD 9048.
- Input and output TTL compatible.
- Output registers.
- No sample & hold required.
- Evaluation board : TSEV-83048.
- Space evaluation performed by CNES (PPL CNES).
- DESC/SMD planned.

APPLICATIONS

- Space applications.
- Military systems.
- Video digitizing.
- Image processing.
- Medical imaging.
- High-energy physics.
- X-Ray and ultrasound imaging.
- Communication/signal intelligence.

PIN CONNECTIONS
(Top view)





Note : For details, see «pin description»

ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Value	Unit
Positive supply voltages (Note 2)	V_{CC}	4 to +6	V
Negative supply voltages (Note 2)	V_{EE}	−6.2 to −4	V
Upper reference voltage	R_T	V_{EE} to +0.5	V
Midpoint reference current	R_M	5	mA
Lower reference voltage	R_B	V_{EE} to +0.5	V
Differential reference voltage	$R_T - R_B$	2.2	V
Analog input (Note 2)	V_{IN}	V_{EE} to +0.5	V
Digital input voltage (Note 2)	CONV	0 to V_{CC}	V
Digital input voltage (Note 2)	NMINV, NLINV	0 to V_{CC}	V
Digital output currents	I_D	30	mA
Junction temperature	T_j	175	°C
Storage temperature	T_{stg}	−65 to +150	°C
Operating temperature range	T_{case}	−55 to +125	°C
Lead temperature (soldering 10 s)	T_{leads}	+260	°C

Note 1 : Absolute maximum ratings are limiting values applied individually while other parameters are within specified operating conditions.
Long exposure to maximum rating may affect device reliability.

Note 2 : With respect to AGND = DGND.

USER WARNING

The power supplies must be applied before all the other signals to prevent damage from occuring on the device.

To prevent reliability problem and dynamic performance damage, high speed transition on power supply must be avoided.

SPECIFICATIONS

Electrical operating characteristics

$V_{CC} = 5\,V$; $V_{EE} = -5.2\,V$; $T_C = 25°C$ (unless otherwise specified)

Parameter	T_{case}	Test level	Min.	Typ.	Max.	Unit
RESOLUTION				8		Bits
DIGITAL INPUTS AND OUTPUTS						
Logic compatibility						
Digital inputs						
• Logic «0» voltage	full	IV	0		0.8	V
• Logic «1» voltage	full	IV	2		5	V
Digital output						
• Logic «0» voltage (Note 1)	full	II, D	0		0.5	V
• Logic «1» voltage	full	II, D	2.4		4.4	V
• Output delay (Note 2)		IV		4		ns
MAXIMUM CLOCK FREQUENCY		I, D	50	60		MHz
ANALOG INPUT						
Voltage range		V		V_{REF}		V
Input capacitance		IV		12	20	pF
Input resistance		V		50		kΩ
Analog bandwidth (Note 3)		V		100		MHz
REFERENCE INPUT						
Positive reference voltage		I, D	−1	0	0.3	V
Negative reference voltage		I, D	−2.5	−2	−1	V
Differential reference voltage		I, D		2	2.5	V
Reference ladder resistance		I, D	125	165	205	Ω
	full	II	90		260	Ω
POWER REQUIREMENTS						
Power supply						
• Positive supply		I, D	4.5	5	5.5	V
	full	II	4.5	5	5.5	V
• Negative supply		I, D	−5.7	−5.2	−4.7	V
	full	II	−5.7	−5.2	−4.7	V
Power dissipation						
• Positive supply		I, D		90	150	mW
	full	II		100	200	mW
• Negative supply		I, D		370	500	mW
	full	II		400	550	mW
THERMAL RESISTANCE		V				
Junction-to-ambient (still air)						
• Ceramic DIL				45		°C/W
• Leadless Ceramic LCCC				50		°C/W
Junction-to-case						
• Ceramic DIL				6		°C/W
• Leadless Ceramic LCCC				12		°C/W
ACCURACY (Note 4)						
Differential nonlinearity		I, D		±0.4	±0.65	LSB
	full	II		±0.6	±0.75	LSB
Integral nonlinearity		I, D		±0.4	±0.65	LSB
	full	II		±0.6	±0.75	LSB
Monotonicity and no missing codes	full	IV	Guaranteed over specified temperature range			

SPECIFICATIONS (Continued)

Electrical operating characteristics

V_{CC} = 5 V ; V_{EE} = −5.2 V ; T_C = 25°C (unless otherwise specified)

Parameter	Test level	Min.	Typ.	Max.	Unit
DYNAMIC CHARACTERISTICS (Note 5)					
Signal to noise ratio					
F_S = 50 MHz F_{in} = 1 MHz	I	43.9	45		dB
F_S = 20 MHz F_{in} = 10 MHz	I	40.9	43.9		dB
F_S = 35 MHz F_{in} = 10 MHz	I	40.2	42.5		dB
F_S = 35 MHz F_{in} = 17 MHz	I	36.6	40		dB
F_S = 1 MHz F_{in} = 0.1 MHz	D	43.9	45		dB
Total harmonic distorsion					
F_S = 50 MHz F_{in} = 1 MHz	I	48	55		dB
F_S = 20 MHz F_{in} = 10 MHz	V		48		dB
F_S = 35 MHz F_{in} = 10 MHz	V		48		dB
F_S = 35 MHz F_{in} = 17 MHz	V		42		dB
F_S = 1 MHz F_{in} = 0.1 MHz	D	48	55		dB
Number of effective bits					
F_S = 50 MHz F_{in} = 1 MHz	I	7	7.2		Bits
F_S = 20 MHz F_{in} = 10 MHz	I	6.5	7		Bits
F_S = 35 MHz F_{in} = 10 MHz	I	6.4	6.8		Bits
F_S = 35 MHz F_{in} = 17 MHz	I	5.8	6.3		Bits
F_S = 1 MHz F_{in} = 0.1 MHz	D	7	7.2		Bits
Aperture uncertainty	V		20		pS
Differential phase	V		1		degree
Differential gain	V		2		%

Note 1 : With I_{OUT} = −4 mA.
Note 2 : See timing diagram.
Note 3 : The analog input frequency at which the spectral power of the fundamental frequency (as determined by FFT analysis) is reduced by 3 dB.
Note 4 : Histogram based on sampling of 100 kHz sinusoïdal analog signal with and encoding rate of 1 MHz.
Note 5 : Dynamic measurements are performed with an analog input signal 1 dB below full scale.

EXPLANATION OF TEST LEVELS

Test level	
I	100 % production tested.
II	100 % production tested at +25°C, and sample tested at specified temperature
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
D	100 % probe tested on wafer at T_{amb} = +25°C.

TIMING DIAGRAM

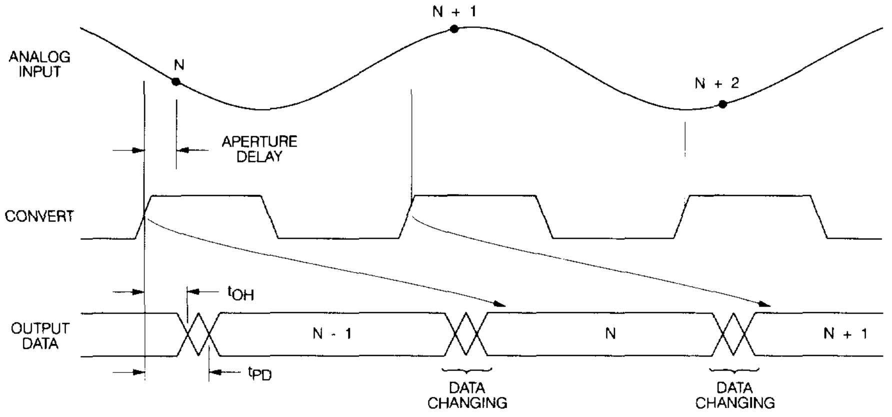


Figure 1

SWITCHING PERFORMANCES (see Note)

Parameter	Symbol	Typ.	Unit
Aperture delay		2	ns
Output hold time	t_{oh}	2	ns
Ouput delay	t_{pd}	4	ns
Rise time		5	ns
Fall time		5	ns
Conversion rate		60	MHz
Note : Output terminated with 40 pF and a 810 Ω pull up resistor.			

FUNCTIONAL BLOCK DIAGRAM

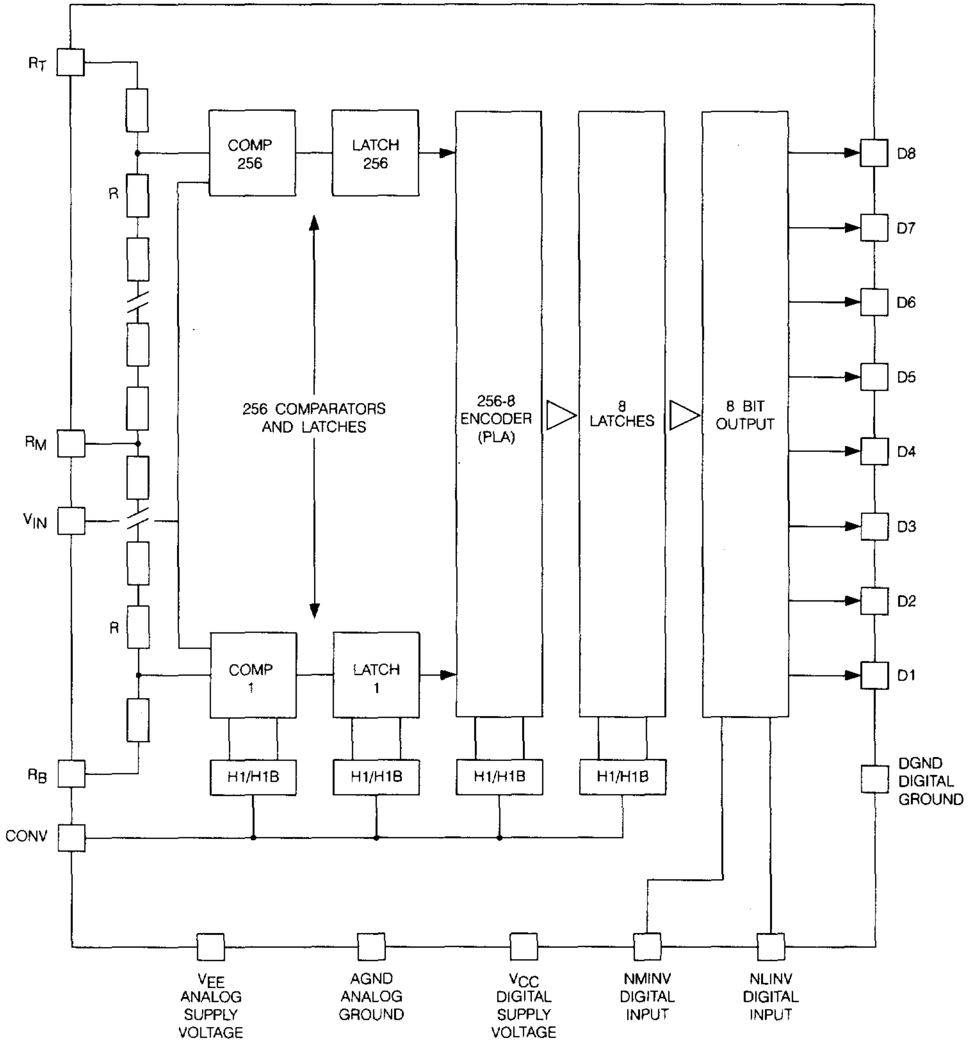


Figure 2

PIN DESCRIPTION

Pin DIL or LCCC	Symbol	Function	Description
1	D1	Digital data output (MSB)	TTL compatible
2	D2	Digital data output	
3	D3	Digital data output	
4	D4	Digital data output	
5	D_{GND}	Digital ground	0 V
6	V_{CC}	Positive digital supply	+ 5 V
7	V_{EE}	Negative analog supply	− 5.2 V
8	V_{EE}	Negative analog supply	− 5.2 V
9	V_{EE}	Negative analog supply	− 5.2 V
10	V_{CC}	Positive digital supply	+ 5 V
11	D_{GND}	Digital ground	0 V
12	NLINV	Not least significant bit invert	TTL compatible
13	D5	Digital data output	TTL compatible
14	D6	Digital data output	
15	D7	Digital data output	
16	D8	Digital data output (LSB)	
17	CONV	Convert	TTL compatible
18	RT	Positive reference voltage input	0 V
19	GND	Analog ground	
20	NC	Not connected	
21	NC	Not connected	
22	NC	Not connected	
23	V_{IN}	Analog input	− 2 V ; 0 V
24	NC	Not connected	
25	GND	Analog ground	
26	RB	Negative reference voltage input	− 2 V
27	RM	Reference mid point	− 1 V
28	NMINV	Not most significant bit invert	TTL compatible

Truth table of the TS 83048

Step	Range		Binary True	Binary Inverted	Offset twos complement True	Offset twos complement Inverted
	− 2.000 V FS 7.8431 mV Step	− 2.0480 V FS 8.000 mV Step	NMINV = 1 NLINV = 1	0 0	0 1	1 0
000	0.0000 V	0.0000 V	00000000	11111111	10000000	01111111
001	− 0.0078 V	− 0.0080 V	00000001	11111110	10000001	01111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
127	− 0.9961 V	− 1.0160 V	01111111	10000000	11111111	00000000
128	− 1.0039 V	− 1.0240 V	10000000	01111111	00000000	11111111
129	− 1.0118 V	− 1.0320 V	10000001	01111110	00000001	11111110
•	•	•	•	•	•	•
•	•	•	•	•	•	•
•	•	•	•	•	•	•
254	− 1.9921 V	− 2.0320 V	11111110	00000001	01111110	10000001
255	− 2.0000 V	− 2.0400 V	11111111	00000000	01111111	10000000

THEORY OF OPERATION

The block diagram (see page 6) shows a conventional flash converter structure having one comparator per state. This architecture enables high speed operation, without external sample and hold.

The analog input signal is fed to all comparators, and is compared to a set of 256 reference levels (8 bits), derived from a resistor ladder network.
Midpoint tap (1/2 V_{REF}) of the reference ladder is provided for linearity adjustment or transfer function modification.

A set of 256 AND latches following the comparator array indicates the appropriate quantization level of the analog input signal.
An encoder stage (R.O.M.) followed output latches provides output data in binary code, followed by high speed TTL output buffers.

APPLICATIONS

Functional description

The TS 83048 operates with input analog signals varying between ± V_{REF} reference voltages, (Nominally $+V_{REF} = 0$ V, $-V_{REF} = -2$ V), applied across an internal resistor ladder.

Maximum differential Reference voltage is 3 V, so external reference generator circuit must limit the voltage to this value, to avoid permanent damage caused to the TS 83048 by excessive current densities.

The typical input capacitance of the TS 83048 is 12 pF, which can be driven directly by most 50 Ω signal sources, otherwise it needs simple buffering requirements.

Full logic TTL input clock signals are recommended for the TS 83048, with fast rise and fall times 1 ns especially when digitizing high frequency input waveforms.
Although the TS 83048 is designed and tested to operate with a 50 % clock cycle, dynamic performance at high data rates can be improved by changing the duty clock cycle.

Output datas is TTL logic compatible.

Two output format control pins, NMINV and NLINV, are provided. These controls are for DC (i.e., steady state) use. They permit the output coding to be either straight binary or offset two's complement, in either true or inverted sense, according to the *Output Coding Table*. These active LOW pins may be tied to V_{CC} (through a 4.7 kΩ resistor) for a logic 1 or D_{GND} for a logic 0.

Packaging

The TS 83048 is mounted in ceramic 28-pin DIL or LCC packages.
Sockets may be used for prototype evaluation, but should be avoided afterwards, because it leads to increased decoupling difficulties, and limitations of TS 83048 dynamic performance.

TYPICAL EVALUATION CIRCUIT (see page 9)

Designs involving the TS 83048 must follow a few precautions to ensure optimum performance. The following design suggestions are essentially meant to avoid many of the high-speed design problems.

Multilayer printed circuit board is recommended, because it enables compact implementation, and allows easy design of low impedance continuous Supply and Ground planes.
All ground pins should be connected to the ground plane as close to the package as possible.
Proper supply decoupling by high resonant frequency chip capacitors close to the device, and high quality tantalum capacitor at each power supply incoming, is especially recommended.

The length of digital input/output signal paths should be matched and kept short, to avoid propagation delay mismatches, increased output bits time skew, and over or undershoot caused by reflections.

So long as propagation delay along the line is shorter than digital signal rise or fall time, the reflection has little effect on the wave form.
However, if long interconnection lengths cannot be avoided, proper design of transmission line impedance with adapted TTL termination loads has to be observed.

50 Ω impedance microstrip line with 50 Ω termination chip resistors should be used for analog and clock input pins.

TYPICAL EVALUATION CIRCUIT

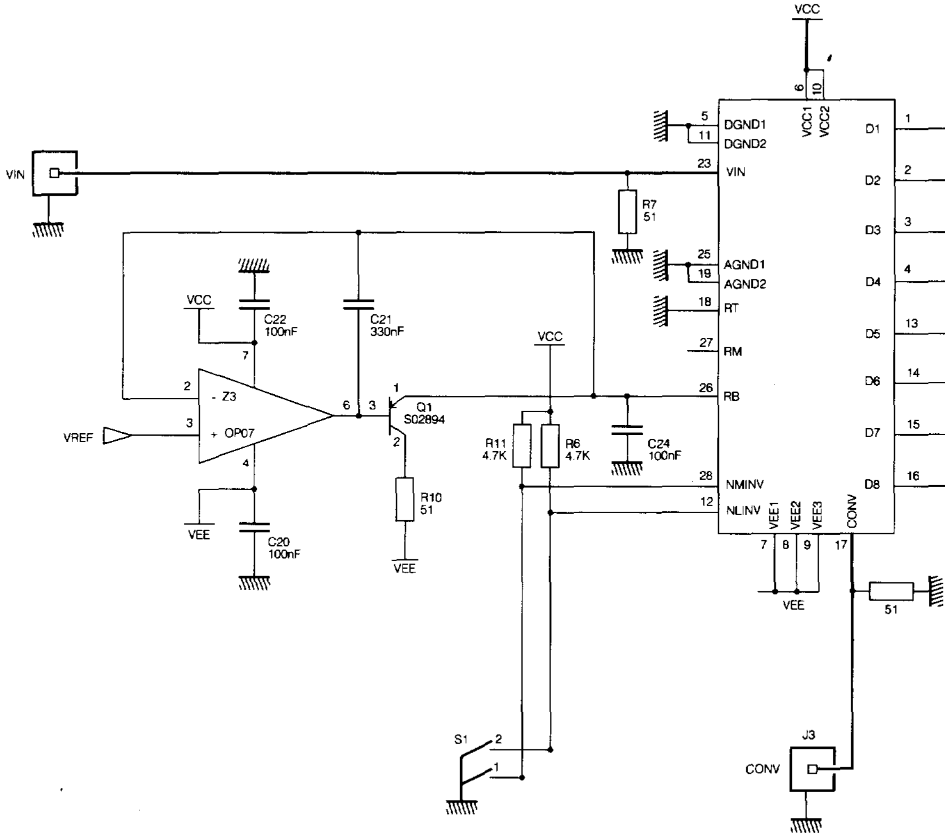


Figure 3

TYPICAL PERFORMANCE CURVES

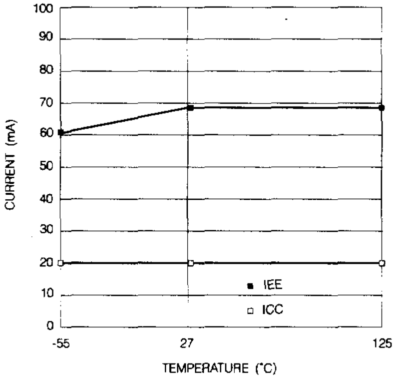


Figure 4 : Supply currents.

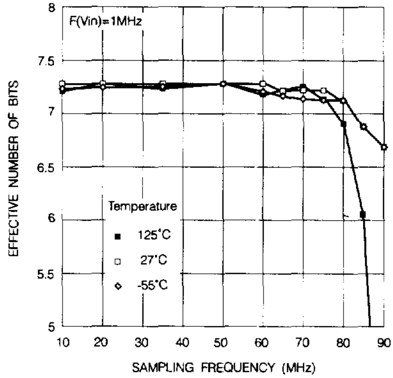


Figure 5 : Effective number of bits in oversampling mode.

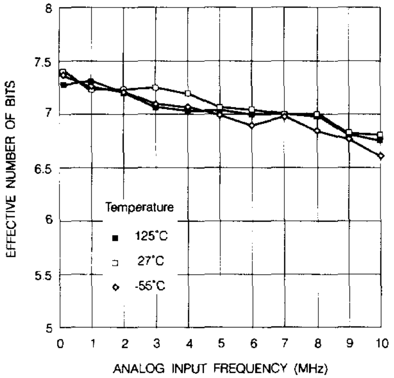


Figure 6 : Dynamic characteristics at 20 MHz sampling frequency.

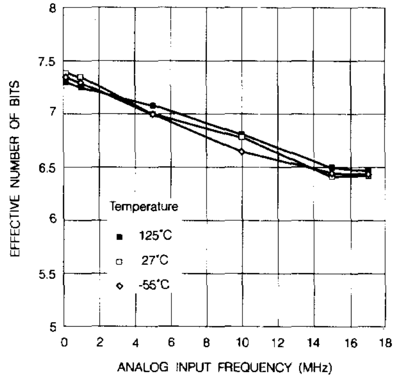


Figure 7 : Dynamic characteristics at 35 MHz sampling frequency.

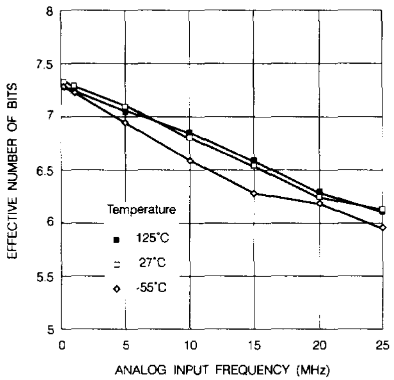


Figure 8 : Dynamic characteristics at 50 MHz sampling frequency.

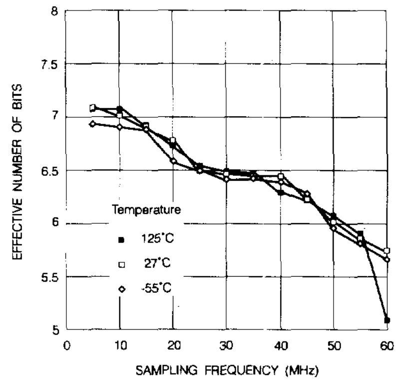


Figure 9 : Dynamic performance at nyquist operation ($F_{sampling} = 2 \times F_{input}$).

DEFINITION OF TERMS

Signal-to-noise ratio (SNR)

determined by FFT analysis,

$$SNR = 10.\log \left[\frac{P(F_{IN})}{P_n}\right] = 10.\log \left[\frac{A^2(F_{IN})}{\Sigma A^2(j)}\right]_{j \neq F_{in}}$$

with :

- $P(F_{IN})$ spectral power of the input frequency F_{IN},
- P_n noise power, which is defined as the sum of the powers of all spectral components, except F_{IN},
- A(f) amplitude of the spectral component of frequency f.

Total harmonic distorsion (THD)

determined by FFT analysis,

$$THD = 10.\log \left[\frac{P(F_{IN})}{P_{hn}}\right] = 10.\log \left[\frac{A^2(F_t)}{\Sigma A^2(k.F_t)}\right] \text{ with } k \geqslant 2$$

with : P_{hn} harmonic noise power, which is defined as the sum of the powers of all harmonics of F_T.

Number of effective bits (N_{eff})

determined by FFT analysis,

$$N_{eff} = \frac{SNR - 1.76}{6.02}$$

Gain error (G_e)

$$G_e = \frac{G - G_o}{G_o}$$

with :

- G_o slope of theoretical straight line of the ADC transfer function.
- G slope of the real best-fit straight line.

Integral nonlinearity (INL)

Measured after trimming the offset and gain errors to zero.

The integral nonlinearity for an output code i, INL (i), is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition.

The ADC integral nonlinearity INL is the maximum value of all [INL(i)].

Differential nonlinearity (DNL)

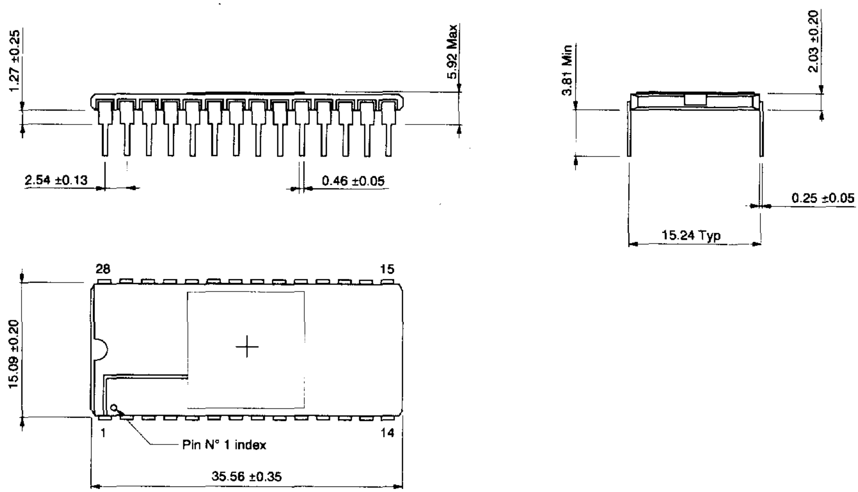
Measured after trimming the offset and gain errors to zero.

The differential nonlinearity for an output code i, DNL(i), is the difference between the measured step size of code i and the ideal LSB step size.

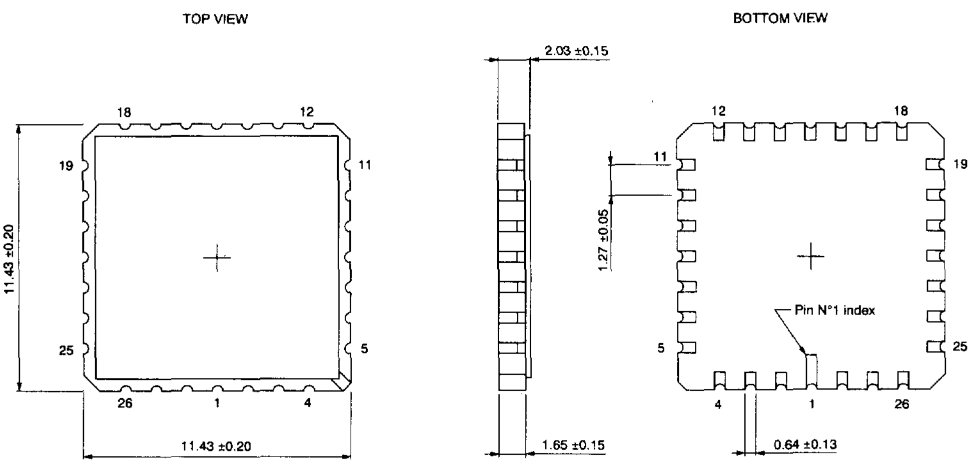
The ADC differential nonlinearity DNL is the maximum value of all [DNL(i)].

MECHANICAL PACKAGE DATA

DIL 28 - Ceramic package (Dimensions in mm)



LCCC 28 - Leadless Ceramic Chip Carrier package (Dimensions in mm)



DIE MECHANICAL INFORMATION : JTS 83048

Pad layout : V547

Pad size : 0.120 × 0.120 mm

Die size : 4.410 × 3.740 mm

Die thickness : 380 μm

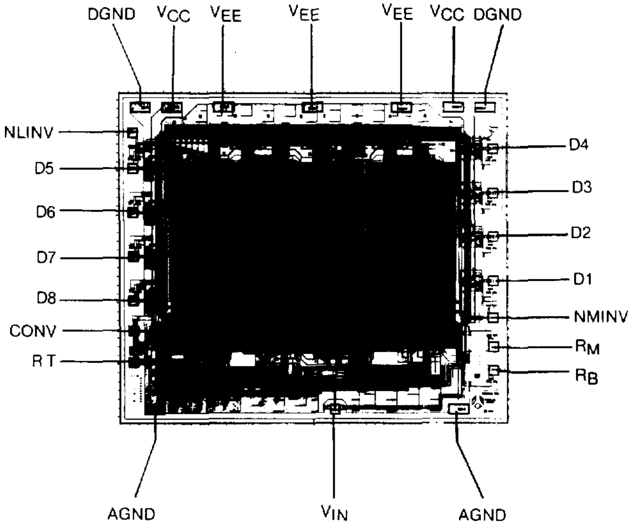
Metallization : Si (Back side)
Al-Si-Ti (Front side)

Passivation : Nitride

Revision : A

Qualification lot package : DIL 28

Back side potential : AV_{EE}



ORDERING INFORMATION

Package device

TS 83048 M C 8 B / C

- TS — TCS (1) prefix
- 83048 — Device or family
- M — Temperature range:
  - M : –55, +125°C
  - V : –40, +85°C
  - C : 0, +70°C
- C — Package:
  - C : DIL ceramic - 28 pins
  - E : LCC ceramic - 28 pins
- 8 — Lead finish:
  - 1 : Tin plated
  - 8 : Gold plated - Not available in B/C for LCC package
- B / C — Quality level:
  - - - : Standard
  - B/C : MIL-STD-883, class B
  - DESC/SMD : planned

Die form

J TS 83048 – 1 V A

- J — Die prefix
- TS — TCS prefix (1)
- 83048 — Generic part number
- 1 — Back side metallization:
  - 1 = Nacked Si
- V — Screening levels (2):
  - V : Visual inspection
- A — Revision of the mask set

Temperature range
_ : Tamb = 25°C

Note 1 : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.
Note 2 : For availability of the different available versions contact your TCS sale office.