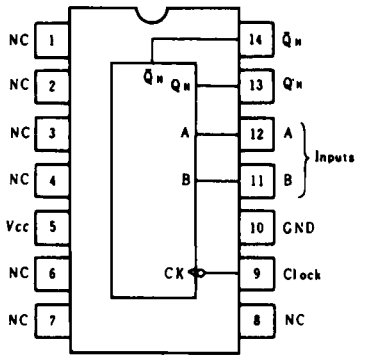
HD74HC91 ●8-bit Shift Register

This serial-in, serial-out, 8-bit shift register is composed of eight R-S master-slave flip-flops, input gating, and a clock drive. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

■ PIN ARRANGEMENT



(Top View)

■ FEATURES

- High Speed Operation: t_{pd}=21ns typ. (C_L=50pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: Vcc=2~6V
- Low Input Current: 1μA max.
- Low Quiescent Supply Current: Icc (static)=4μA max. (Ta=25°C)

■ FUNCTION TABLE

Inputs		Outputs	
t_n		t_{n+8}	
A	B	Q_H	$\bar{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

Notes) x:irrelevant
t_n:Reference bit time, clock low
t_{n+8}:Bit time after 8 low-to-high clock transitions

■ DC CHARACTERISTICS

Item	Symbol	V_{CC}(V)	Test Conditions		Ta=25℃ min	Ta=25℃ typ	Ta=25℃ max	Ta=−40~+85℃ min	Ta=−40~+85℃ max	Unit
Input Voltage	V_{IH}	2.0			1.5	—	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	
		6.0			4.2	—	—	4.2	—	
	V_{IL}	2.0			—	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	
Output Voltage	V_{OH}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OH}=−20μA	1.9	2.0	—	1.9	—	V
		4.5			4.4	4.5	—	4.4	—	
		6.0			5.9	6.0	—	5.9	—	
		4.5		I_{OH}=−4mA	4.18	—	—	4.13	—	
		6.0		I_{OH}=−5.2mA	5.68	—	—	5.63	—	
	V_{OL}	2.0	V_{in}=V_{IH} or V_{IL}	I_{OL}=20μA	—	0.0	0.1	—	0.1	V
		4.5			—	0.0	0.1	—	0.1	
		6.0			—	0.0	0.1	—	0.1	
		4.5		I_{OL}=4mA	—	—	0.26	—	0.33	
		6.0		I_{OL}=5.2mA	—	—	0.26	—	0.33	
Input Current	I_{in}	6.0	V_{in}=V_{CC} or GND		—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	6.0	V_{in}=V_{CC} or GND, I_{out}=0μA		—	—	4.0	—	40	μA

■ AC CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

Item	Symbol	V_{CC}(V)	Test Conditions	Ta=25℃ min	Ta=25℃ typ	Ta=25℃ max	Ta=−40~+85℃ min	Ta=−40~+85℃ max	Unit
Maximum Clock Frequency	f_{max}	2.0		—	—	5	—	4	MHz
		4.5		—	—	25	—	20	
		6.0		—	—	29	—	24	
Propagation Delay Time	t_{PLH}	2.0		—	—	210	—	265	ns
		4.5		—	21	42	—	53	
		6.0		—	—	36	—	45	
	t_{PHL}	2.0		—	—	210	—	265	ns
		4.5		—	21	42	—	53	
		6.0		—	—	36	—	45	
Pulse Width	t_w	2.0	Clock	125	—	—	156	—	ns
		4.5		25	9	—	31	—	
		6.0		21	—	—	26	—	
Set up Time	t_{su}	2.0		125	—	—	156	—	ns
		4.5		25	1	—	31	—	
		6.0		21	—	—	26	—	
Hold Time	t_h	2.0		5	—	—	5	—	ns
		4.5		5	−1	—	5	—	
		6.0		5	—	—	5	—	
Output Rise / Fall Time	t_{TLH} t_{THL}	2.0		—	—	75	—	95	ns
		4.5		—	5	15	—	19	
		6.0		—	—	13	—	16	
Input Capacitance	C_{in}	—		—	5	10	—	10	pF