

May 1991

## 16 Bit Numerically Controlled Oscillator

### Features

- 25.6MHz, 33MHz, 40MHz Versions
- 32-Bit Center and Offset Frequency Control
- 16-Bit Phase Control
- 8 Level PSK Supported Through Three Pin Interface
- Simultaneous 16 Bit Sine and Cosine Outputs
- Output in Two's Complement or Offset Binary
- <0.01Hz Tuning Resolution at 40MHz
- Serial or Parallel Outputs
- Spurious Frequency Components < -90dBc
- 16 Bit Microprocessor Compatible Control Interface
- 85 Pin PGA, 84 Pin PLCC

### Applications

- Direct Digital Synthesis
- Quadrature Signal Generation
- Modulation - FM, FSK, PSK (BPSK, QPSK, 8PSK)
- Precision Signal Generation

### Description

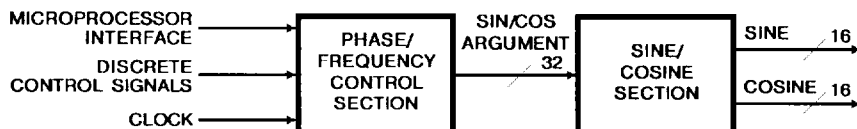
The Harris HSP45106 is a high performance 16-bit quadrature numerically controlled oscillator (NCO16). The NCO16 simplifies applications requiring frequency and phase agility such as frequency-hopped modems, PSK modems, spread spectrum communications, and precision signal generators. As shown in the block diagram, the HSP45106 is divided into a Phase/Frequency Control Section (PFCS) and a Sine/Cosine Section.

The inputs to the Phase/Frequency Control Section consist of a microprocessor interface and individual control lines. The frequency resolution is 32 bits, which provides for resolution of better than 0.01Hz at 40MHz. User programmable center frequency and offset frequency registers give the user the capability to perform phase coherent switching between two sinusoids of different frequencies. Further, a programmable phase control register allows for phase control of better than 0.006°. In applications requiring up to 8-level PSK, three discrete inputs are provided to simplify implementation.

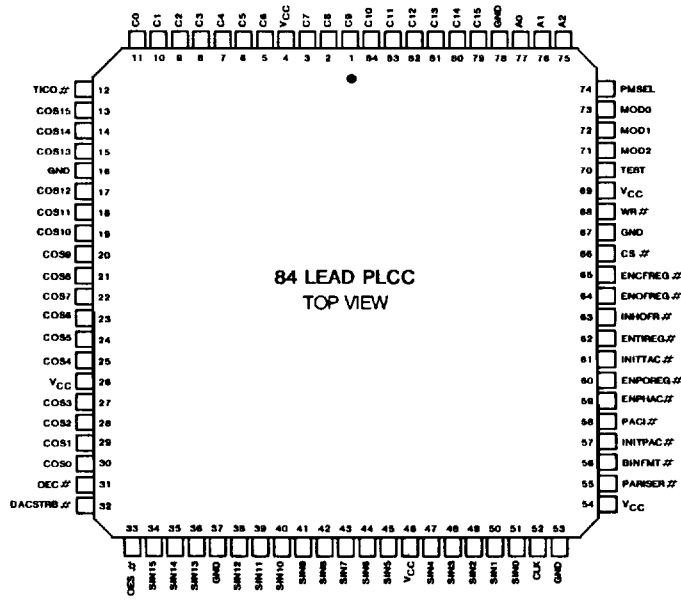
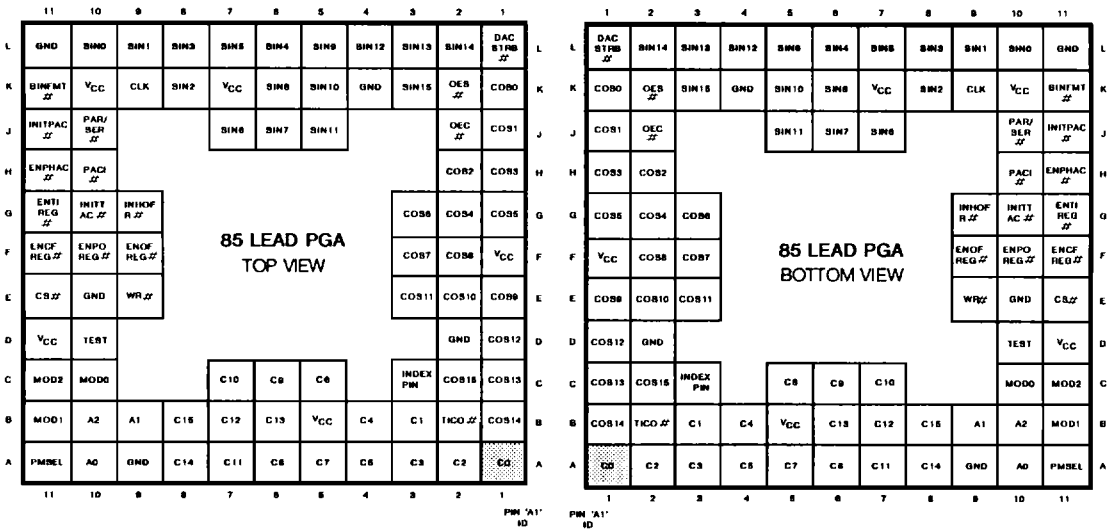
The output of the PFCS is a 32-bit phase which is input to the Sine/Cosine Section for conversion into sinusoidal amplitude. The outputs of the sine/cosine section are two 16-bit quadrature signals. The spurious free dynamic range of this complex vector is greater than 90dBc.

For added flexibility when using the NCO16 in conjunction with DAC's, a choice of either parallel or serial outputs with either two's complement or offset binary encoding is provided. In addition, a synchronization signal is available which signals serial word boundaries.

### Block Diagram



Pinouts



**Pin Description**

NAME	PGA PIN NUMBER	TYPE	DESCRIPTION
VCC	B5, D11, F1, K7, K10		+5 power supply pin.
GND	A9, D2, E10, K4, L11		Ground
CO-15	A1-8, B3-4 B6-8, C5-7	I	Control input bus for loading phase, frequency, and timer data into the PFCS. C0 is LSB.
A0-2	A10, B9-10	I	Address pins for selecting destination of CO-15 data (Table 2).
CS#	E11	I	Chip select (Active low). Enables data to be written into control registers by WR#.
WR#	E9	I	Write enable (Active low). Data is clocked into the register selected by A0-2 on the rising edge of WR# when CS# is low.
CLK	K9	I	Clock. All registers, except the control registers clocked with WR#, are clocked (when enabled) by the rising edge of CLK.
ENPOREG#	F10	I	Phase Offset Register Enable (Active low). Registered on chip by CLK. When active, after being clocked onto chip, ENPOREG# enables the clocking of data into the Phase Offset Register. Allows ROM address to be updated regardless of ENPHAC#.
ENOFREG#	F9	I	Offset Frequency Register Enable (Active low). Registered on chip by CLK. When active, after being clocked onto chip, ENOFREG# enables the clocking of data into the Offset Frequency Register.
ENCFREG#	F11	I	Center Frequency Register Enable (Active low). Registered on chip by CLK. When active, after being clocked onto chip, ENCFREG# enables the clocking of data into the Center Frequency Register.
ENPHAC#	H11	I	Phase Accumulator Register Enable (Active low). Registered on chip by CLK. When active, after being clocked onto chip, ENPHAC# enables the clocking of data into the Phase Accumulator Register.
ENTIREG#	G11	I	Timer Increment Register Enable (Active low). Registered on chip by CLK. When active, after being clocked onto chip, ENTIREG# enables the clocking of data into the Timer Increment Register.
INHOFR#	G9	I	Inhibit Offset Frequency Register Output (active low). Registered on chip by CLK. When active, after being clocked onto chip, INHOFR# zeroes the data path from the Offset Frequency Register to the Frequency Adder. New data can be still clocked into the Offset Frequency Register. INHOFR# does not affect the contents of the register.
INITPAC#	J11	I	Initialize Phase Accumulator (Active low). Registered on chip by CLK. Zeroes the feedback path in the Phase Accumulator. Does not clear the Phase Accumulator Register.
MOD0-2	B11, C10-11	I	Modulation Control Inputs. When selected with the PMSEL line, these bits add an offset of 0, 45, 90, 135, 180, 225, 270, or 315 degrees to the current phase (i.e., modulate the output). The lower 13 bits of the phase control are set to zero. These bits are registered when the Phase Offset Register is enabled.
PMSEL	A11	I	Phase Modulation Select input. Registered on chip by CLK. This input determines the source of the data clocked into the Phase Offset Register. When high, the Phase Input Register is selected. When low, the external modulation pins (MOD0-2) control the three most significant bits of the Phase Offset Register and the 13 least significant bits are set to zero.
PACI#	H10	I	Phase Accumulator Carry Input (Active low). Registered on chip by CLK.
INITTAC#	G10	I	Initialize Timer Accumulator (Active low). This input is registered on chip by CLK. When active, after being clocked onto chip, INITTAC# enables the clocking of data into the Timer increment Register, and also zeroes the feedback path in the Timer Accumulator.
TEST	D10	I	Test select input. Registered on chip by CLK. This input is active high. When active, this input enables test busses to the outputs instead of the sine and cosine data.
PAR/SER#	J10	I	Parallel/Serial Output Select. This input is registered on chip by CLK. When low, the sine and cosine outputs are in serial mode. The output shift registers will load in new data after ENPHAC# goes low and will start shifting the data out after ENPHAC# goes high. When this input is high, the output registers are loaded every clock and no shifting takes place.
BINFMT#	K11	I	Format. This input is registered on chip by CLK. When low, the MSB of the SIN and COS are inverted to form an offset binary (unsigned) number.
OES#	K2	I	Three-state control for bits SIN0-15. Outputs are enabled when OES# is low.
OEC#	J2	I	Three-state control for bits COS0-15. Outputs are enabled when OEC# is low.
TICO#	B2	O	Timer Accumulator Carry Output. Active low, registered. This output goes low when a carry is generated by the Timer Accumulator.

**Pin Description** (Continued)

NAME	PGA PIN NUMBER	TYPE	DESCRIPTION
DACSTRB#	L1	O	DAC Strobe (Active low). In serial mode, this output will go low when the first bit of a new output word is valid at the shift register output.
SINO-15	J5-7, K3, K5-6, K8, L2-10	O	Sine output data. When parallel mode is enabled, data is output on SINO-15. When serial mode is enabled, output data bits are shifted out of SIN15 and SINO. The bit stream on SIN 15 is provided MSB first while the bit stream on SINO is provided LSB first.
COSO-15	B1, C1-2, D1, E1-3, F2-3, G1-3, H1-2, J1, K1	O	Cosine output data. When parallel mode is enabled, data is output on COSO-15. When serial mode is enabled, output data bits are shifted out of COS15 and COS0. The bit stream on COS15 is provided LSB first.
Index Pin	C3		Used to align chip in socket or on circuit board. Must be left as a no connect in circuit.

**Functional Description**

The 16-bit Numerically Controlled Oscillator (NCO16) produces a digital complex sinusoid waveform whose frequency and phase are controlled through a standard microprocessor interface and discrete inputs. The NCO16 generates 16-bit sine and cosine vectors at a maximum sample rate of 40MHz. The NCO16 can be preprogrammed to produce a constant (CW) sine and cosine output for Direct Digital Synthesis (DDS) applications. Alternatively, the phase and frequency inputs can be updated in real time to produce a FM, PSK, FSK, or MSK modulated waveform. To simplify PSK generation, a 3 pin interface is provided to support modulation of up to 8 levels.

As shown in the Block Diagram, the NCO16 is comprised of a Phase and Frequency Control Section (PFCS) and Sine/Cosine Section. The PFCS stores the phase and frequency control inputs and uses them to calculate the phase angle of a rotating complex vector. The Sine/Cosine Section performs a lookup on this phase and generates the appropriate amplitude values for the sine and cosine. These quadrature outputs may be configured as serial or parallel with either two's complement or offset binary format.

**Phase/Frequency Control Section**

The phase and frequency of the quadrature outputs are controlled by the PFCS (Figure 1). The PFCS generates a 32 bit word which represents the instantaneous phase (Sin/Cos argument) of the sine and cosine waves being generated. This phase is incremented on the rising edge of each CLK by the preprogrammed amounts in the phase and frequency control registers. As the instantaneous phase steps from 0 through full scale ( $2^{32} - 1$ ), the phase of the quadrature outputs proceeds from  $0^\circ$  around the unit circle counter clockwise.

The PFCS is comprised of a Phase Accumulator Section, Phase Offset adder, Input Section, and a Timer Accumulator Section. The Phase Accumulator computes the instantaneous phase angle from user programmed values in the Center and Offset Frequency Registers. This angle is then fed into the Phase Offset adder where it is offset by the preprogrammed value in the Phase Offset Register. The Input Section routes data from a microprocessor compatible control bus and discrete input signals into the appropriate configuration registers. The Timer Accumulator

supplies a pulse to mark the passage of a user programmed period of time.

**Input Section**

The Input Section loads the data on CO-15 into one of the seven input registers, the LSB and MSB Center Frequency Input Registers, the LSB and MSB Offset Frequency Registers, the LSB and MSB Timer Input Registers, and the Phase Input Register. The destination depends on the state of A0-2 when CS# and WR# are low (Table 1).

TABLE 1

A2-0 DECODING					FUNCTION
A2	A1	A0	CS#	WR#	
0	0	0	0	↑	Load least significant bits of Center Frequency input.
0	0	1	0	↑	Load most significant bits of Center Frequency input.
0	1	0	0	↑	Load least significant bits of Offset Frequency input.
0	1	1	0	↑	Load most significant bits of Offset Frequency input.
1	0	0	0	↑	Load least significant bits of Timing Interval input.
1	0	1	0	↑	Load most significant bits of Timing Interval input.
1	1	0	0	↑	Load Phase Register
1	1	1	0	↑	Reserved
X	X	X	1	X	Input Disabled

Once the input registers have been loaded, the control inputs ENCFREG#, ENOFREG#, ENTIREG#, ENCTIREG#, and ENPOREG# will allow the input registers to be downloaded to the PFCS control registers with the input CLK. The control inputs are latched on the rising edge of CLK and the control registers are updated on the rising edge of the following CLK. For example, to load the Center Frequency Register, the data is loaded into the LSB and MSB Center Frequency Input Register, and ENCFREG# is set to zero; the next rising edge of CLK will pass the registered version of ENCFREG#, R.ENCFREG#, to the

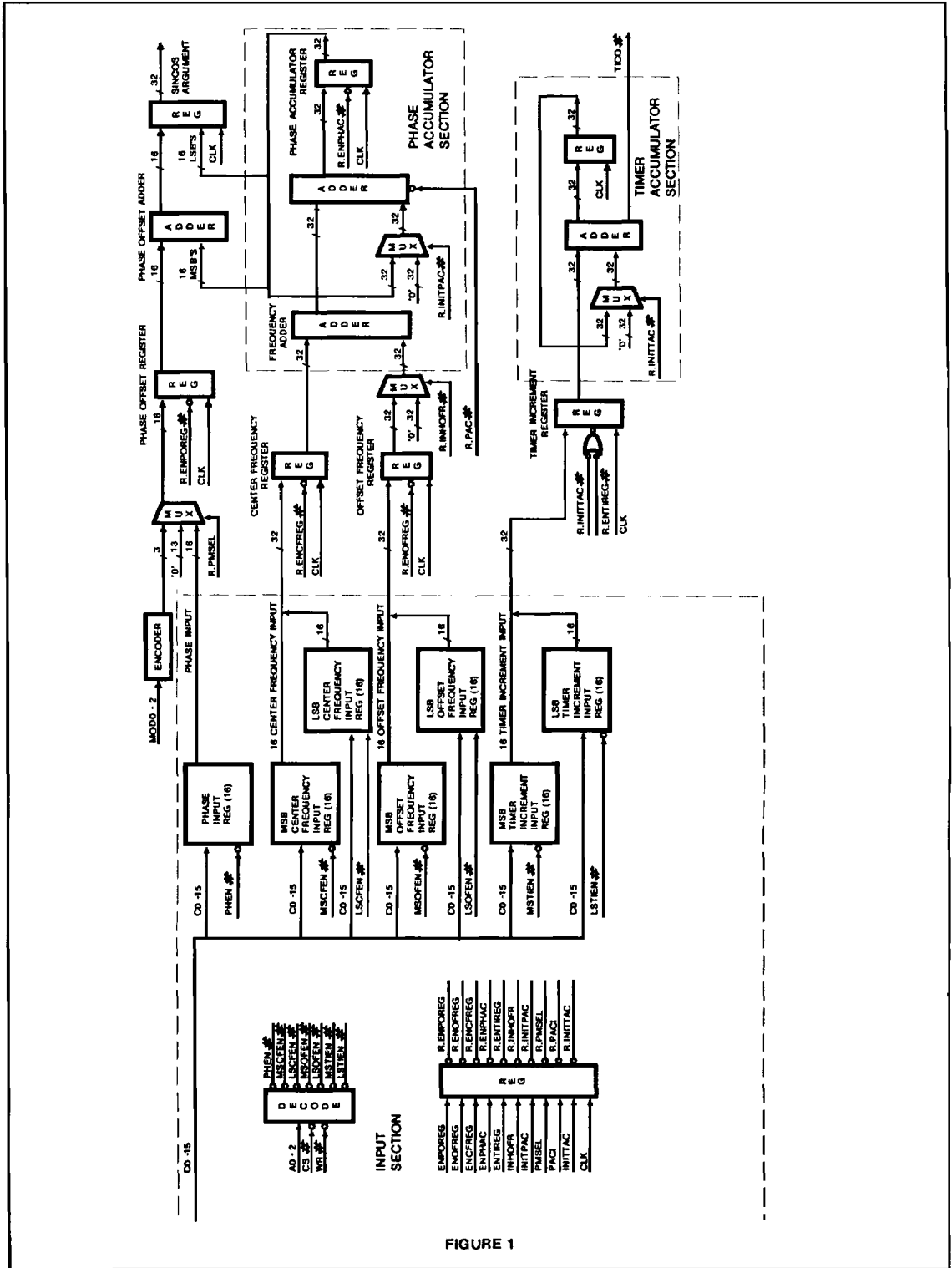


FIGURE 1

clock enable of the Center Frequency Register; this register then gets loaded on the following rising edge of CLK. The contents of the input registers are downloaded to the control registers every clock if the control inputs are enabled.

#### Phase Accumulator Section

The Phase Accumulator adds the 32 bit output of the Frequency Adder with the contents of a 32 bit Phase Accumulator Register on every clock cycle. When the sum causes the adder to overflow, the accumulation continues with the least significant 32 bits of the result.

Initializing the Phase Accumulator Register is done by putting a low on the INITPAC# and ENPHAC# lines. This zeroes the feedback path to the accumulator, so that the register is loaded with the current value of the Frequency Adder on the next clock.

The frequency of the quadrature outputs is based on the number of clock cycles required to step from 0 to full scale. The number of steps required for this transition depends on the phase increment calculated by the frequency adder. For example, if the Center and Offset Frequency registers are programmed such that the output of the Frequency Adder is 4000 0000 hex, the Phase Accumulator will step the phase from 0 to 360 degrees every 4 clock cycles. Thus, for a 30 MHz CLK, the quadrature outputs will have a frequency of 30/4 MHz or 7.5MHz. In general, the frequency of the quadrature output is determined by  $N \times FCLK/2^{32}$ , where N is the output of the Frequency Adder and FCLK is the frequency of CLK.

The Frequency Adder sums the contents of both the Center and Offset Frequency Registers to produce a phase increment. By enabling INHOFR#, the output of the Offset Frequency Register is disabled so that the output frequency is determined from the Center Frequency Register alone. For BPSK modems, INHOFR# can be asserted/de-asserted to toggle the quadrature outputs between two programmed frequencies. Note: enabling/disabling INHOFR# preserves the contents of the Offset Frequency Register.

#### Phase Offset Adder

The output of the Phase Accumulator goes to the Phase Offset Adder, which adds the 16 bit contents of the Phase Offset Register to the 16 MSB's of the phase. The resulting 32-bit number forms the instantaneous phase which is fed to the Sine/Cosine Section.

The user has the option of loading the Phase Offset Registers with the contents of the Phase Input Register or the MOD0-2 inputs depending on the state of PMSEL. When PMSEL is high, the contents of the Phase Input Register are loaded. If PMSEL is low, MOD0-2 encode the upper 3 bits of the Phase Offset Register while the lower 13 bits are cleared. The MOD0-2 inputs simplify PSK modulation by providing a 3 input interface to phase modulate the carrier as shown in Table 2. The control input ENPOREG# acts as a clock enable and must be low to enable clocking of data into the Phase Offset Register.

TABLE 2

MOD2-0 DECODING			
MOD2	MOD1	MOD0	PHASE SHIFT (DEGREES)
0	0	0	0
0	0	1	45
0	1	0	90
0	1	1	135
1	0	0	270
1	0	1	315
1	1	0	180
1	1	1	225

#### Timer Accumulator Section

The Timer Accumulator consists of a register which is incremented on every clock. The amount by which it increments is loaded into the Timer Increment Input Registers and is latched into the Timer Increment Register on rising edges of CLK while ENTIREG# is low. The output of the Timer Accumulator is the accumulator carry out, TICO#. TICO# can be used as a timer to enable the periodic sampling of the output of the NCO-16. The number programmed into this register equals  $(2^{32} \times \text{CLK period}) / (\text{desired time interval})$ .

#### Sine/Cosine Section

The Sine/Cosine Section (Figure 2) converts the instantaneous phase from the PFCS Section into the appropriate amplitude values for the sine and cosine outputs. It takes the most significant 20 bits of the PFCS output and passes them through a Sine/Cosine look up to form the 16 bit quadrature outputs. The sine and cosine values are computed to reduce the amount of ROM needed. The magnitude of the error in the computed value of the complex vector is less than -90.2dB. The error in the sine or cosine alone is approximately 2dB better. The 20 bit phase word maps into  $2\pi$  radians so that the angular resolution is  $(2\pi)/2^{20}$ . An address of zero corresponds to 0 radians and an address of hex FFFF corresponds to  $2\pi - ((2\pi)/2^{20})$  radians. The outputs of the Sine/Cosine Section are two's complement sine and cosine values. The ROM contents have been scaled by  $(2^{16}-1)/(2^{16}+1)$  for symmetry about zero.

To simplify interfacing with D/A converters, the format of the sine/cosine outputs may be changed to offset binary by enabling BINFMT#. When BINFMT# is enabled, The MSB of the Sine and Cosine outputs (SIN15 and COS15 when the outputs are in parallel mode) are inverted. Depending upon the state of BINFMT#, the output is centered around midscale and ranges from 8001H to 7FFFH (two's complement mode) or 0001H to FFFFH (offset binary mode).

Serial output mode may be chosen by enabling PAR/SER#. In this mode the user loads the output shift registers with Sine/Cosine ROM output by enabling ENPHAC#. After ENPHAC# goes inactive the data is shifted out serially. For

example, to clock out one 16 bit sine/cosine output, ENPHAC# would be active for one cycle to load the output shift register, and would then go inactive for the following 15 cycles to clock the remaining bits out. Output bit streams are provided in formats with either MSB first or LSB first. The MSB first format is available on the SIN15 and COS15 output pins. The LSB first format is available on the SINO and COS0 output pins. In MSB first format, zero's follow the LSB if a new output word is not loaded into the shift register. In LSB first format, the sine extension bit follows the MSB if

a new data word is not loaded. The output signal DACSTRB# is provided to signal the first bit of a new output word is valid (Figure 3). Note: all unused pins of SINO-15 and COS0-15 should be left floating.

A test mode is supplied which enables the user to access the phase input to the Sine/Cosine ROM. If TEST and PAR/SER# are both high, the 28 MSB's of the phase input to the Sine/Cosine Section are made available on SINO-15 and COS4-15. The SINO-15 outputs represent the MSW of the address.

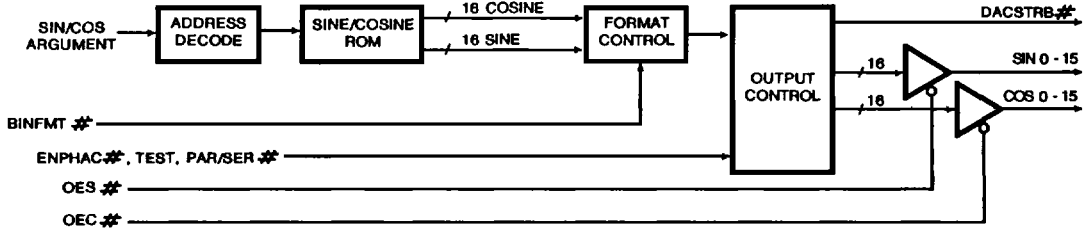


FIGURE 2. SINE/COSINE BLOCK DIAGRAM

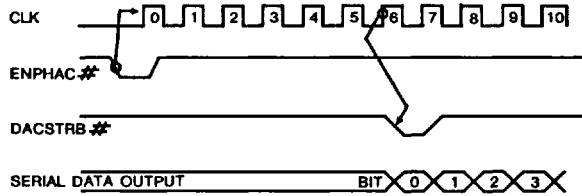


FIGURE 3. SERIAL OUTPUT I/O TIMING DIAGRAM

# Specifications HSP45106

## Absolute Maximum Ratings

Supply Voltage .....	+8.0V
Input, Output or I/O Voltage Applied .....	GND -0.5V to $V_{CC} + 0.5V$
Storage Temperature Range .....	-65°C to +150°C
Maximum Package Power Dissipation .....	2.16W
$\theta_{jc}$ .....	8.3°C/W
$\theta_{ja}$ .....	23.1°C/W
Component Count .....	103,000 Transistors
Junction Temperature .....	+175°C
Lead Temperature (Soldering, Ten Seconds) .....	+300°C
ESD Classification .....	Class 1

*CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Operating Conditions

Operating Voltage Range .....	+4.75V to +5.25V
Operating Temperature Range .....	0°C to +70°C

## D.C. Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
$V_{IH}$	Logical One Input Voltage	2.0	-	V	$V_{CC} = 5.25V$
$V_{IL}$	Logical Zero Input Voltage	-	0.8	V	$V_{CC} = 4.75V$
$V_{IHC}$	High Level Clock Input	3.0	-	V	$V_{CC} = 5.25V$
$V_{ILC}$	Low Level Clock Input	-	0.8	V	$V_{CC} = 4.75V$
$V_{OH}$	Output HIGH Voltage	2.6	-	V	$I_{OH} = -400\mu A, V_{CC} = 4.75V$
$V_{OL}$	Output LOW Voltage	-	0.4	V	$I_{OL} = +2.0mA, V_{CC} = 4.75V$
$I_I$	Input Leakage Current	-10	10	$\mu A$	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$
$I_O$	I/O Leakage Current	-10	10	$\mu A$	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 5.25V$
$I_{CCSB}$	Standby Power Supply Current	-	500	$\mu A$	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$ , Note 3
$I_{CCOP}$	Operating Power Supply Current	-	256	mA	$f = 25.6MHz, V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.25V$ , Notes 1 and 3

## Capacitance ( $T_A = +25^\circ C$ , Note 2)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
$C_{IN}$	Input Capacitance	-	10	pF	FREQ = 1MHz, $V_{CC} =$ Open, All measurements are referenced to device ground
$C_O$	Output Capacitance	-	10	pF	

### NOTES:

- Power supply current is proportional to operating frequency. Typical rating for  $I_{CCOP}$  is 10mA/MHz.
- Not tested, but characterized at initial design and at major process/design changes.
- Output load per test load circuit with switch open and  $C_L = 40pF$ .

5  
SIGNAL SYNTHESIZERS

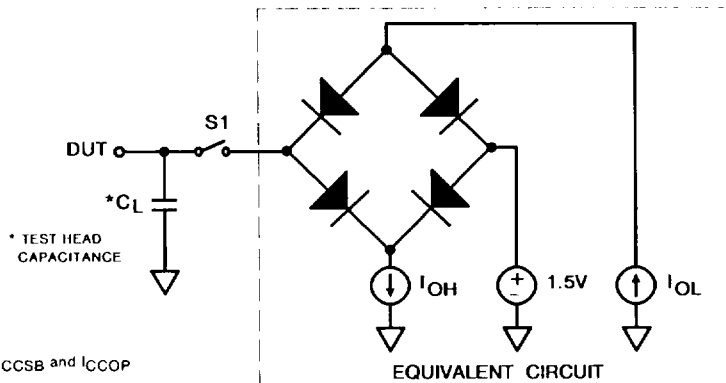
**A.C. Electrical Specifications** (Note 1)

SYMBOL	PARAMETER	25.6MHz		33MHz		40MHz		COMMENTS
		MIN	MAX	MIN	MAX	MIN	MAX	
T <sub>CP</sub>	CLK Period	39	-	30	-	25	-	ns
T <sub>CH</sub>	CLK High	15	-	12	-	10	-	ns
T <sub>CL</sub>	CLK Low	15	-	12	-	10	-	ns
T <sub>WP</sub>	WR# Period	39	-	30	-	25	-	ns
T <sub>WH</sub>	WR# High	15	-	12	-	10	-	ns
T <sub>WL</sub>	WR# Low	15	-	12	-	10	-	ns
T <sub>AWS</sub>	Set-up Time A0-2, CS# to WR# going high	13	-	13	-	12	-	ns
T <sub>AWH</sub>	Hold Time A0-2, CS# from WR# going high	1	-	1	-	1	-	ns
T <sub>CWS</sub>	Set-up Time C0-15 to WR# going high	15	-	15	-	12	-	ns
T <sub>CWH</sub>	Hold Time C0-15 from WR# going high	0	-	0	-	0	-	ns
T <sub>WC</sub>	Set-up time WR# high to CLK high	16	-	12	-	10	-	ns, Note 2
T <sub>MCS</sub>	Set-up Time MOD0-2 to CLK going high	15	-	15	-	12	-	ns
T <sub>MCH</sub>	Hold Time MOD0-2 from CLK going high	0	-	0	-	0	-	ns
T <sub>ECS</sub>	Set-up Time ENPOREG#, ENOFREG#, ENCFREG#, ENPHAC#, ENTIREG#, INHOFR#, PMSEL#, INITPAC#, BINFMT#, TEST, PAR/SER#, PACI#, INITTAC# to CLK going high	12	-	12	-	12	-	ns
T <sub>ECH</sub>	Hold Time ENPOREG#, ENOFREG#, ENCFREG#, ENPHAC#, ENTIREG#, INHOFR#, PMSEL#, INITPAC#, BINFMT#, TEST, PAR/SER#, PACI#, INITTAC# from CLK going high	0	-	0	-	0	-	ns
T <sub>DO</sub>	CLK to Output Delay SIN0-15, COS0-15, TICO#	-	18	-	15	-	13	ns
T <sub>DSO</sub>	CLK to Output Delay DACSTRB#	2	18	2	15	2	13	ns
T <sub>OE</sub>	Output Enable Time	-	12	-	12	-	12	ns
T <sub>OD</sub>	Output Disable Time	-	15	-	15	-	13	ns, Note 3
T <sub>RF</sub>	Output rise, fall time	-	8	-	8	-	8	ns, Note 3

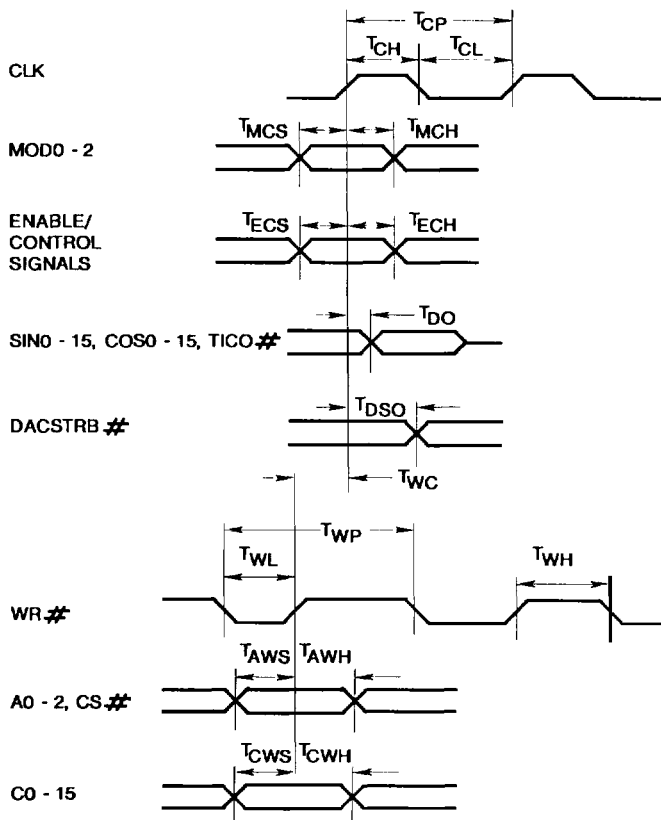
NOTES:

1. A.C. testing is performed as follows: Input levels (CLK Input) 4.0V and 0V; Input levels (all other inputs) 0V and 3.0V; Timing reference levels (CLK) 2.0V; All others 1.5V. Input rise and fall times driven at 1ns/V. Output load per test load circuit with switch closed and C<sub>L</sub> = 40 pF. Output transition is measured at V<sub>OH</sub> ≥ 1.5V and V<sub>OL</sub> ≤ 1.5V.
2. If ENOFREG#, ENCFREG#, ENTIREG#, OR ENPOREG# are active, care must be taken to not violate set-up and hold times to these registers when writing data into the chip via the C0-15 port.
3. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

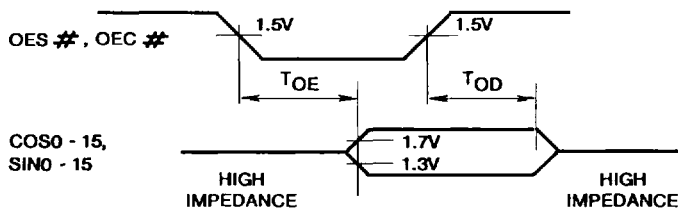
**A.C. Test Load Circuit**



Waveforms



OUTPUT ENABLE, DISABLE TIMING



OUTPUT RISE AND FALL TIMES

