



PJL9602

30V Complementary Enhancement Mode MOSFET

Voltage 30 / -30V **Current** 6.1 / -6.0A

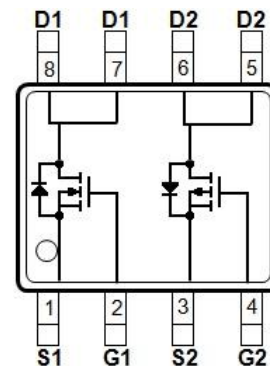
Features

- Advanced Trench Process Technology
- Low Gate Charge
- Low reverse transfer capacitance
- Lead free in compliance with EU RoHS 2.0
- Green molding compound as per IEC 61249 standard

Mechanical Data

- Case: SOP-8 Package
- Terminals: Solderable per MIL-STD-750, Method 2026
- Approx. Weight: 0.0029 ounces, 0.083 grams

SOP-8



Maximum Ratings and Thermal Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER		SYMBOL	N-CH LIMIT	P-CH LIMIT	UNITS
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	± 20	± 20	V
Continuous Drain Current	$T_a=25^\circ\text{C}$	I_D	6.1	-6.0	A
	$T_a=70^\circ\text{C}$	I_D	4.9	-4.7	A
Pulsed Drain Current (Note 4)		I_{DM}	24.4	-24	A
Power Dissipation	$T_a=25^\circ\text{C}$	P_D	1.7		W
	$T_a=70^\circ\text{C}$		1.1		
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150		$^\circ\text{C}$
Thermal resistance - Junction to Ambient (Note 3)		$R_{\theta JA}$	73.5		$^\circ\text{C/W}$



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N-Channel Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.3	2.1	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=6.0A$	-	23	28	m Ω
		$V_{GS}=4.5V, I_D=3.0A$	-	36	43	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=6A,$ $V_{GS}=10V$ (Note 3)	-	7.8	-	nC
Gate-Source Charge	Q_{gs}		-	1.2	-	
Gate-Drain Charge	Q_{gd}		-	1.5	-	
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V,$ $f=1.0\text{MHz}$	-	343	-	pF
Output Capacitance	C_{oss}		-	48	-	
Reverse Transfer Capacitance	C_{rss}		-	34	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=15V, I_D=6A,$ $V_{GS}=10V, R_G=3\Omega$ (Note 3)	-	3	-	ns
Turn-On Rise Time	t_r		-	40	-	
Turn-Off Delay Time	$t_{d(off)}$		-	38	-	
Turn-Off Fall Time	t_f		-	39	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	6.1	A
Diode Forward Voltage	V_{SD}	$I_S=1.0A, V_{GS}=0V$	-	0.78	1.2	V



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P-Channel Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNITS
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=-250\mu A$	-30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.6	-2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-4A$	-	26	30	m Ω
		$V_{GS}=-4.5V, I_D=-2A$	-	36	45	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-30V, V_{GS}=0V$	-	-	-1.0	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-15V, I_D=-5A,$ $V_{GS}=-4.5V$ (Note 1,2)	-	7.8	-	nC
Gate-Source Charge	Q_{gs}		-	2.7	-	
Gate-Drain Charge	Q_{gd}		-	2.8	-	
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V,$ $f=1.0\text{MHZ}$	-	870	-	pF
Output Capacitance	C_{oss}		-	130	-	
Reverse Transfer Capacitance	C_{rss}		-	93	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DS}=-15V, I_D=-1A,$ $V_{GS}=-10V, R_G=6\Omega$ (Note 1,2)	-	6.5	-	ns
Turn-On Rise Time	t_r		-	8.8	-	
Turn-Off Delay Time	$t_{d(off)}$		-	73	-	
Turn-Off Fall Time	t_f		-	44	-	
Drain-Source Diode						
Maximum Continuous Drain-Source Diode Forward Current	I_S	---	-	-	-6.2	A
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$	-	-0.75	-1.0	V

NOTES :

1. Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature typical characteristics.
3. The maximum current rating is package limited.
4. Repetitive rating, pulse width limited by junction temperature $T_J(\text{MAX})=150^{\circ}\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^{\circ}\text{C}$.
5. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. Mounted on a 1 inch² with 2oz.square pad of copper.
6. Guaranteed by design, not subject to production testing.



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N-CH TYPICAL CHARACTERISTIC CURVES

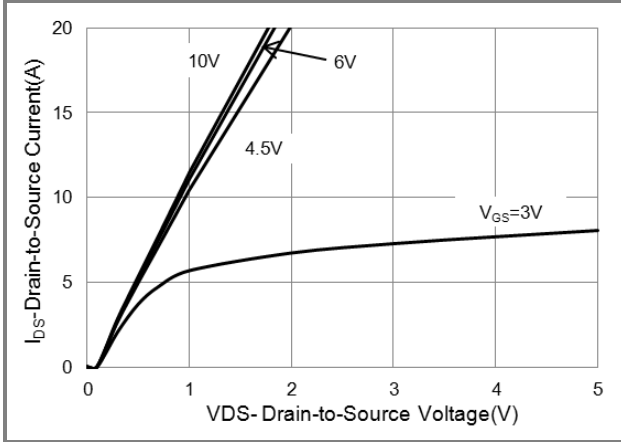


Fig.1 On-Region Characteristics

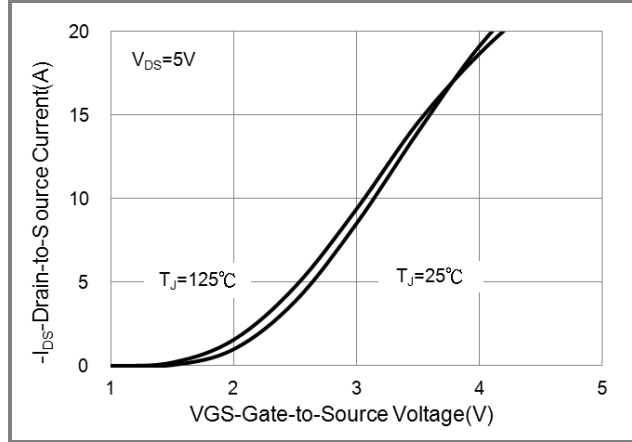


Fig.2 Transfer Characteristics

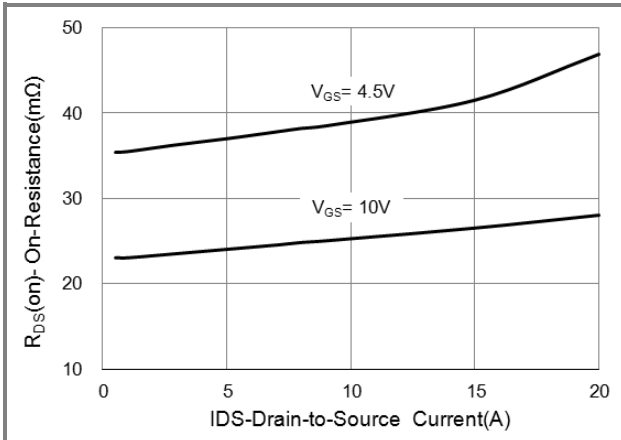


Fig.3 On-Resistance vs. Drain Current

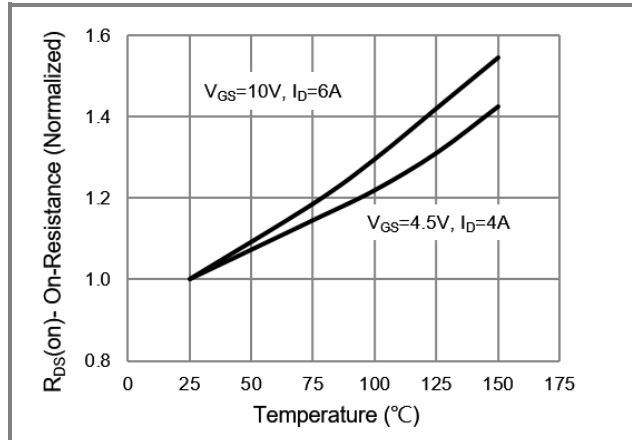


Fig.4 On-Resistance vs. Junction temperature

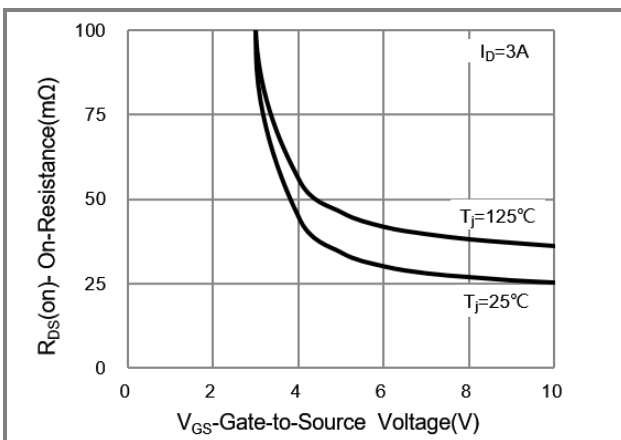


Fig.5 On-Resistance Variation with VGS.

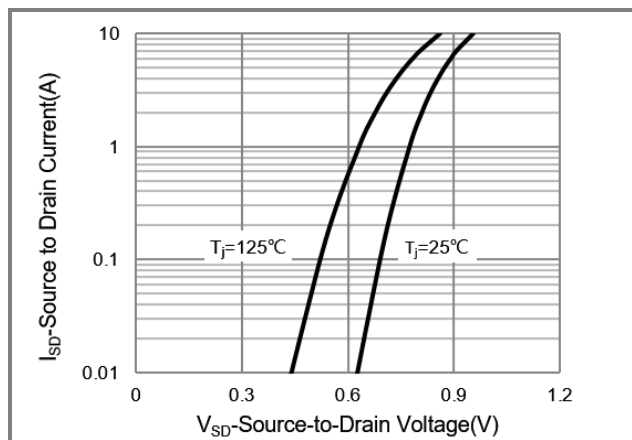


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

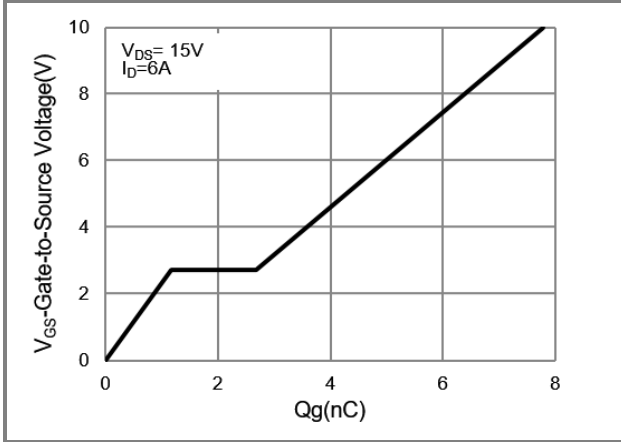


Fig.7 Gate-Charge Characteristics

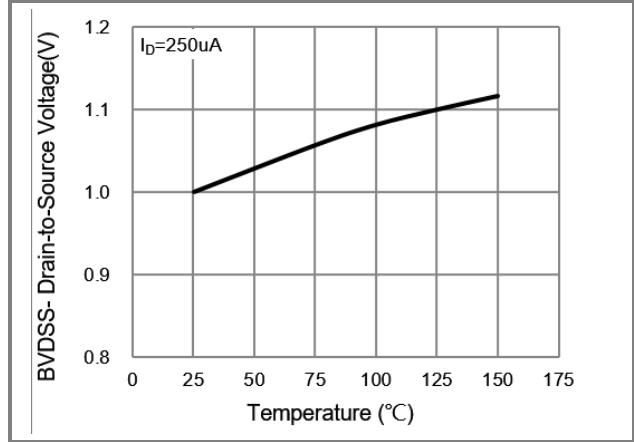


Fig.8 Breakdown Voltage Variation vs. Temperature

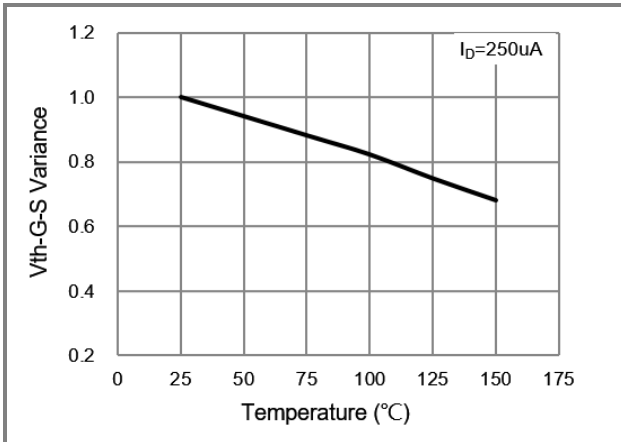


Fig.9 Threshold Voltage Variation with Temperature.

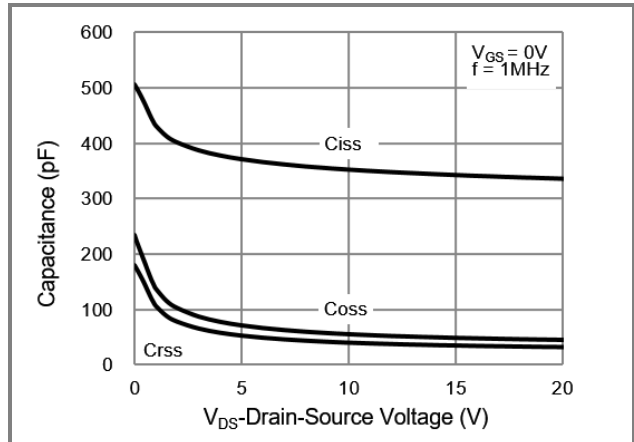


Fig.10 Capacitance vs. Drain-Source Voltage.



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P-CH TYPICAL CHARACTERISTIC CURVES

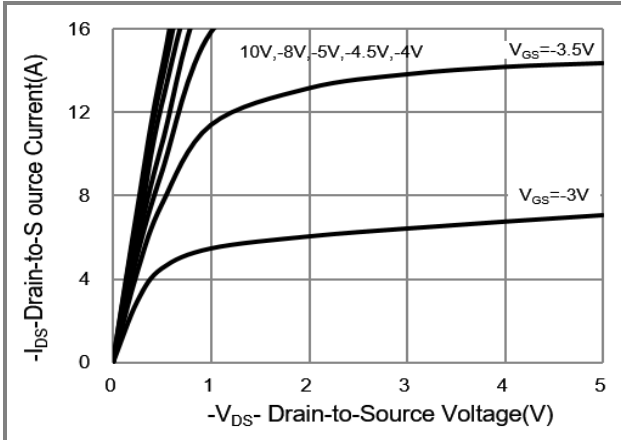


Fig.1 On-Region Characteristics

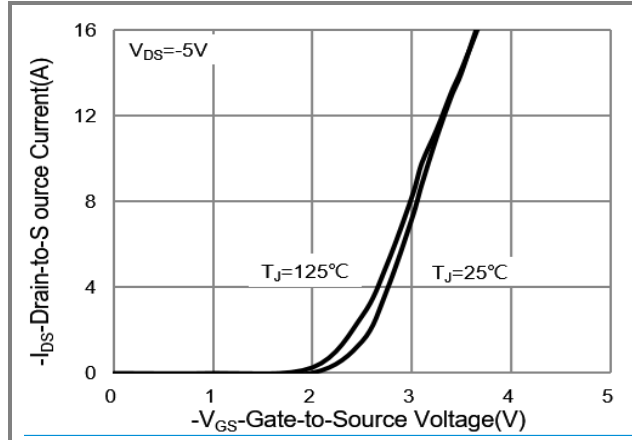


Fig.2 Transfer Characteristics

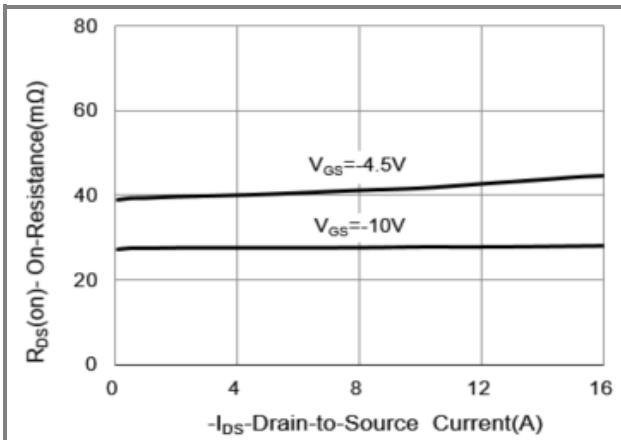


Fig.3 On-Resistance vs. Drain Current

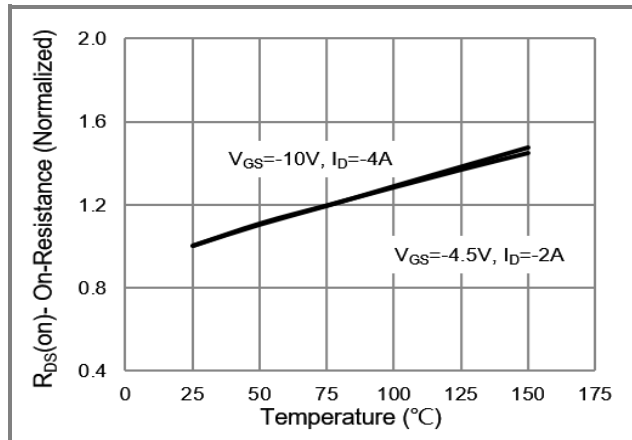


Fig.4 On-Resistance vs. Junction temperature

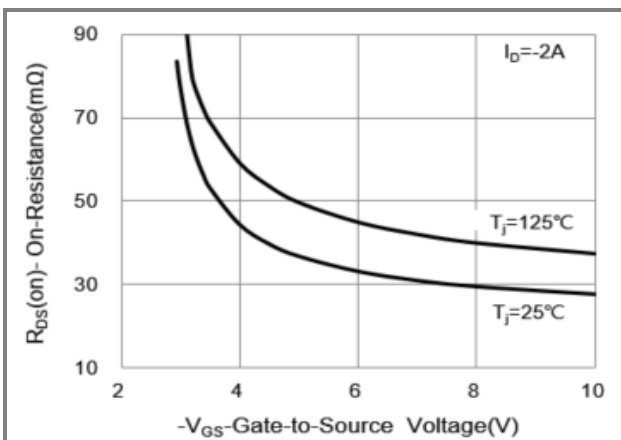


Fig.5 On-Resistance Variation with V_GS.

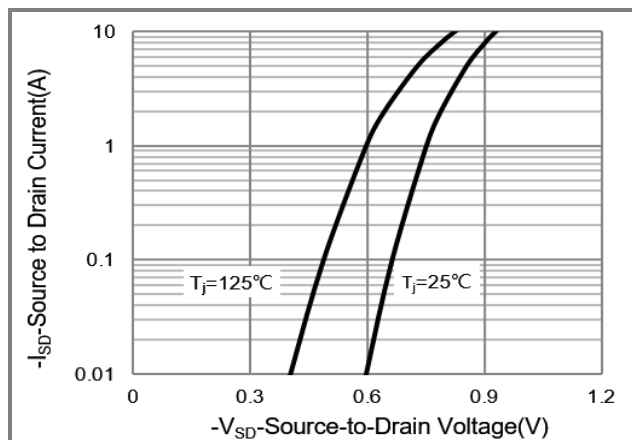


Fig.6 Body Diode Characteristics



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TYPICAL CHARACTERISTIC CURVES

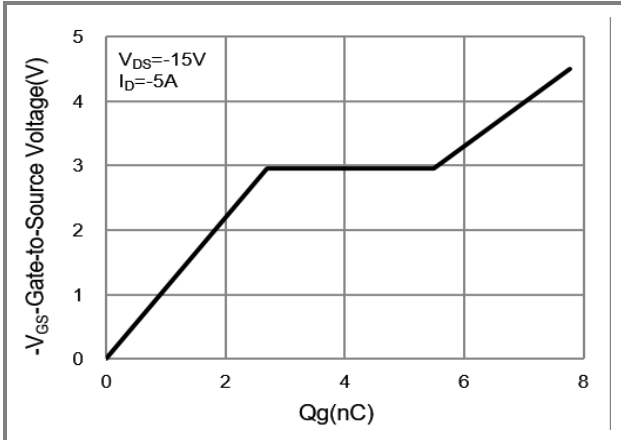


Fig.7 Gate-Charge Characteristics

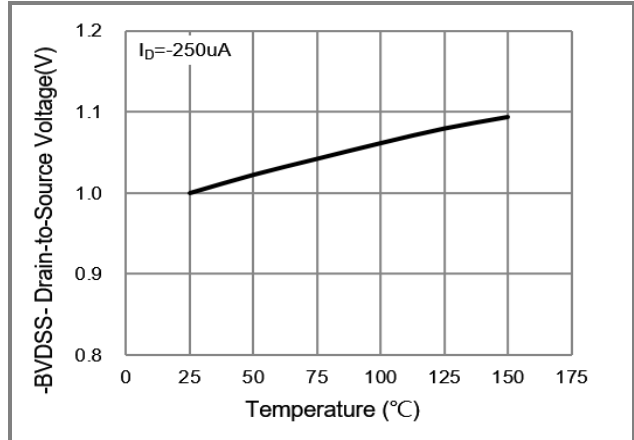


Fig.8 Threshold Voltage Variation with Temperature

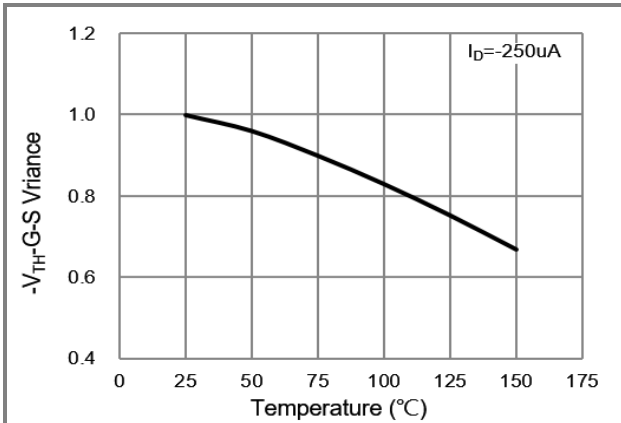


Fig.9 Threshold Voltage Variation with Temperature.

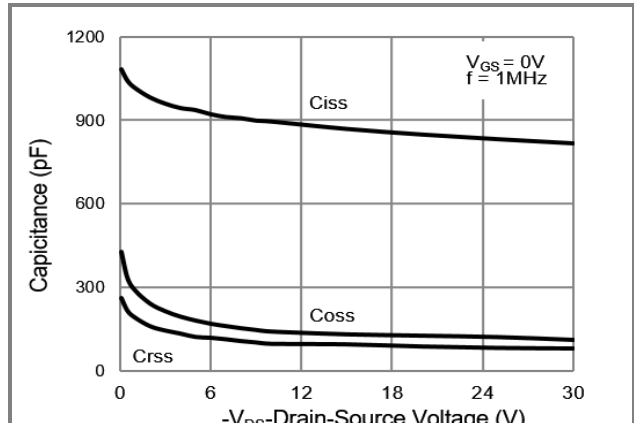


Fig.10 Capacitance vs. Drain-Source Voltage.

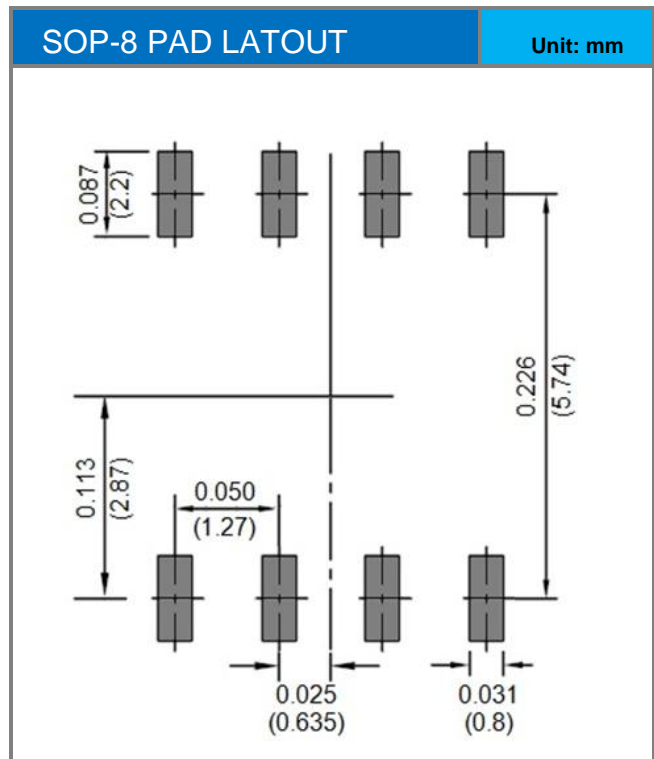
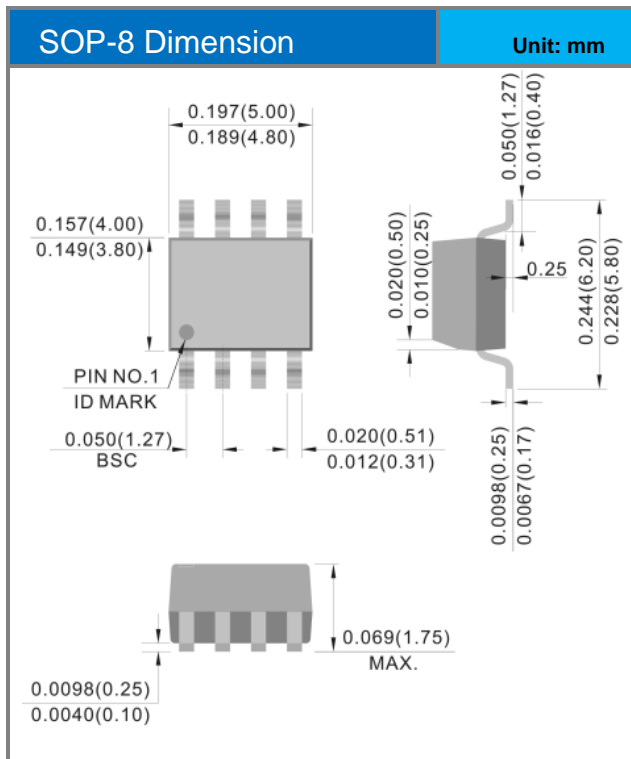


PJL9602

PART NO PACKING CODE VERSION

Part No Packing Code	Package Type	Packing type	Marking	Version
PJL9602_R2_00001	SOP-8	2.5K pcs / 13" reel	L9602	Halogen free

MOUNTING PAD LAYOUT





PJL9602

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