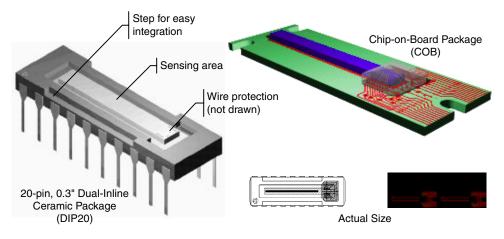
## Features

- Sensitive Layer Over a 0.8 mm CMOS Array
- Image Zone: 0.4 x 14 mm = 0.02" x 0.55"
- Image Array: 8 x 280 = 2240 pixels
- Pixel Pitch: 50 mm x 50 mm = 500 dpi
- Pixel Clock: up to 2 MHz Enabling up to 1780 Frames per Second
- Die Size: 1.7 x 17.3 mm
- Operating Voltage Range: Nominal 3V to 5.5V
- Power Consumption: 20 mW @ 3.3V, 1 MHz, 25°C
- Operating Temperature Range: 0°C to +70°C: C suffix (-40°C to +85°C to be characterized)
- Naturally Protected Against ESD: > 16 kV Air Discharge
- Resistant to Abrasion: >1 Million Finger Sweeps
- 20-lead Ceramic DIP or Chip-On-Board (COB) Package, with Specific Protective Layer

# Applications

- Terminal Access (PCs, access to networks, etc.)
- Electronic payment associated with payment card (Auto-mated Teller Machine, Portable Point Of Sale, etc.)
- Building access
- Electronic keys (cars, home, etc.)
- Cellular phones (usable only by registered users)
- Portable fingerprint imaging for law enforcement
- TV access
- Weapons (usable only by registered users)



# Description

FCD4A14 is part of the FingerChip<sup>™</sup> Atmel monolithic fingerprint sensor family for which no optics, no prism and no light source are required.

FCD4A14 is a single chip, high performance, low cost sensor based on temperature physical effects for fingerprint sensing.

FCD4A14 has a linear shape, allowing for the capture of a fingerprint image by sweeping the finger across the sensing area. After capturing several images, Atmel proprietary software can reconstruct a full 8-bit fingerprint image, if needed.

FCD4A14 has a small surface combined with CMOS technology, and a ceramic dualin-line or Chip-On-Board package assembly. These facts contribute to a low-cost device.





Thermal Fingerprint Sensor with 0.4 mm x 14 mm (0.02" x 0.55") Sensing Area and Digital Output (on-chip ADC)

# FDC4A14 FingerChip™

Rev. 1962A-01/00



FCD4A14 delivers a programmable number of images per second, while an integrated Analog to Digital Converter delivers a digital signal adapted to interfaces such as an EPP parallel port, USB microcontroller or directly to microprocessors. Thus, no frame grabber or glue interface is necessary to send the frames. These facts make FCD4A14 an easy device to include in any system for identification or verification applications.

## Absolute Maximum Ratings (1)

Parameter	Symbol	Comments	Value	Unit
Positive supply voltage	V <sub>cc</sub>		GND to 6.5	V
Temperature stabilization power	TPP		GND to 6.5	V
Front plane	FPL		GND to V <sub>CC</sub>	V
Digital input voltage	RSTPCLK		GND to V <sub>CC</sub>	V
Digital output current	I <sub>D</sub>			mA
Die temperature	Tj		-55 to +85	°C
Storage temperature	T <sub>stg</sub>		-55 to +85	°C
Lead temperature (soldering 10 s)	T <sub>leads</sub>	Do not solder DIP: socket mandatory	Forbidden	°C

Note: 1. Absolute maximum ratings are limiting values, to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability.

### **Recommended Conditions Of Use**

Parameter	Symbol	Comments	Min	Unit		
Positive supply voltage	V <sub>cc</sub>		3V			V
Front plane	FPL	Must be grounded.		V		
Digital input voltage				V		
Digital output voltage				V		
Digital load	CL			50		pF
Analog load	C <sub>A</sub>			20		pF
Analog loau	R <sub>A</sub>			10		kΩ
Operating temperature range	T <sub>amb</sub>	Civil: "C" grade		0 to +70		°C
Duty cycle	DC	Clock PCLK	20	50	80	%



# Resistance

	Min value	Standard method								
ESD										
On pins. HBM (Human Body Model) CMOS I/O	2 kV	MIL-STD-883- method 3015.7								
On die surface (Zapgun) Air discharge Contact	±16 kV ±9 kV	NF EN 6100-4-2 CEI 1000-4-2								
MECHANICAL ABRASION										
# cycles without lubricant multiply by a factor of 20 for correlation with a real finger	300 000	MIL E 12397B								
CHEMICAL RESISTANCE										
Cleaning agent, acid, grease, alcohol, diluted acetone	4 hours	Internal method								

# Specifications

Parameter	Symbol	T <sub>amb</sub>	Test level	Min	Тур	Мах	Unit
Resolution			IV		50		micron
Size			IV		8x280		pixel
Yield: number of bad pixels			I			15	bad pixels
Equivalent resistance on TPP pin			I		30		ohm

Expla	Explanation Of Test Levels						
I	100% production tested at +25°C						
II	100% production tested at +25°C, and sample tested at specified temperatures (AC testing done on sample)						
Ш	Sample tested only						
IV	Parameter is guaranteed by design and/or characterization testing						
V	Parameter is a typical value only						
VI	100% production tested at temperature extremes.						
D	100% probe tested on wafer at $T_{amb} = +25^{\circ}C$						



# 5 Volt

Power supply = +5V;  $T_{amb}$  = 25°C;  $F_{PCLK}$  = 1 MHz; Duty cycle = 50%;

 $C_{\text{load}}\,120~\text{pF}$  on digital outputs, analog outputs disconnected otherwise specified.

Parameter	Symbol	T <sub>amb</sub>	Test level	Min	Тур	Max	Unit
Power Requirements							
Positive supply voltage	V <sub>CC</sub>			4.5	5	5.5	V
Digital positive supply current on $V_{CC}$ pin			I		13		mA
C <sub>load</sub> = 0	I <sub>CC</sub>		IV		6		mA
Power dissipation on $V_{\text{CC}}$			I		65		mW
C <sub>load</sub> = 0	P <sub>CC</sub>		IV		30		mW
Power dissipation on $V_{\text{CC}}$ in NAP mode	P <sub>CCNAP</sub>		I			0.1	mW
Analog Output							
Voltage range	V <sub>AVx</sub>		I	0		2.8	V
Digital Inputs							
Logic compatibility					CMOS		
Logic "0" voltage	V <sub>IL</sub>		I	0		1.2	V
Logic "1" voltage	V <sub>IH</sub>		I	3.6		VCC	V
Logic "0" current	I <sub>IL</sub>		I			100	μA
Logic "1"current	I <sub>IH</sub>		I			100	μA
Digital Outputs C <sub>load</sub> 120 pF					-		
Logic compatibility					CMOS		
Logic "0" voltage <sup>(1)</sup>	V <sub>OL</sub>		I			1.5	V
Logic "1" voltage <sup>(1)</sup>	V <sub>OH</sub>		I	3.5			V
Output rise time (10% - 90% final value)	tr		IV		10		ns
Output rise time (10% - 90% final value)	tf		IV		5		ns

Note: 1. With  $I_{OL} = 1$  mA and  $I_{OH} = -1$  mA

FCD4A14

### 3.3 Volt

Power supply = +3.3V;  $T_{amb}$  = 25°C;  $F_{PCLK}$  = 1 MHz; Duty cycle = 50%;

 $C_{\text{load}}$  120 pF on digital outputs, analog outputs disconnected otherwise specified

Parameter	Symbol	<b>T</b> <sub>amb</sub>	Test level	Min	Тур	Max	Unit
Power Requirements							
Positive supply voltage	V <sub>CC</sub>			3.0	3.3	3.6	V
Digital positive supply current on $V_{CC}$ pin $C_{load} = 0$	I <sub>CC</sub>		l IV		10 6		mA mA
Power dissipation on $V_{CC}$ $C_{\text{load}} = 0 \label{eq:cc}$	P <sub>CC</sub>		l IV		33 20		mW mW
Power dissipation on $V_{CC}$ in NAP mode	P <sub>CCNAP</sub>					0.1	mW
Analog Output	L						
Voltage range	V <sub>AVx</sub>		I	0		2.8	V
Digital Inputs	L						
Logic compatibility					CMOS		
Logic "0" voltage	V <sub>IL</sub>		I	0		0.8	V
Logic "1" voltage	V <sub>IH</sub>		I	2.3		VCC	V
Logic "0" current	I <sub>IL</sub>		I			100	μA
Logic "1"current	I <sub>IH</sub>		I			100	μA
Digital Outputs C <sub>load</sub> 120 pF	L						
Logic compatibility					CMOS		
Logic "0" voltage <sup>(1)</sup>	V <sub>OL</sub>		I			0.6	V
Logic "1" voltage <sup>(1)</sup>	V <sub>OH</sub>		I	2.4			V
Output rise time (10% - 90% final value)	tr		IV		10		ns
Output rise time (10% - 90% final value)	tf		IV		5		ns

Note: 1. With  $I_{OL} = 1$  mA and  $I_{OH} = -1$  mA





# **Switching Performances**

 $T_{amb} = 25^{\circ}C$ ;  $F_{PCLK} = 1$  MHz; Duty cycle = 50%;  $C_{load}$  120 pF on digital and analog outputs otherwise specified

Parameter	Symbol	T <sub>amb</sub>	Test level	Min	Тур	Max	Unit
Clock frequency	F <sub>PCLK</sub>		I	0.1	1	2	MHz
Minimum clock pulse width (high)	T <sub>HCLK</sub>		I			250	ns
Minimum clock pulse width (low)	T <sub>LCLK</sub>		I			250	ns
Min clock setup time (high) / reset falling edge	T <sub>Setup</sub>		I			0	ns
Min clock hold time (high) / reset falling edge	T <sub>Hold</sub>		I			20	ns

## 5.0 Volt

All power supplies = +5 V

Parameter	Symbol	T <sub>amb</sub>	Test level	Min	Тур	Max	Unit
Output delay from PCLK to ACKN rising edge	T <sub>PLHACKN</sub>		I		20		ns
Output delay from PCLK to ACKN falling edge	T <sub>PHLACKN</sub>		I		17		ns
Output delay from PCLK to Data output Dxi	T <sub>PDATA</sub>		I		68		ns
Output delay from PCLK to Analog output Avx	T <sub>PAVIDEO</sub>		I		266		ns
Output delay from OE to data high-Z	T <sub>DATAZ</sub>		I		25		ns
Output delay from OE to data output	T <sub>ZDATA</sub>		I		29		ns

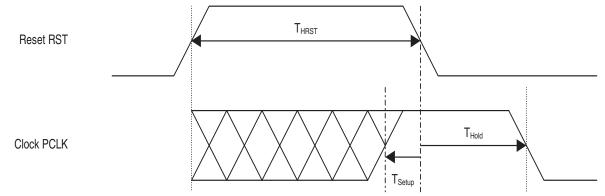
# 3.3 Volt

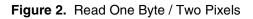
All power supplies = +3.3 V

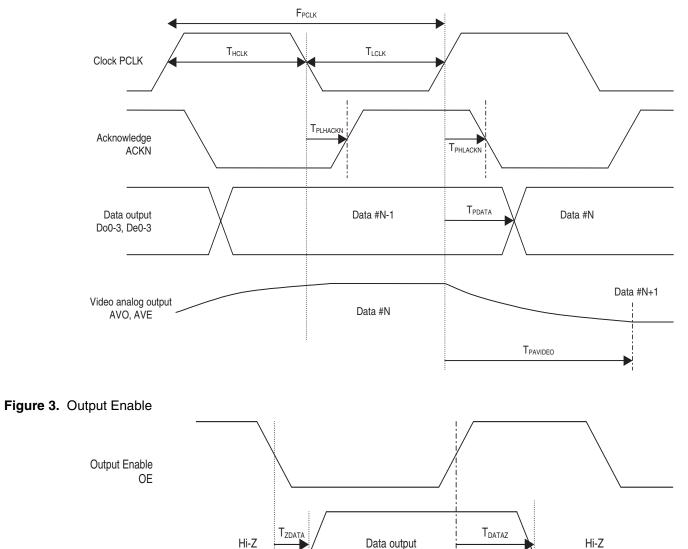
Parameter	Symbol	T <sub>amb</sub>	Test level	Min	Тур	Max	Unit
Output delay from PCLK to ACKN rising edge	T <sub>PLHACKN</sub>		I		31		ns
Output delay from PCLK to ACKN falling edge	T <sub>PHLACKN</sub>		I		26		ns
Output delay from PCLK to Data output Dxi	T <sub>PDATA</sub>		I		82		ns
Output delay from PCLK to Analog output AVx	T <sub>PAVIDEO</sub>		I		266		ns
Output delay from OE to data high-Z	T <sub>DATAZ</sub>		IV		34		ns
Output delay from OE to data output	T <sub>ZDATA</sub>		I		47		ns

# FCD4A14

Figure 1. Reset













Data output



Pin number	Name	Туре
1	GND	GND
2	AVE	Analog output
3	TPP	Power
4	VCC	Power
5	RST	Digital input
6	OE	Digital input
7	De0	Digital output
8	De1	Digital output
9	De2	Digital output
10	De3	Digital output
11	FPL	GND
12	Do3	Digital output
13	Do2	Digital output
14	Do1	Digital output
15	Do0	Digital output
16	GND	GND
17	ACKN	Digital output
18	PCLK	Digital input
19	TPE	Digital input
20	AVO	Analog output

GND	1		20	AVO
AVE	2		19	TPE
TPP	3	q     <b>       </b>     p	18	PCLK
VCC	4	d	17	ACKN
RST	5	d	16	GND
OE	6	Q     <b>B B</b>     P	15	Do0
De0	7	Q	14	Do1
De1	8		13	Do2
De2	9		12	Do3
De3	10		11	FPL

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Die Attach is connected to pin 1 and 16, and must be grounded. FPL pin must be grounded.

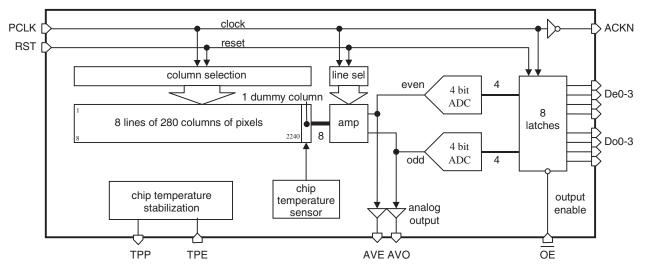
### Pad Connection For Chip-on-board Package

NameTypeGND 11GNDGND2AVEAnalog output3AVOAnalog output4TPPPower5TPEDigital input6VCCPower7GNDGND8RSTDigital input9PCLKDigital input10OEDigital output11ACKNDigital output12De0Digital output13Do0Digital output14De1Digital output15Do1Digital output16De2Digital output17Do2Digital output18De3Digital output19Do3Digital output20FPLGND21GNDGND		•		_	
1GNDGNDAVO32AVEAnalog outputTPP43AVOAnalog outputTPE54TPPPowerGND75TPEDigital inputRST86VCCPowerPCLK97GNDGNDOE108RSTDigital inputDe0129PCLKDigital inputDe11410OEDigital outputDo11512De0Digital outputDe21613Do0Digital outputDe31815Do1Digital outputGND2116De2Digital outputGND2118De3Digital output20FPL20FPLGNDKNDK	Pad number	Name	Туре		1
2AVEAnalog outputTPP43AVOAnalog outputTPE54TPPPowerGND75TPEDigital inputRST86VCCPowerPCLK97GNDGNDOE108RSTDigital inputACKN 119PCLKDigital inputDe01210OEDigital inputDe01311ACKNDigital outputDe11411ACKNDigital outputDe21613Do0Digital outputDo21714De1Digital outputDo31915Do1Digital outputFPL2016De2Digital outputGND19Do3Digital output204FPLGND4	1	GND	GND		3
4TPPPowerVCC65TPEDigital inputRST86VCCPowerPCLK97GNDGNDOE108RSTDigital inputDOE109PCLKDigital inputDe0129PCLKDigital inputDo11310OEDigital outputDo11512De0Digital outputDo21714De1Digital outputDo31915Do1Digital outputGND2116De2Digital outputGND2118De3Digital output20FPL20FPLGNDGND11	2	AVE	Analog output		4
4IPPPowelGND75TPEDigital inputRST86VCCPowerPCLK97GNDGNDOE108RSTDigital inputACKN 119PCLKDigital inputDe01210OEDigital inputDo01310OEDigital outputDe11411ACKNDigital outputDe21613Do0Digital outputDe21614De1Digital outputDo31915Do1Digital outputGND2116De2Digital outputGND18De3Digital outputGND20FPLGNDGND	3	AVO	Analog output		5
5TPEDigital inputRST86VCCPowerPCLK97GNDGNDOE108RSTDigital inputDOE109PCLKDigital inputDe01210OEDigital inputDo01310OEDigital outputDe11411ACKNDigital outputDo11512De0Digital outputDe21613Do0Digital outputDo21714De1Digital outputDo31915Do1Digital outputFPL2016De2Digital outputGND2118De3Digital output20FPL20FPLGNDGND11	4	TPP	Power		6
6VCCPowerPCLK 97GNDGNDOE108RSTDigital inputACKN 119PCLKDigital inputDe01210OEDigital inputDo11311ACKNDigital outputDe11411ACKNDigital outputDe21613Do0Digital outputDo21714De1Digital outputDo31915Do1Digital outputGND2116De2Digital outputGND2117Do2Digital outputGND2118De3Digital output20FPLQFPLGNDGND11	5	TPE	Digital input		
8RSTDigital inputACKN 119PCLKDigital inputDo0 1210OEDigital inputDo1 1311ACKNDigital outputDe1 1411ACKNDigital outputDo1 1512De0Digital outputDe2 1613Do0Digital outputDo2 1714De1Digital outputDe3 1815Do1Digital outputDo3 1916De2Digital outputFPL 2016De3Digital outputGND 2117Do2Digital outputGND 2118De3Digital output2019FPLGND	6	VCC	Power		
0FightDigital inputDe0129PCLKDigital inputDo01310OEDigital inputDe11411ACKNDigital outputDo11512De0Digital outputDe21613Do0Digital outputDe31814De1Digital outputDo31915Do1Digital outputFPL2016De2Digital outputGND2117Do2Digital outputGND2118De3Digital output20FPL20FPLGNDGND11	7	GND	GND		
9PCLKDigital inputDo01310OEDigital inputDe11411ACKNDigital outputDo11512De0Digital outputDe21613Do0Digital outputDe21714De1Digital outputDo31915Do1Digital outputFPL2016De2Digital outputGND2117Do2Digital outputGND2118De3Digital output20FPL20FPLGNDGND11	8	RST	Digital input		
10OEDigital inputDe11411ACKNDigital outputDo11512De0Digital outputDe21613Do0Digital outputDo21714De1Digital outputDe31815Do1Digital outputDo31916De2Digital outputGND2117Do2Digital outputGND2118De3Digital output20FPL20FPLGNDGND11	9	PCLK	Digital input		
11ACKNDigital outputDo11512De0Digital outputDe21613Do0Digital outputDo21714De1Digital outputDe31815Do1Digital outputDo31916De2Digital outputGND2117Do2Digital outputGND2118De3Digital output20FPL20FPLGNDGND11	10	OE	Digital input		
12De0Digital outputDe21613Do0Digital outputDo21714De1Digital outputDe31815Do1Digital outputDo31916De2Digital outputFPL2016De2Digital outputGND2117Do2Digital outputGND2118De3Digital output20FPL20FPLGNDGND11	11	ACKN	Digital output		
16De1Digital outputDe31814De1Digital outputDo31915Do1Digital outputFPL2016De2Digital outputGND2117Do2Digital outputGND2118De3Digital output20FPL20FPLGNDGND	12	De0	Digital output		16
14DefDigital outputDo31915Do1Digital outputFPL2016De2Digital outputGND2117Do2Digital output18De3Digital output19Do3Digital output20FPLGND	13	Do0	Digital output		
15Do1Digital outputFPL 2016De2Digital outputGND 2117Do2Digital output18De3Digital output19Do3Digital output20FPLGND	14	De1	Digital output		
16De2Digital outputGND 2117Do2Digital output18De3Digital output19Do3Digital output20FPLGND	15	Do1	Digital output		
17Do2Digital output18De3Digital output19Do3Digital output20FPLGND	16	De2	Digital output		21
19Do3Digital output20FPLGND	17	Do2	Digital output		
20 FPL GND	18	De3	Digital output		
	19	Do3	Digital output		
21 GND GND	20	FPL	GND		
	21	GND	GND		

Die Attach is connected to pin 1, 7 and 21, and must be grounded. FPL pin must be grounded.

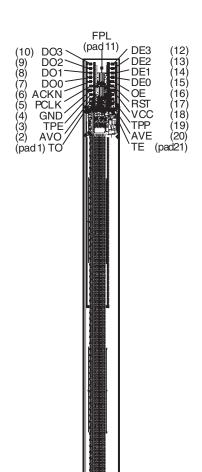
# FCD4A14

## FCD4A14 Block Diagram



## **Pin Description**

	Name	Pad	DIP	СОВ	Pin Type	Function
1	GND	4	1, 16	1,7,21	Ground	Ground
2	VCC	18	4	6	Power	Power supply
3	PCLK	5	18	9	Digital Input	Pixel clock
4	RST	17	5	8	Digital Input	Reset
5	OE	16	6	10	Digital Input	Data Output Enable. Tri-state when high
6	Do0	7	15	13	Digital Output	Odd pixel bit 0 LSB
7	Do1	8	14	15	Digital Output	Odd pixel bit 1
8	Do2	9	13	17	Digital Output	Odd pixel bit 2
9	Do3	10	12	19	Digital Output	Odd pixel bit 3 MSB
10	De0	15	7	12	Digital Output	Even pixel bit 0 LSB
11	De1	14	8	14	Digital Output	Even pixel bit 1
12	De2	13	9	16	Digital Output	Even pixel bit 2
13	De3	12	10	18	Digital Output	Even pixel bit 3 MSB
14	ACKN	6	17	11	Digital Output	Acknowledge signal / EPP protocol
15	FPL	11	11	20	Ground	Front plane. Must be grounded.
16	TPP	19	3	4	Power	Temp. stabilization power
17	TPE	3	19	5	Digital Input	Temp. stabilization enable
18	AVO	2	20	3	Analog Output	Analog output odd pixels
19	AVE	20	2	2	Analog Output	Analog output even pixels
20	то	1	N/A	N/A	Analog Input	Test purpose only
21	TE	21	N/A	N/A	Analog Input	Test purpose only



N/A: not available





### **Die Mechanical Information**

Mask set reference	H97A	Passivation/coating	Specific
Die size.	1.7 x 17.34 mm	Revision	A
Pad size	100 x 100 μm	Back side potential	Ground
Die thickness	675 ± 25 μm	Transistor count	18827
Metallization	Ti (front side)	Die attach	Ероху
	Poly (back side)	Bond wire	AlSi/Ti

## **Functional Description**

The circuit is divided into two main sections: sensor and data conversion. One particular column among 280+1 is selected in the sensor array (1), then each pixel of the selected column sends its electrical information to amplifiers (2) (one per line), then two lines at a time are selected (odd and even) so that two particular pixels send their information to the input of two 4 bit Analog to Digital Converters (3), so 2 pixels can be read for each clock pulse (4).

### Sensor

Each pixel is a sensor in itself. The sensor detects a temperature differential between the beginning of acquisition and the reading of information: this is the integration time. The integration time begins with a reset of the pixel to a predefined initial state. Note that the integration time reset has nothing to do with the reset of the digital section.

Then, at a rate depending on the sensitivity of the pyroelectric layer, on the temperature variation between the reset and the end of the integration time, and on the duration of the integration time, electrical charges are generated at the pixel level.

### Analog-to-Digital Converter / Reconstructing an 8-bit Fingerprint Image

An Analog to Digital Converter (ADC) is used to convert the analog signal coming from the pixel into digital data that can be used by a processor.

The U.S. Federal Bureau of Investigation requires a 256level grey scale image; that is, an 8 bit per pixel resolution.

As the data rate for parallel port and USB is in the range of 1 Megabyte per second, and we need at least a rate of 500 frames per second to reconstruct the image with a fair sweeping speed for the finger, two 4-bit ADCs have been used to output 2 pixels at a time on one byte. Then, as frames are recovered, the reconstruction routine computes an 8-bit value for each pixel. This value is calculated from the pixels of each frame coming from the device, which appear to be at the same place, therefore reducing noise and increasing resolution.

## **Start Sequence**

Although a reset is normally needed only once, after power up, it is better to reset the FingerChip before each fingerprint acquisition.

A reset is **not** necessary between each frame acquisition! Start sequence must consist of:

- 1. Set the RST pin to high
- 2. Set the RST pin to low
- 3. Send 4 clock pulses (due to pipe-line)
- 4. Send clock pulses to skip the first frame.

Note that the first frame never contains relevant information because the integration time is not correct.

## **Reading the Frames**

A frame consists of 280 true columns + 1 dummy column of 8 pixels. As two pixels are output at a time, a system must send 281x4 = 1124 clock pulses to read one frame.

Reset must be low when reading the frames.

# Read One Byte / Output Enable

Clock is taken into account on the falling edge and data are output on the rising edge.

For each clock pulse, after the start sequence, a new byte is output on the Do0-3, De0-3 pins. This byte contains 2 pixels: 4 bit on Do0-3 (odd pixels), 4 bit on De0-3 (even pixels).

To output the data, the output enable (OE) pin must be low. When OE is high, the Do0-3 & De0-3 pins are in high impedance state. This enables an easy connection to a microprocessor bus without additional circuitry-it will enable

FCD4A14

data output by using a chip select signal. Note that the FCD4A14 is always sending data: there is no data exchange to perform using read/write mode.

### Video Output

An analog signal is also available on pins AVE & AVO. Note that video output is available one clock pulse before the corresponding digital output (one clock pipe-line delay for the analog to digital conversion).

### **Pixel Order**

After a reset, pixel number one is located on the upper left corner, looking at the chip with bond pads to the right. For each column of 8 pixels, pixels 1-3-5-7 are output on odd data Do0-3 pins, pixels 2-4-6-8 are output on even data De0-3 pins. Most significant bit is bit #3, least significant is bit #0.

### Synchronization: The Dummy Column

A dummy column has been added to the sensor to act as a specific pattern to detect the first pixel. So, 280 true columns + 1 dummy column are read for each frame.

#### Figure 4.

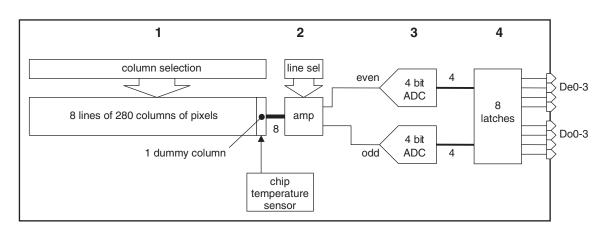
The 4 bytes of the dummy column contain a fixed pattern on the two first bytes, and temperature information on the last two bytes (see later):

	Even	Odd
Dummy Byte 1 DB1:	0000	1111
Dummy Byte 2 DB2:	0000	1111
Dummy Byte 3 DB3:	nnnn	rrrr
Dummy Byte 4 DB4:	рррр	tttt

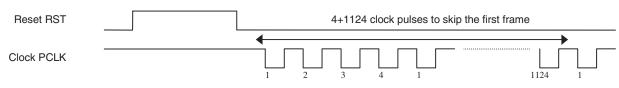
The sequence 00001111 00001111 is a very rare sequence in real fingerprint image, because it means that we have the sequence ridge/valley/ridge/valley within 4 pixels, that is 200mm. Moreover, this sequence appears on every frame (exactly every 1124 clock pulses), so it is an easy pattern to recognize for synchronization purposes.

### Integration Time and Clock Jitter

The FCD4A14 is not very sensitive to clock jitter (clock variation). The most important requirement is a regular integration time that ensures the frame reading rate is also as regular as possible, in order to get consistent fingerprint



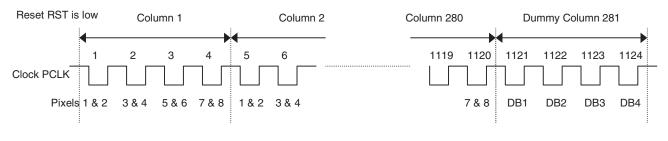
#### Figure 5. Start Sequence



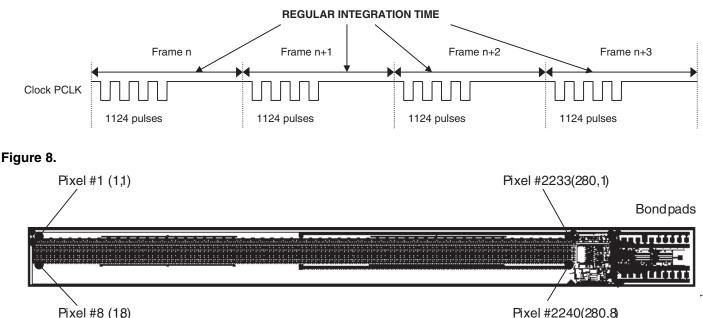




#### Figure 6. Read One Frame



#### Figure 7. Regular Integration Time



### **Temperature Management**

Each pixel of the FingerChip is a temperature sensor that detects temperature changes. This change is generated by the temperature difference between the finger and the chip. The best case happens when there is a large temperature difference, for instance when the chip temperature is very low or very high: this is a rather unusual case. The worst case happens when the finger temperature is exactly the same as the chip temperature.

In order to get a contrasted image, we need at least one degree difference between the sensor and the finger. Critical temperature is in the range of  $33^{\circ}C$  (±5 as finger temperature may vary). Chip temperature stabilization circuitry is implemented on the FCD4A14 to stabilize the sensor image quality when needed.

Several strategies may be used depending on external constraints:

- First, read the sensor temperature. Most of the time, it will be out of the critical area (near 33°C), so no stabilization is required.
- If power is not a critical resource, and if the sensor temperature is typically close to the critical area, the user may always stabilize the temperature above the usual finger temperature (>37°C). Note that this stabilization may take one minute or more, depending on the surroundings, thermal resistance and the chip's initial temperature.
- If power is a critical resource, the best solution is to have a first trial with the finger without stabilization as most of the time the temperature difference will be high enough. If authentication fails and we detect a chip temperature that is in the critical area, simply enable the stabilization feature and try again. It may take a few seconds, as we just need to stabilize a few degrees above the measured temperature.

Two separate features are available in the FCD4A14:

- 1. An absolute temperature sensor. Information is digitally provided in the dummy bytes DB3 and DB4.
- 2. Temperature stabilization circuitry, with two pins, TPP and TPE.

The stabilization feedback is externally managed: an external processor or algorithm will decide whether or not this feature is enabled. In this way, the user has full control over power consumption.

TPP is the pin that delivers power, and must be externally connected to the power supply through a resistor to limit the maximum current and avoid reaching extreme temperatures. Value of the resistor depends on external conditions such as voltage, environmental use, thermal isolation...

TPE controls the injected power: when the temperature is below the desired temperature, TPE must be set to high, and when the temperature is reached, TPE must be set to low. This is a digital input: no power is required to drive this pin, so any processor output or bus may drive it.

Please contact Atmel for more information and assistance in your specific application.

Temperature information is digitally provided on DB3 & DB4. Data format, values and a program to manage to manage the temperature stabilization circuitry will be available once characterization of the chip is complete.

### **Power Management**

### Nap Mode

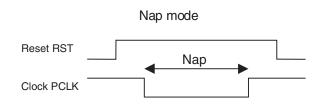
Several strategies are possible to reduce power consumption when not in use.

The simplest and most efficient is to cut the power supply, using external means.

A nap mode is also implemented in the FCD4A14. To activate this nap mode, user must:

- 1. Set the reset RST pin to high. Doing this, all analog sections of the device are internally powered down.
- 2. Set the clock PCLK pin to high (or low), thus stopping the entire digital section.
- 3. Set the TPE pin to low or disconnect TPP to stop the temperature stabilization feature.

4. Set Output Enable OE pin to high, so current can be drained through the outputs.



## **Application Notes**

### **Finger Speed Versus Acquisition Speed**

A finger speed is:

- very very slow below 1 cm/s
- slow at a few cm/s (you have to take care to go slowly)
- normal at 10 cm/s
- fairly fast at 20 cm/s
- maximum in the range of 100 cm/s (difficult to sweep)

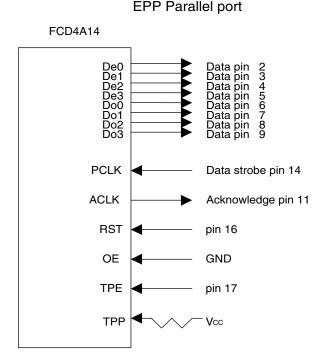
As a full fingerprint image is reconstructed from the slices, it is important that slices recover. The strict minimum is one line of recovery, but 2 lines recovery is a good value, so the finger must not move more than 6 pixels between two frames.

Maximum finger speed vs acquisition speed is summarized in the following figure, and will help the user define the system requirements for acquisition:

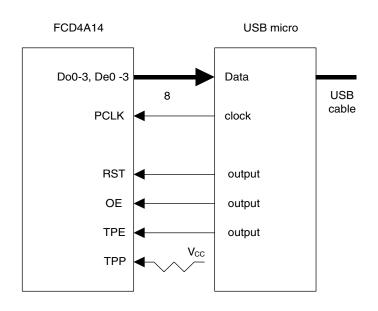
Acquisition Speed		Maximum Finger Speed	
kbyte/s	frame/s	cm/s	Comments
100	89	2.7	Slow
250	222	6.7	Normal/Bidir Parallel Port
700	623	18.7	Fair Speed/EPP
1000	890	26.7	Fast Speed/USB
1500	1335	40.0	Very Fast/Max USB
2000	1779	53.4	Extremely Fast







#### USB port



### **Parallel Port**

Parallel port must conform to the EPP specification for speed purposes. A standard bi-directional parallel port is able to acquire only about 200 kilobyte per second (it depends on the PC): this is three times slower than EPP. Thus the maximum finger speed is reduced 3 times.

The FCD4A14 can be directly connected to the parallel port without interface glue.

**FCD4A14** 

Power must be supplied via the PS/2 port, for instance, as power is not consistently available on the parallel port.

From a software point of view, the system must have a high priority during acquisition, because if the PC does something else (such as accessing the hard drive), some frames may be skipped resulting in a "hole" in the fingerprint image.

### **USB / Microprocessor**

The FCD4A14 is easy to connect to a microcontroller that will manage the USB protocol. The same applies for a microprocessor / microcontroller / DSP.

(see also FC15A140 application note 02).

The USB microcontroller will send the data read on the data bus directly on the USB cable. A program, called firmware, is run on the USB microcontroller, and another program, called the driver, is run on the host computer (generally a PC).

A transfer must be done, with a proper bandwidth reservation, to make sure that the acquisition is regular without skipping frames.

### Software

Atmel doesn't provide specific authentication software with the FingerChip. Imaging software is provided with the demonstration kit, so that it will be possible to evaluate the sensor's capabilities (standard bitmap image files of the fingerprint may be saved), but no matching software for extracting minutia and performing comparisons is provided.

FingerChip is compatible with software adapted to optical sensors, but it may be better to take advantage of the specific features of the device-particularly the fact that large images with more information may be obtained, thus enabling a reduction of the FAR & FRR.

Many of our FingerChip Partners have adapted (or are in the process of adapting) their algorithms and/or matching hardware to the FingerChip. If you need more information on these products, please contact Atmel or visit our web site.

# Reducing Area: Sweeping the Finger Over the Fingerchip

Reducing the cost of the sensor is one of the most important topics in fingerprint capture. In silicon sensors particularly, the smaller the area, the less expensive the device.

FingerChip technology delivers this size reduction by using an array with very few columns. A user sweeps his/her finger over the sensor, and FingerChip delivers a burst of images.

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# FCD4A14

At this time, two strategies are possible:

- reconstruct the complete fingerprint image, and then perform authentication
- analyze the images on the fly, and decide user is recognized if enough images are matched

Analysis on the fly is better from a user point of view, because the acceptance can be given before the end of the finger's sweep.

The clock rate has to be chosen carefully to enable the user to move his/her finger quite quickly, while also obtaining many overlapping images. With the FingerChip, it is possible, using only the images, to reconstruct the complete fingerprint without knowing the real speed of the finger.

Correlating two images to find out the distance between them seems at first to be too computer-time intensive. Yet while this is more or less true for the first two images, as we don't know the finger's speed, for the following images, the position is easily guessed as the speed of the finger is more or less constant, and a clever strategy may be used.

### **Software Library**

Atmel provides a dynamic linked library (FC\_GetImage.dll) with only one routine to call to get an image. Contact Atmel for the application note describing all the features of this library.

This library calls low-level routines to access hardware. Different libraries will exist, depending on the associated hardware (EPP/USB/etc.), but the call will remain the same, so developers do not need to update their software if the hardware changes.

The EPP version of the library is delivered with the parallel port kit.

### **Start And Stop Acquisition**

When the user is asked to sweep his/her finger, the system begins to analyze incoming images to detect the finger and avoid storing blank frames (in the case of storing images for later reconstruction, if not done on the fly).

The same problem occurs when acquisition must end. The provided library contains all the basic routines that perform these operations. This analysis is done on the fly.

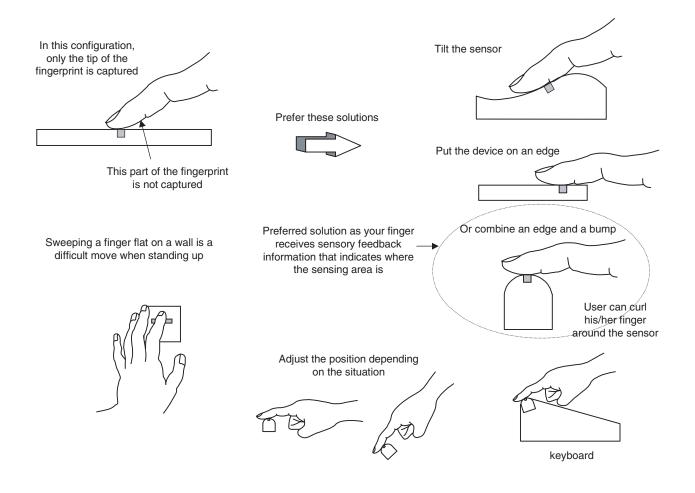
Note that it is very important to have a regular acquisition without (large) processor interrupts during storage of fingerprint slices (once the finger is detected). If slices are missing, it may be impossible to reconstruct a complete fingerprint image. Developers must take care to provide a high priority level during acquisition to the process, so that heavy applications running at the same time will not interfere.

#### Ergonomy

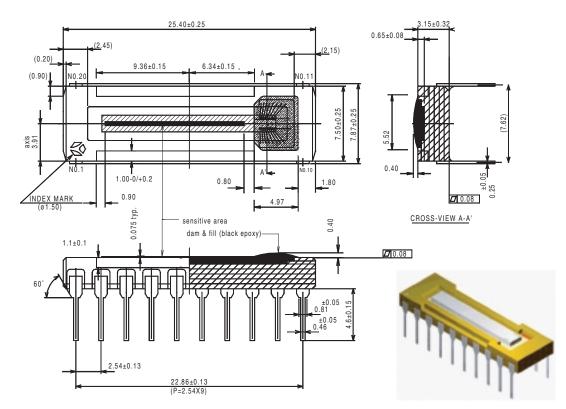
Special attention must be taken in order to make the sensor easy to use. The second level packaging (the box that contains the FingerChip and other electronic components) must allow the user to continuously touch the device during sweeping. Nothing should be placed in the path of the finger.

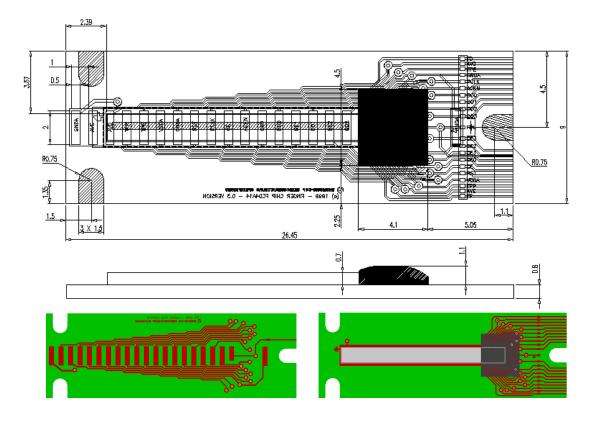
To make sure the finger touches the device, it is better to allow the user to curl his/her finger around the second level packaging. This also depends if you are standing or sitting in front of the device. For instance, it is very difficult to put your finger flat on a wall in front of you (see figure).





### Packaging: Mechanical Data



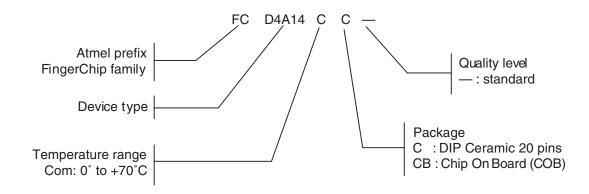






## **Ordering Information**

### Package device





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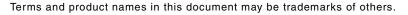
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